Reversed Temperature-Dependent Propagation Delay Characteristics in Nanometer CMOS Circuits

Ranjith Kumar and Volkan Kursun, *Member, IEEE*

***Abstract*—The supply voltage to threshold voltage ratio is reduced with each new technology generation. The gate overdrive variation with temperature plays an increasingly important role in determining the speed characteristics of CMOS integrated circuits. The temperature-dependent propagation delay characteristics, as shown in this brief, will experience a complete reversal in the near future. Contrary to the older technology generations, the speed of circuits in a 45-nm CMOS technology is enhanced when the temperature is increased at the nominal supply voltage. Operating an integrated circuit at the prescribed nominal supply voltage is not preferable for reliable operation under temperature fluctuations. A design methodology based on optimizing the supply voltage for temperature-variation-insensitive circuit performance is proposed in this brief. The optimum supply voltage is 45% to 53% lower than the nominal supply voltage in a 180-nm CMOS technology. Alternatively, the optimum supply voltage is 15% to 35% higher than the nominal supply voltage in a 45-nm CMOS technology. The speed and energy tradeoffs in the supply voltage optimization technique are also presented.**

***Index Terms*—High temperature speed, supply voltage scaling, temperature variations.**

I. Introduction

PROCESS and environment parameter variations in scaled CMOS technologies are posing greater challenges in the design of reliable integrated circuits. Because of the imbalanced utilization and diversity of circuitry at different sections of an integrated circuit, temperature can vary significantly from one die area to another [1]. Furthermore, environmental temperature fluctuations can cause significant variations in the die temperature. For example, electronic systems mounted on automobile engines operate at a temperature range from −40 °C to 150 °C [2]. Variations in the die temperature affect the device characteristics, thereby altering the performance of integrated circuits.

The supply and threshold voltage scaling trends are shown in Fig. 1 [3]. The supply voltage is scaled primarily based on the device reliability and target clock frequency requirements in a new technology generation. Scaling the device dimensions strengthens the electric fields between device terminals while lowering the parasitic capacitances, thereby enhancing the speed of CMOS integrated circuits. The speed of a circuit can be further enhanced by scaling the threshold voltages. Due to the subthreshold leakage current constraints, however, the threshold voltages are scaled at a much slower rate as compared to the supply voltage. The supply voltage to threshold voltage ratio is reduced with each new technology generation. The temperature-fluctuation-induced threshold voltage variation is therefore expected to have an increasingly important role in determining the MOSFET drain current variations when the temperature fluctuates. As shown in this brief, a complete reversal in the temperature-dependent speed characteristics of CMOS circuits will be observed in the near future.

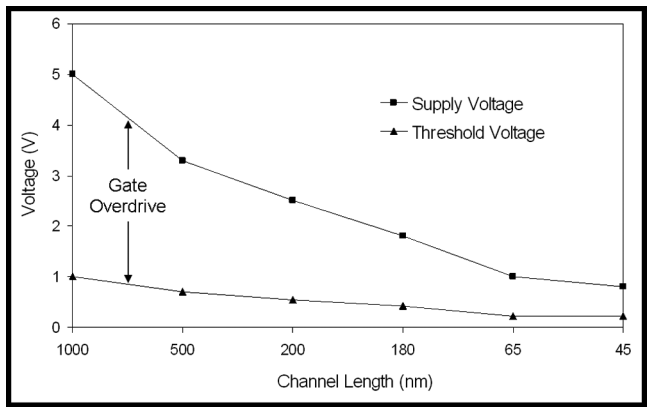

Fig. 1. Supply and threshold voltages in different CMOS technology generations.

Temperature-dependent device parameters that determine MOSFET current characteristics in the 180- and 45-nm CMOS technologies are identified in this brief. MOSFET current is characterized at elevated temperature and scaled supply voltages for two different CMOS technologies. A design methodology based on optimizing the supply voltage for temperature-variation-insensitive circuit performance is proposed. The optimum supply voltages providing temperature-variation-insensitive propagation delay are identified for a diverse set of circuits in the 180- and 45-nm CMOS technologies. The tradeoffs in the supply voltage optimization technique are presented.

This brief is organized as follows: Temperature-dependent device parameters that determine the drain current produced by a MOSFET are identified in Section II. Effects of temperature fluctuations on the device and circuit characteristics are examined in Section III. The optimum supply voltages providing temperature-variation-insensitive circuit performance are presented in Section IV. The tradeoffs of operating the circuits at the supply voltages that achieve temperature-variation-insensitive circuit speed are discussed in Section V. Finally, some conclusions are provided in Section VI.

Manuscript received July 11, 2005; revised May 16, 2006. This work was supported in part by the Wisconsin Alumni Research Foundation (WARF). This paper was recommended by Associate Editor A. G. Andreou

The authors are with the Department of Electrical and Computer Engineering, University of Wisconsin-Madison, Madison, WI 53706-1691 USA (e-mail: ranjithkumar@wisc.edu).

Digital Object Identifier 10.1109/TCSII.2006.882218

II. Factors Influencing MOSFET Current Under Temperature Fluctuations

Device parameters that are affected by temperature fluctuations, causing variations in the drain current produced by a MOSFET, are identified in this section. BSIM3 and BSIM4 MOSFET current equations are used for an accurate characterization of drain current in deeply scaled nanometer devices. The drain current of a MOSFET is as follows [4]–[6]:

$$I_{\rm ds} \propto \frac{I_{\rm ds0}}{1+\frac{R_{\rm ds}I_{\rm ds0}}{V_{\rm dseff}}} \tag{1}$$

$$I_{\rm ds0} \propto \frac{V_{\rm gsteff}\mu_{\rm eff}V_{\rm dseff}\left(1-\frac{A_{\rm bulk}V_{\rm dseff}}{2(V_{\rm gsteff}+2V_T)}\right)}{\left(1+\frac{V_{\rm dseff}}{E_{\rm SAT}L_{\rm eff}}\right)} \tag{2}$$

where $I_{\rm ds}$, $I_{\rm ds0}$, $R_{\rm ds}$, $V_{\rm dseff}$, $V_{\rm gsteff}$, $A_{\rm bulk}$, $\mu_{\rm eff}$, V_T, $E_{\rm SAT}$, and $L_{\rm eff}$ are the drain current with short-channel effects, drain current of a long-channel device, parasitic drain-to-source resistance, effective drain-to-source voltage, effective gate overdrive ($|V_{\rm GS}-V_t|$), parameter to model the bulk-charge effect, effective carrier mobility, thermal voltage, electric field at which the carrier drift velocity saturates, and effective channel length, respectively. Threshold voltage and carrier mobility are as follows [5], [6]:

$$\text{nMOS}: V_t(T) = V_t(T_0)+\left(\text{KT1}+\frac{\text{KT1}L}{L_{\rm eff}}+V_{\rm bseff}\text{KT2}\right)\left(\frac{T}{T_0}-1\right) \tag{3}$$

$$\text{pMOS}: V_t(T) = V_t(T_0)-\left(\text{KT1}+\frac{\text{KT1}L}{L_{\rm eff}}+V_{\rm bseff}\text{KT2}\right)\left(\frac{T}{T_0}-1\right) \tag{4}$$

$$\mu_{\rm eff}(T) = \left(U_0\left(\frac{T}{T_0}\right)^{U_{\rm te}}\right)\left\{1+\left(\frac{V_{\rm gsteff}+2V_t(T)}{T_{\rm OXE}}\right)^2 U_b(T) + (U_c(T)V_{\rm bseff}+U_a(T))\times\left(\frac{V_{\rm gsteff}+2V_t(T)}{T_{\rm OXE}}\right)\right\}^{-1} \tag{5}$$

where V_t, KT1, KT1L, KT2, $V_{\rm bseff}$, U_0, $U_{\rm te}$, $T_{\rm OXE}$, U_a, U_b, U_c, T_0, and T are the threshold voltage, temperature coefficient for threshold voltage, channel length dependence of the temperature coefficient for threshold voltage, body-bias coefficient of threshold voltage temperature effect, effective substrate bias voltage, mobility at the reference temperature, mobility temperature exponent, electrical gate-oxide thickness, first-order mobility degradation coefficient, second-order mobility degradation coefficient, body effect of mobility degradation coefficient, reference temperature, and the operating temperature, respectively.

As given by (3)–(5), absolute values of threshold voltage and carrier mobility degrade as the temperature is increased [4]–[6].

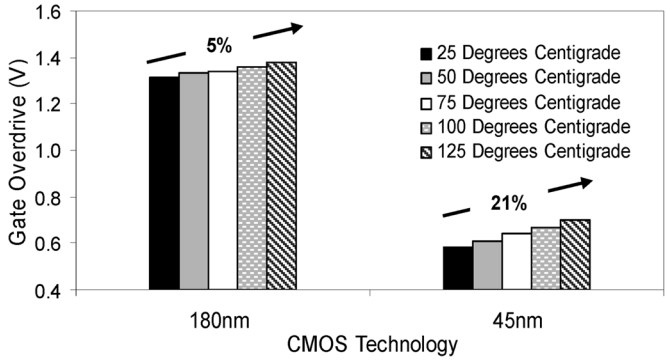

Fig. 2. Gate overdrive variation with temperature for an nMOS device in the 180- and 45-nm CMOS technologies.

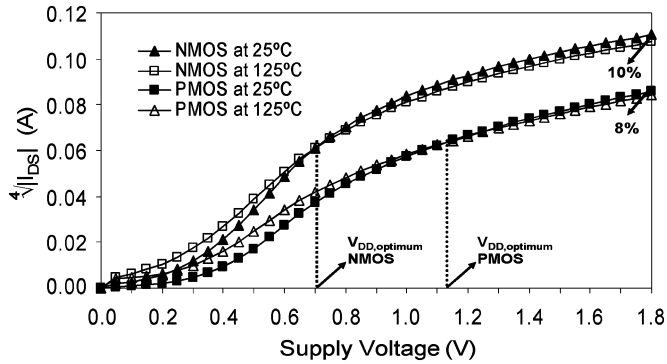

Fig. 3. Variation of MOSFET drain current ($I_{\rm DS}$) with supply voltage ($V_{\rm DD}$) and temperature in a 180-nm CMOS technology. $|V_{\rm DS}| = |V_{\rm GS}| = V_{\rm DD}$.

Threshold voltage degradation with temperature tends to enhance the drain current because of the increase in gate overdrive ($|V_{\rm GS}-V_t|$). Alternatively, degradation in carrier mobility tends to lower the drain current as given by (1) and (2). Effective variation of MOSFET current is therefore determined by the variation of the dominant device parameter when the temperature fluctuates.

III. Device and Circuit Behavior Under Temperature Fluctuations

Influence of temperature fluctuations on the device and circuit characteristics in TSMC 180-nm and Berkeley Predictive 45-nm CMOS technologies [7] are evaluated in this section. Temperature-fluctuation-induced gate overdrive variations at the nominal supply voltage are shown in Fig. 2 for an nMOS device in the 180- and 45-nm CMOS technologies. The nominal supply voltages are 1.8 and 0.8 V for the 180- and 45-nm CMOS technologies, respectively. Variation of the drain current ($I_{\rm DS}$) of nMOS and pMOS transistors with supply voltage ($V_{\rm DD}$) and temperature in the 180- and 45-nm CMOS technologies are shown in Figs. 3 and 4, respectively.

In older technology generations with higher supply voltage to threshold voltage ratio, the variation in the carrier mobility dominates the MOSFET current when the temperature fluctuates at the nominal supply voltage [9]. The MOSFET drain current and the circuit speed are therefore reduced following the degradation of carrier mobility when the temperature is increased, as shown in at the nominal supply voltage Fig. 3. The reduction

TABLE I
DELAY VARIATION WITH TEMPERATURE FOR CIRCUITS OPERATING AT THE NOMINAL SUPPLY VOLTAGE ($V_{DD} = 1.8$ V) IN A 180-nm CMOS TECHNOLOGY

180nm CMOS Technology	Temp (°C)	Inverter	NAND2	NAND4	NOR2	NOR4	XOR2	Domino AND2	Domino OR2	16-bit Brent Kung Adder
Average Delay (s)	25	2.88E-11	9.41E-11	1.45E-10	1.21E-10	2.49E-10	6.12E-11	6.06E-11	5.18E-11	1.28E-09
	125	3.06E-11	1.10E-10	1.74E-10	1.37E-10	2.81E-10	6.79E-11	6.90E-11	5.84E-11	1.44E-09
Delay Variation (%)		6.4	16.6	19.6	13.2	13.0	11.0	14.0	12.8	12.6

TABLE II
DELAY VARIATION WITH TEMPERATURE FOR CIRCUITS OPERATING AT THE NOMINAL SUPPLY VOLTAGE ($V_{DD} = 0.8$ V) IN A 45-nm CMOS TECHNOLOGY

45nm CMOS Technology	Temp (°C)	Inverter	NAND2	NAND4	NOR2	NOR4	XOR2	Domino AND2	Domino OR2	16-bit Brent Kung Adder
Average Delay (s)	25	4.13E-11	6.59E-11	1.21E-10	1.38E-10	3.55E-10	2.91E-10	4.53E-11	5.24E-11	1.98E-09
	125	3.87E-11	6.12E-11	1.13E-10	1.32E-10	3.42E-10	2.69E-10	4.15E-11	4.66E-11	1.74E-09
Delay Variation (%)		-6.29	-7.24	-7.02	-4.08	-3.61	-7.32	-8.51	-11.04	-12.07

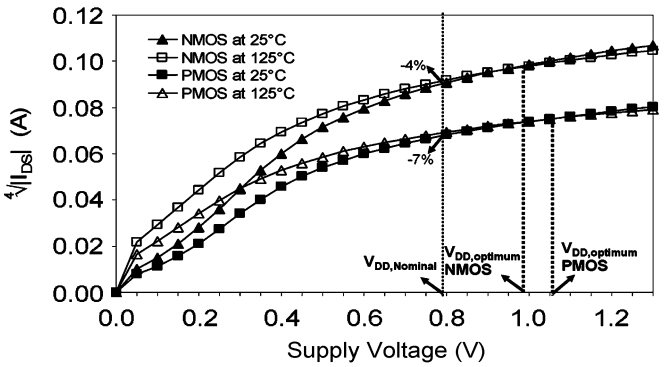

Fig. 4. Variation of MOSFET drain current (I_{DS}) with supply voltage (V_{DD}) and temperature in a 45-nm CMOS technology. $|V_{DS}| = |V_{GS}| = V_{DD}$.

in the supply voltage to threshold voltage ratio with technology scaling enhances the rate of increase of the gate overdrive with the increased temperature, as shown in Figs. 1 and 2. The enhanced sensitivity of the gate overdrive to the fluctuations of the temperature alters the device and circuit characteristics in deeply scaled CMOS technologies. Contrary to the devices in a 180-nm CMOS technology, MOSFET drain current increases at the nominal supply voltage when the temperature is increased in a 45-nm CMOS technology, as shown in Fig. 4. The increase in the drain current with temperature indicates that the temperature-dependent propagation delay characteristics of nanometer CMOS circuits will experience a complete reversal in the near future due to the lagging threshold voltage scaling.

Test circuits are designed for equal low-to-high and high-to-low propagation delays at the worst case temperature. Propagation delay variations with temperature for the test circuits operating at the nominal supply voltage in the 180- and 45-nm CMOS technologies are listed in Tables I and II, respectively. When operating at the nominal supply voltage, the speed degrades by up to 19.6% as the temperature is increased from 25 °C to 125 °C in a 180-nm CMOS technology. Alternatively, the speed is enhanced by up to 12% with increased temperature for the circuits in a 45-nm CMOS technology. The reversal in the temperature-dependent speed characteristics confirms the gate-overdrive-dominated current characteristics of the devices in scaled nanometer CMOS technologies. The enhancement of the circuit speed with the increased temperature is expected to add a new dimension to the design process of future integrated circuits.

IV. SUPPLY VOLTAGE OPTIMIZATION

The results presented in Section III indicate that operating an integrated circuit at the prescribed nominal supply voltage is not preferable for reliable operation under temperature variations. A new design methodology is desirable for suppressing the delay variations due to temperature fluctuations. There exists a gate bias voltage for which the variation of the carrier mobility is compensated by the variation of the gate overdrive when the temperature fluctuates [8], [10]. A transistor biased at this optimum voltage produces a temperature-variation-insensitive constant drain saturation current, as illustrated in Figs. 3 and 4. The optimum supply voltages for a diverse set of circuits in the 180- and 45-nm CMOS technologies are listed in Tables III and IV, respectively.

In a 180-nm CMOS technology, the propagation delay of a circuit operating at the nominal supply voltage is determined primarily by the variations of the mobility as the temperature fluctuates. To compensate the carrier mobility variations, the sensitivity of the gate overdrive to the temperature fluctuations should be enhanced by lowering the supply voltage. At the optimum supply voltage, the gate overdrive variation completely counterbalances the variation of the carrier mobility when the temperature fluctuates. As listed in Table III, the circuits in the 180-nm CMOS technology display a temperature-variation-insensitive propagation delay characteristics when operated at a

TABLE III
OPTIMUM SUPPLY VOLTAGES FOR TEMPERATURE-VARIATION-INSENSITIVE PROPAGATION DELAY CHARACTERISTICS IN A 180-nm CMOS TECHNOLOGY

180nm CMOS Technology	Temp (°C)	Inverter	NAND2	NAND4	NOR2	NOR4	XOR2	Domino AND2	Domino OR2	16-bit Brent Kung Adder
Average Delay (s) at Optimum Supply Voltage	25	5.78E-11	3.05E-10	5.78E-10	3.01E-10	6.61E-10	1.67E-10	1.84E-10	1.47E-10	3.50E-09
	125	5.79E-11	3.05E-10	5.81E-10	3.01E-10	6.62E-10	1.67E-10	1.84E-10	1.47E-10	3.50E-09
Delay Variation (%)		0.09	0.14	0.50	0.22	0.13	-0.12	0.26	-0.01	0.03
Optimum Supply Voltage (V)		0.97	0.89	0.85	0.99	0.97	0.97	0.94	0.95	0.96

TABLE IV
OPTIMUM SUPPLY VOLTAGES FOR TEMPERATURE-VARIATION-INSENSITIVE PROPAGATION DELAY CHARACTERISTICS IN A 45-nm CMOS TECHNOLOGY

45nm CMOS Technology	Temp (°C)	Inverter	NAND2	NAND4	NOR2	NOR4	XOR2	Domino AND2	Domino OR2	16-bit Brent Kung Adder
Average Delay (s) at Optimum Supply Voltage	25	3.67E-11	5.71E-11	1.03E-10	1.27E-10	3.38E-10	2.46E-10	4.02E-11	4.20E-11	1.55E-09
	125	3.64E-11	5.68E-11	1.02E-10	1.29E-10	3.40E-10	2.48E-10	4.03E-11	4.20E-11	1.55E-09
Delay Variation (%)		-1.00	-0.63	-0.80	0.89	0.55	0.69	0.17	0.04	-0.21
Optimum Supply Voltage (V)		0.97	0.99	1.00	0.94	0.92	1.00	1.08	1.07	1.05

TABLE V
PERCENT DELAY VARIATION AT THE LOWEST, HIGHEST, AND AVERAGE OPTIMUM SUPPLY VOLTAGES

Percent Delay Variation	Supply Voltage (V)	Inverter	NAND2	NAND4	NOR2	NOR4	XOR2	Domino AND2	Domino OR2	16-Bit Brent-Kung Adder
180nm CMOS Technology	(Min. Optimum) = 0.85	-4.2	-2.2	0.5	-7.9	-7.2	-6.9	-5.1	-6.1	-6.5
	(Max. Optimum) = 0.99	0.6	5.6	8.5	0.2	1.4	0.8	3.2	1.6	1.2
	(Avg. Optimum) = 0.92	-1.4	2.2	5.3	-3.1	-2.4	-2.5	-0.4	-1.6	-1.7
45nm CMOS Technology	(Min. Optimum) = 0.92	-1.9	-2.0	-3.0	-1.8	0.6	-1.9	-6.1	-5.0	-5.7
	(Max. Optimum) = 1.08	2.4	2.0	2.2	7.4	8.7	3.1	0.2	0.4	0.9
	(Avg. Optimum) = 1.00	0.4	0.2	0.8	5.2	5.5	0.7	-2.6	-2.0	-2.2

supply voltage that is 45% to 53% lower than the nominal supply voltage.

Alternatively, in a deeply scaled nanometer CMOS technology such as the 45-nm CMOS technology considered in this brief, the speed of a circuit operating at the nominal supply voltage is determined primarily by the variations of the gate overdrive as the temperature fluctuates. In order for the mobility variations to compensate the gate overdrive variations, the sensitivity of the gate overdrive to the temperature fluctuations should be weakened by increasing the supply voltage. At the optimum supply voltage, the carrier mobility variation completely counterbalances the gate overdrive variation. As listed in Table IV, the circuits in the 45-nm technology exhibit temperature-variation-insensitive speed for the supply voltages that are 15% to 35% higher than the nominal supply voltage.

Generating a unique supply voltage for each individual circuit is not feasible. In an integrated circuit based on the proposed voltage optimization technique, only one or a small subset of these optimum supply voltages would be employed. The percent delay variations with temperature when circuits are operated at the lowest, highest, and average $((\text{lowest}+\text{highest})/2)$ optimum supply voltage (for each technology) are listed in Table V. As listed in Table V, the delay variations are within 5.5% when the circuits operate at the average optimum supply voltage in both technologies. The proposed design technique of operating large-scale designs at a supply voltage close to the optimum supply voltage to reduce the sensitivity of the circuit speed to temperature variations is therefore feasible.

V. TRADEOFFS IN THE SUPPLY VOLTAGE OPTIMIZATION TECHNIQUE

The tradeoffs of operating the circuits at the supply voltages providing temperature-variation-insensitive circuit performance are discussed in this section. The energy per cycle and the propagation delay at the nominal supply voltage and the optimum supply voltages are compared. As listed in Tables I and III, when

TABLE VI
NORMALIZED ENERGY AT THE NOMINAL AND OPTIMUM SUPPLY VOLTAGES FOR CIRCUITS IN THE 180- AND 45-nm CMOS TECHNOLOGIES

Normalized Energy per Switching Cycle		Temp (°C)	Inverter	NAND2	NAND4	NOR2	NOR4	XOR2	Domino AND2	Domin o OR2	16-Bit Brent-Kung Adder
180nm CMOS Technology	Nominal Supply Voltage (V_{DD}= 1.8)	25	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
		125	1.01	1.01	1.02	1.02	1.02	1.01	1.01	1.02	1.02
	Optimum Supply Voltage	V_{DD}	0.97	0.89	0.85	0.99	0.97	0.97	0.94	0.95	0.96
		25	0.29	0.21	0.19	0.26	0.24	0.29	0.24	0.26	0.27
		125	0.30	0.21	0.19	0.26	0.25	0.29	0.24	0.26	0.27
45nm CMOS Technology	Nominal Supply Voltage (V_{DD}= 0.8)	25	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
		125	1.03	1.05	1.08	1.13	1.18	1.11	1.18	1.20	2.18
	Optimum Supply Voltage	V_{DD}	0.97	0.99	1.00	0.94	0.92	1.00	1.08	1.07	1.05
		25	1.46	1.52	1.59	1.43	1.38	1.54	1.79	1.72	1.79
		125	1.50	1.57	1.67	1.56	1.58	1.70	1.99	1.98	3.76

circuits in a 180-nm CMOS technology are operated at the optimum supply voltages, the circuit speed is degraded by up to 299% as compared to the speed at the nominal supply voltage. Alternatively, as listed in Tables II and IV, the speed of circuits in a 45-nm CMOS technology is enhanced by up to 22% at the optimum supply voltages providing temperature-variation-insensitive circuit speed.

The energy per cycle at the nominal supply voltage and the optimum supply voltages providing temperature-variation-insensitive propagation delay are listed in Table VI. The energy consumed by circuits operating at the optimum supply voltage is 71% to 81% lower than the energy consumed at the nominal supply voltage in a 180-nm CMOS technology. Alternatively, circuits in a 45-nm CMOS technology consume 33% to 79% higher energy per switching cycle at the optimum supply voltages, as listed in Table VI.

The optimum supply voltages for temperature-variation-insensitive circuit performance are lower than the nominal supply voltage in a 180-nm CMOS technology. The proposed supply voltage optimization technique is therefore attractive for low-power circuits with relaxed speed requirements in this 180-nm CMOS technology. Alternatively, reduction in the supply voltage to threshold voltage ratio shifts the region where the temperature-variation-insensitive circuit performance is observed for a 45-nm CMOS technology. The penalties paid for achieving temperature-variation-insensitive delay in a deeply scaled technology with reversed temperature dependence are the higher energy consumption and the degradation in the long-term device reliability due to the optimum supply voltages that are higher than the nominal supply voltage.

VI. CONCLUSION

The temperature-fluctuation-induced propagation delay variations in CMOS integrated circuits are examined in this brief. Temperature-dependent device parameters that cause variations in MOSFET drain current are identified. The gate overdrive variation with temperature plays an increasingly important role in determining the speed of CMOS integrated circuits with the scaling of technology. It is shown that the propagation delay is reduced with the increased temperature in a 45-nm CMOS technology, indicating a complete reversal in the temperature-dependent speed characteristics of nanometer CMOS integrated circuits.

A design methodology based on optimizing the supply voltage for temperature-variation-insensitive circuit performance is presented. The supply voltages, which compensate the temperature-fluctuation-induced variations of the carrier mobility and the threshold voltage, are identified for circuits in two different technology generations. The circuits display a temperature-variation-insensitive behavior when operated at a supply voltage that is 45% to 53% lower than the nominal supply voltage in a 180-nm CMOS technology. Alternatively, the circuits in a deeply scaled 45-nm CMOS technology exhibit temperature-variation-insensitive behavior for the supply voltages that are 15% to 35% higher than the nominal supply voltage.

REFERENCES

[1] S. Borkar *et al.*, "Parameter variation and impact on circuits and microarchitecture," in *Proc. IEEE/ACM Int. Des. Autom. Conf.*, Jun. 2003, pp. 338–342.
[2] R. W. Johnson *et al.*, "The changing automotive environment: High temperature electronics," *IEEE Trans. Electron. Packag. Manuf.*, vol. 27, no. 3, pp. 164–176, Jul. 2004.
[3] Y. Taur, "CMOS design near the limit of scaling," *IBM J. Res. Develop.*, vol. 46, no. 2/3, p. 213, May 2002.
[4] Y. Cao *et al.*, "New paradigm of predictive MOSFET and interconnect modeling for early circuit design," in *Proc. IEEE Custom Integr. Circuits Conf.*, Jun. 2000, pp. 201–204.
[5] W. Liu *et al., BSIM3v3.2.2 MOSFET model-user manual*. Berkeley, CA: Dept. Elect. Comput. Eng., Univ. California, 1999.
[6] X. Xi *et al., BSIM4.3.0 MOSFET model-user manual*. Berkeley, CA: Dept. Elect. Comput. Eng., Univ. California, 2003.
[7] ASU, Berkeley Predictive Technology Model (BPTM) Dept. of EE, Arizona State Univ., Tempe, AZ, 2006 [Online]. Available: http://www.eas.asu.edu/~ptm/
[8] Y. P. Tsividis, *Operation and Modeling of the MOS Transistor*. New York: McGraw-Hill, 1999.
[9] R. Kumar and V. Kursun, "A design methodology for temperature variation insensitive low power circuits," in *Proc. ACM/SIGDA Great Lakes Symp. VLSI*, May 2006, pp. 410–415.
[10] A. Bellaouar, A. Fridi, M. J. Elmasry, and K. Itoh, "Supply voltage scaling for temperature insensitive CMOS circuit operation," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 45, no. 3, pp. 415–417, Mar. 1998.