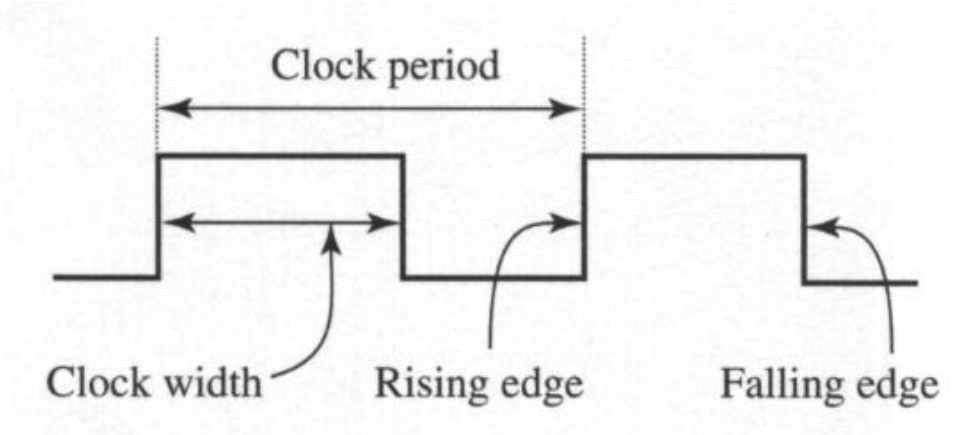
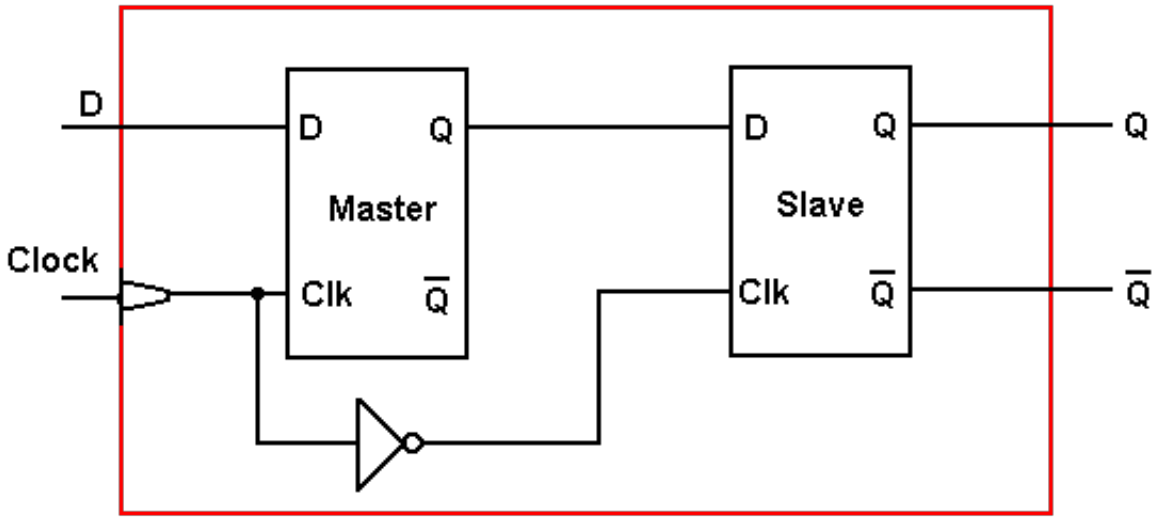
GLOBAL CLOCK SIGNAL
KIRK GOLENIAK

Definition

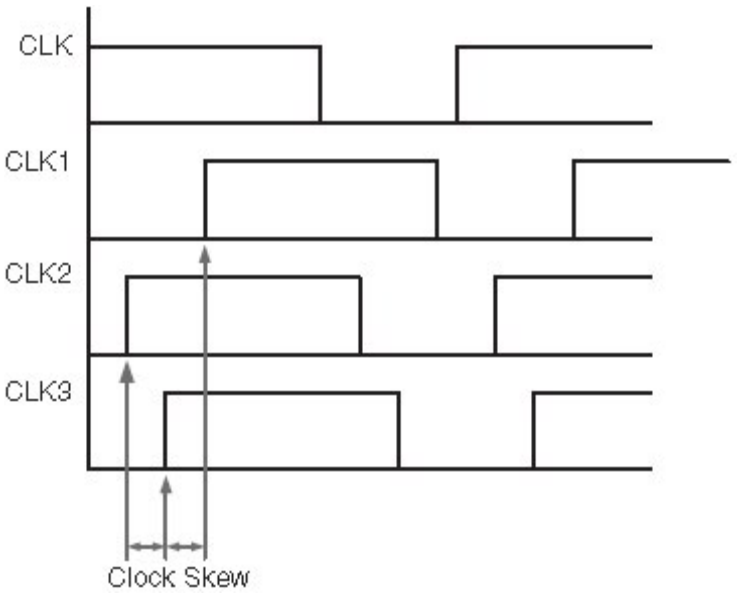
- Synchronous Design
- Omnipresent
- Implications

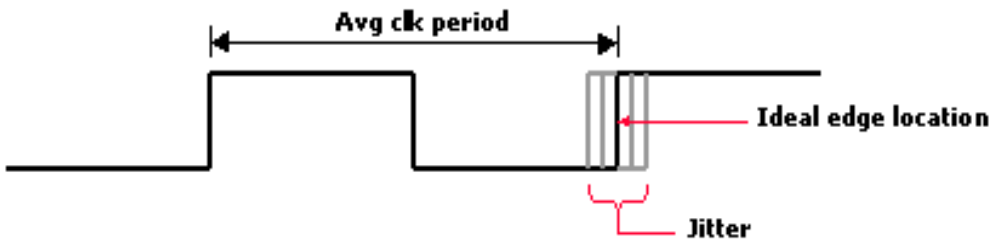




Clock Alignment

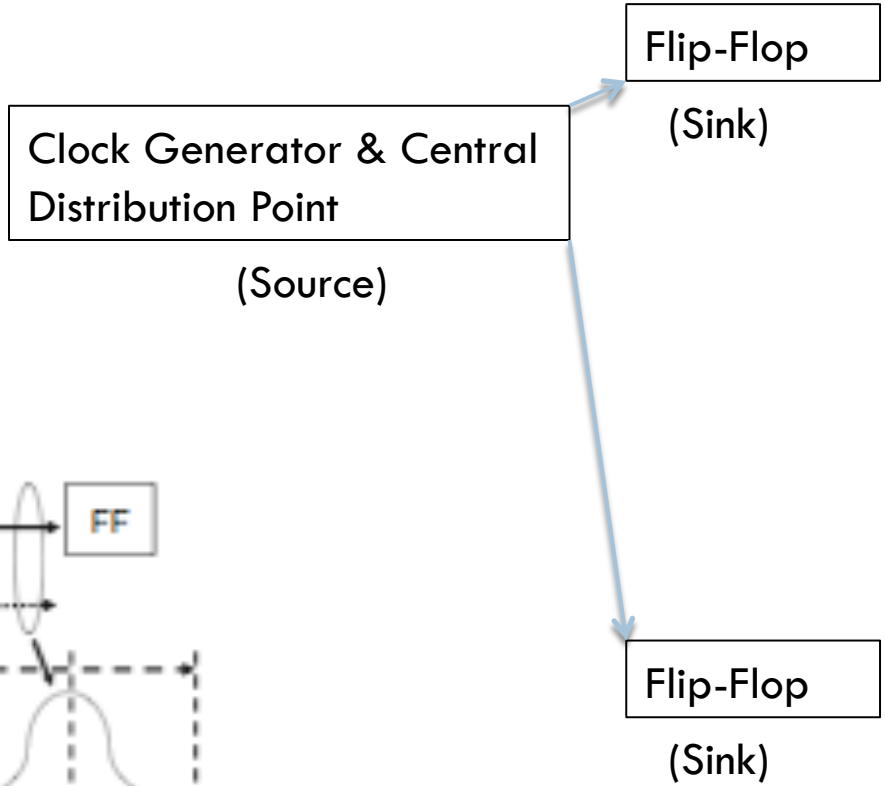
- Skew (spatial variation)
  - Non-uniform loads
  - Temperature gradients (time varying)
  - Process variations
- Jitter (temporal variation)
  - Random
  - Dynamic Variations
  - Absolute Jitter

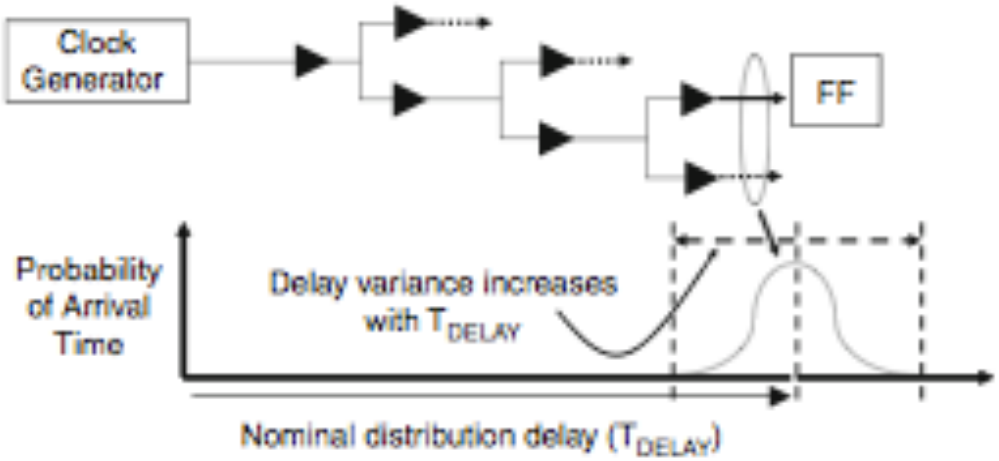




Design Methodology

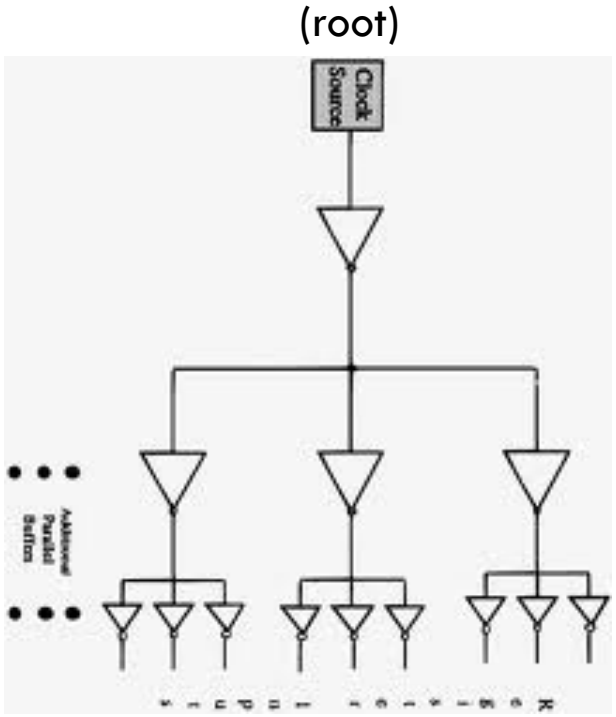
- Absolute Delay VS. Phase Delay
- Prefer Upper Metal Layers
- Segmentation & Buffers





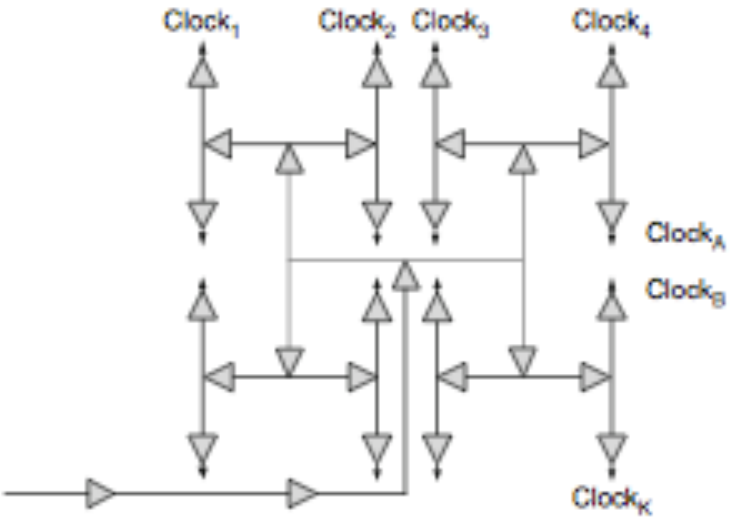
Balanced Trees

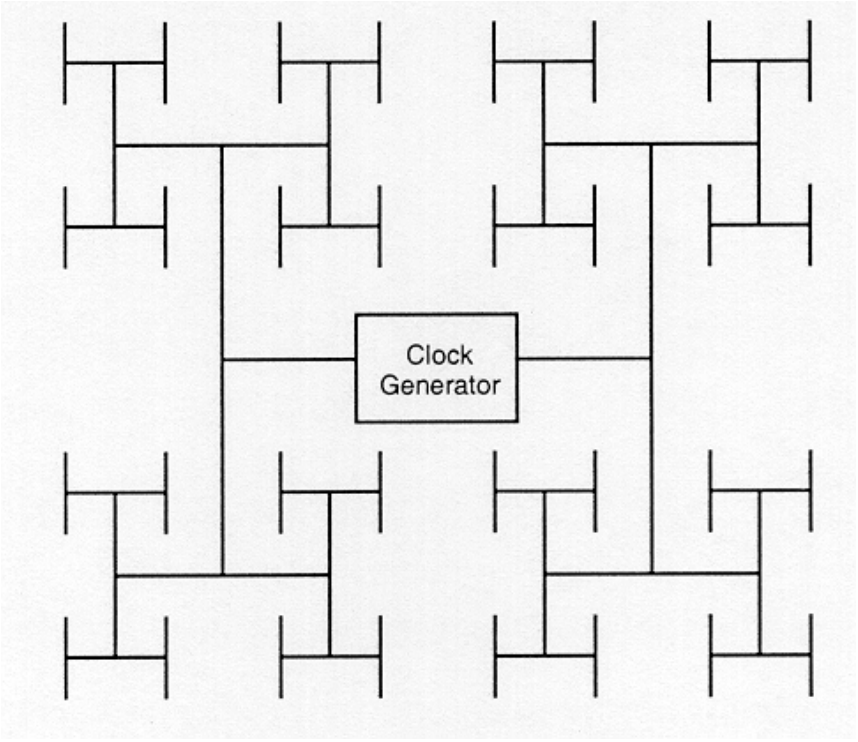
- Hierarchy
  - Partition into balanced load segments
- Balanced Paths (Delay Matching)
  - Modify path delay
  - Matched interconnect & buffers
- Automatic Generation



H-Tree Structure

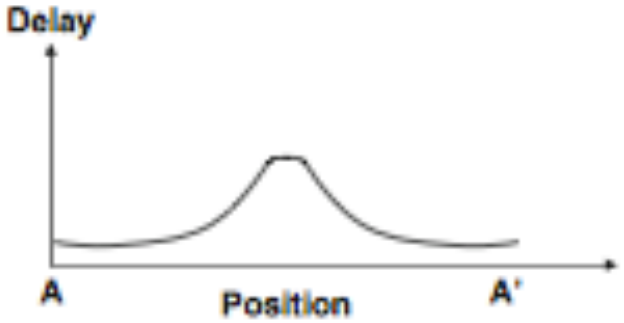
- Recursive
- Matched

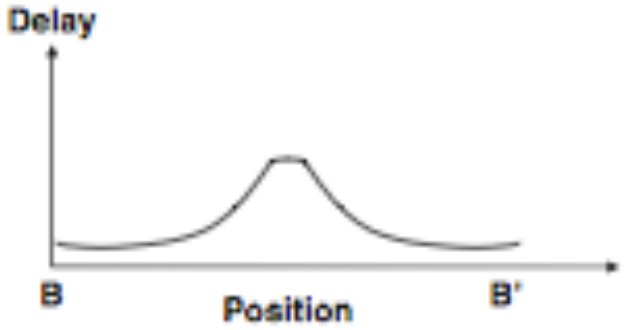


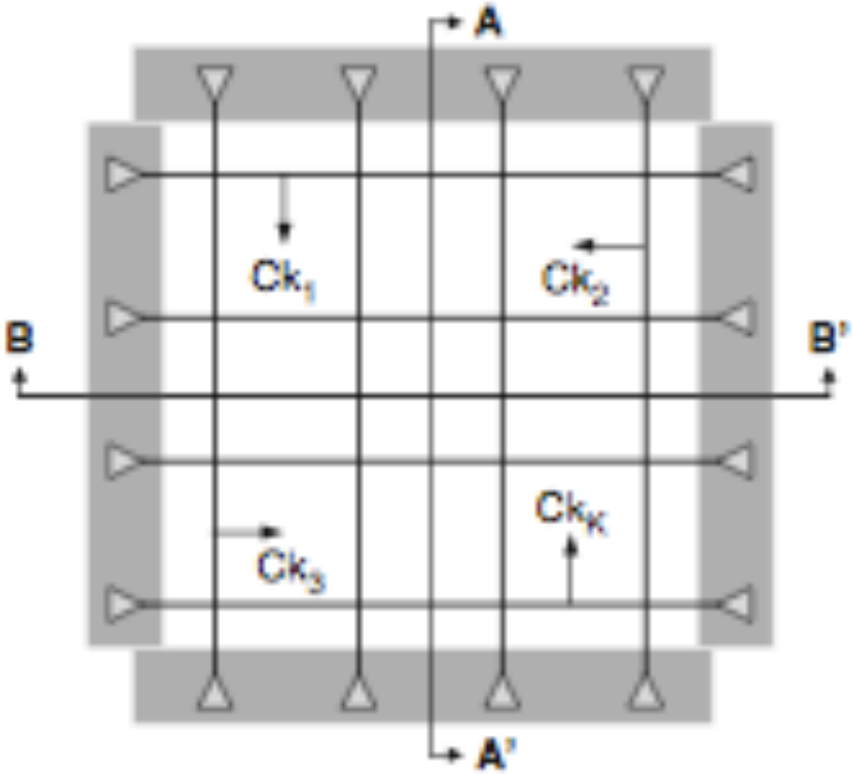


Grid Structure

- Design Flexibility
- Power Consumption

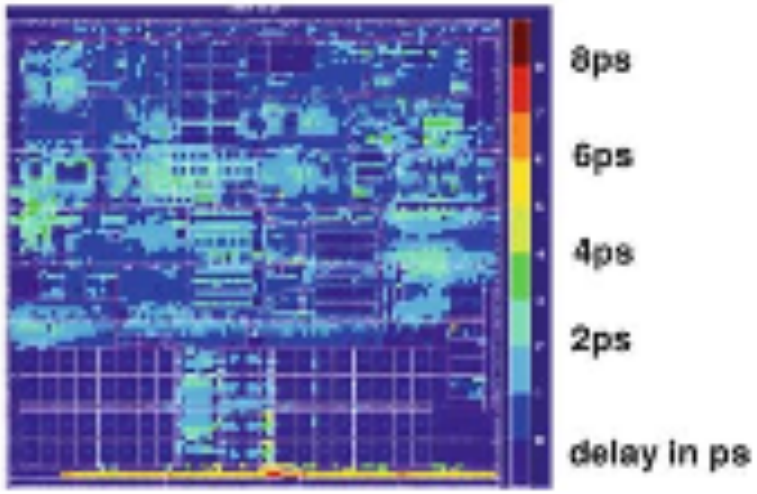




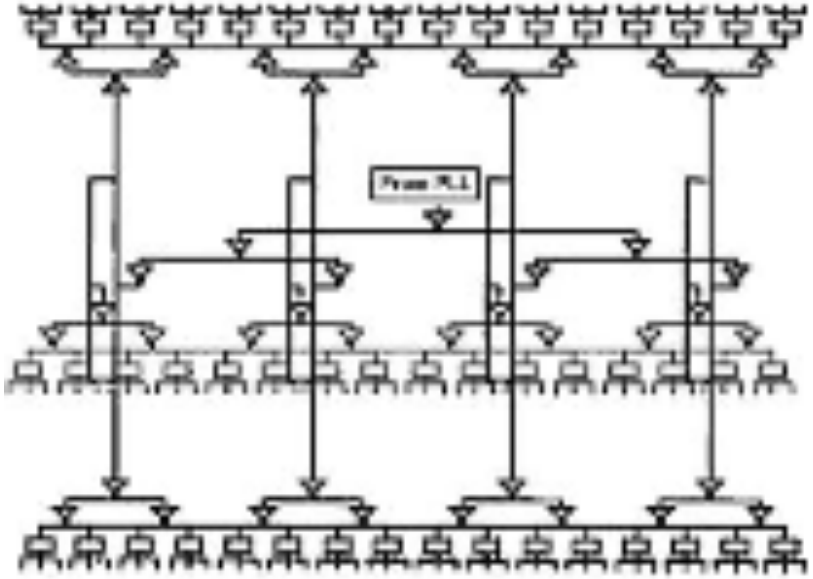


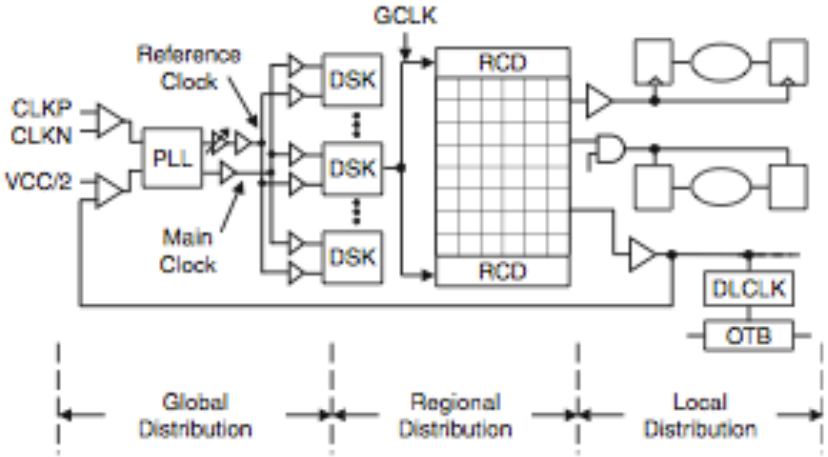
Examples (No Single Solution)

System Wide Clock Delay Measurements



Spine Distribution Network





Hierarchical Network