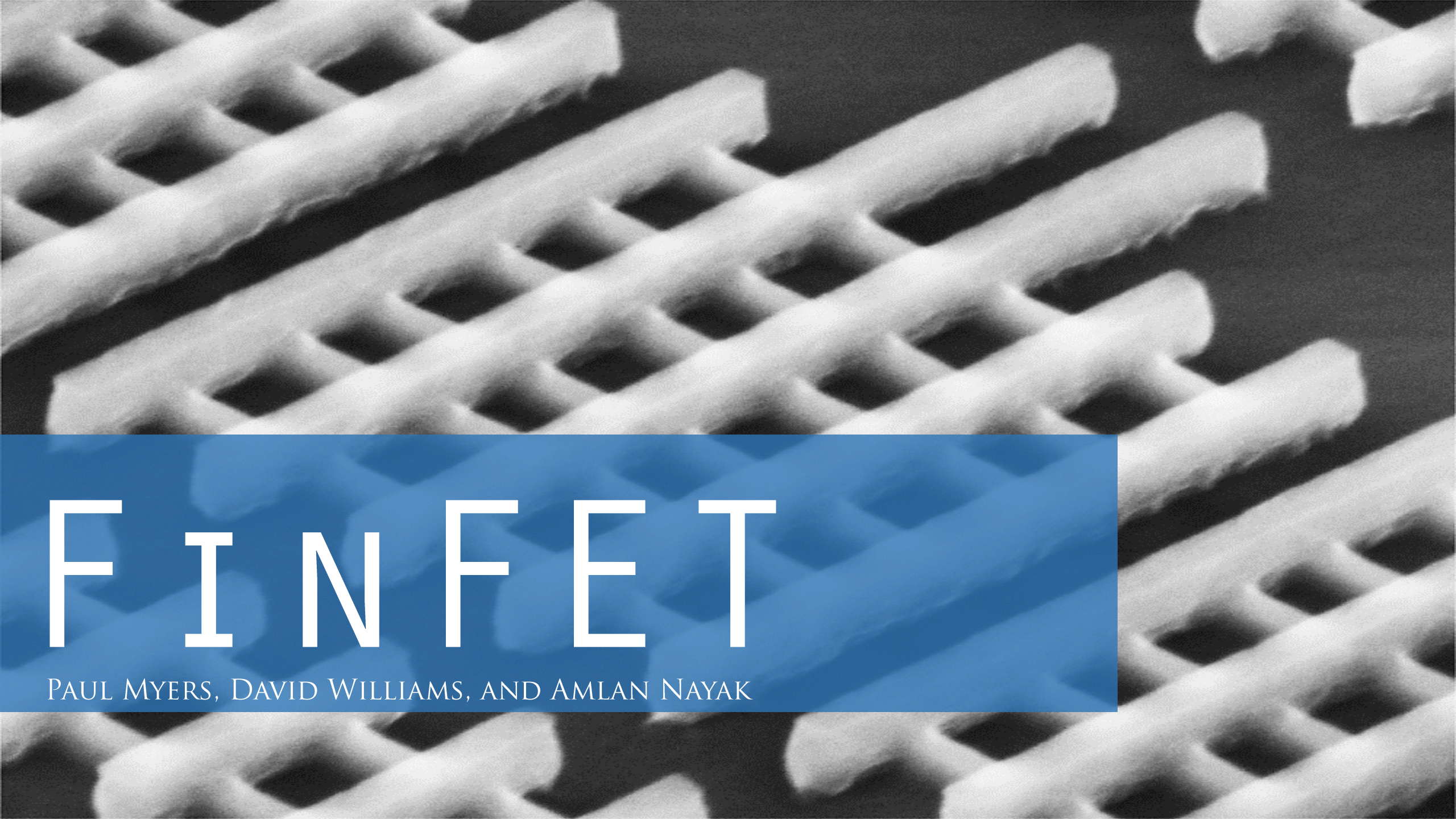


# FinFET

Paul Myers, David Williams, and Amlan Nayak

# Overview

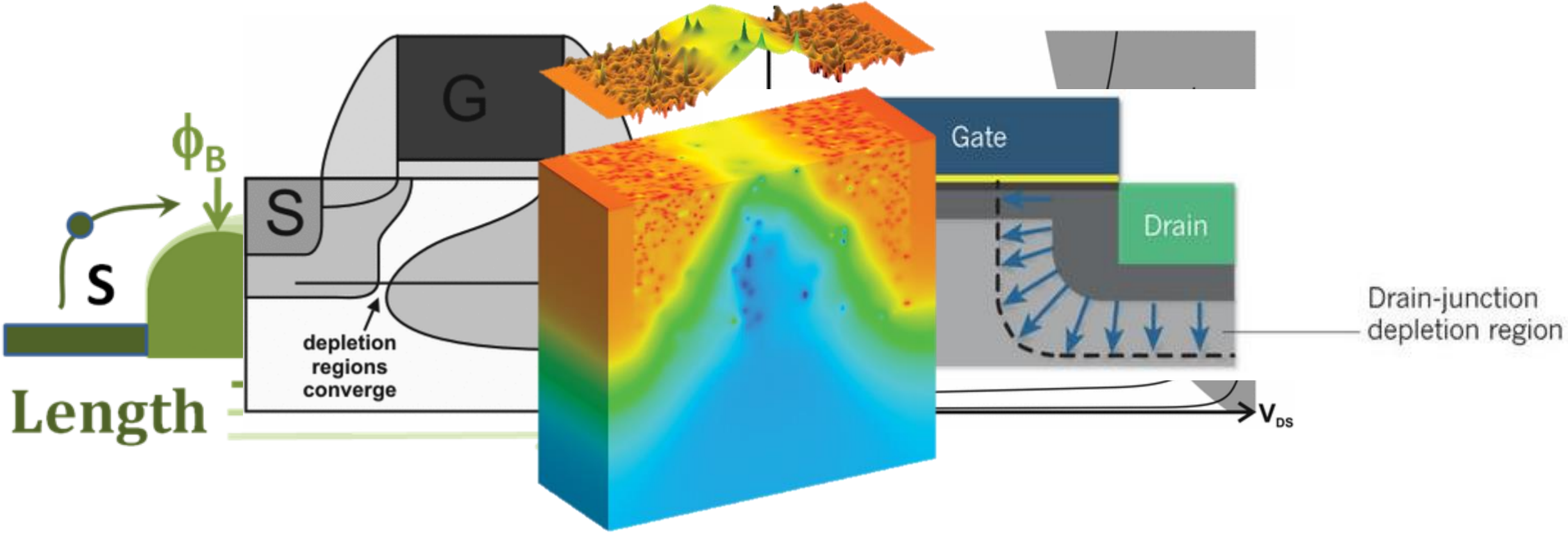
- Motivation
- Combatting Issues/Solutions
- FinFETs
- FinFET Logic Design/Schematic
- Implementations
- Questions

# Short Channel Effects

Drain Induced Barrier Lowering(DIBL)

Random Dopant Fluctuation(RDF)

Punch Through

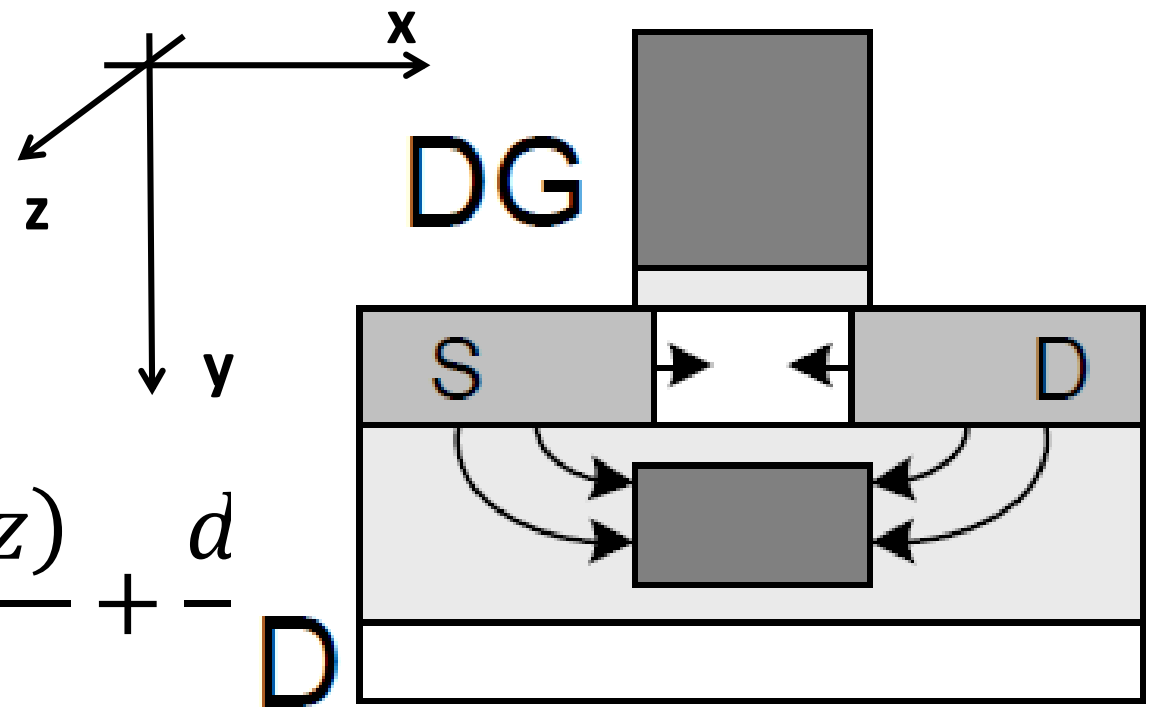


# Quantitative Analysis I

## Poisson's Equation:

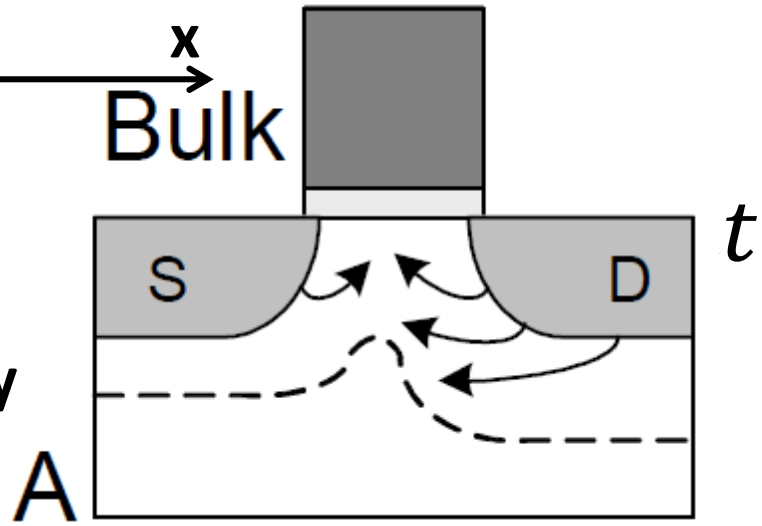
## Use:

$$\frac{d^2\Phi(x,y,z)}{dx^2} + \frac{d^2\Phi(x,y,z)}{dy^2} + \frac{d}{dz}$$




## Re-write:

$$\frac{dE_x(x,y,z)}{dx} + \frac{dE_y(x,y,z)}{dy} + \frac{dE_z(x}{dz}$$




Analysis drawn from: *FinFETs and Other Multi-Gate Transistors* by Jean-Pierre Colinge

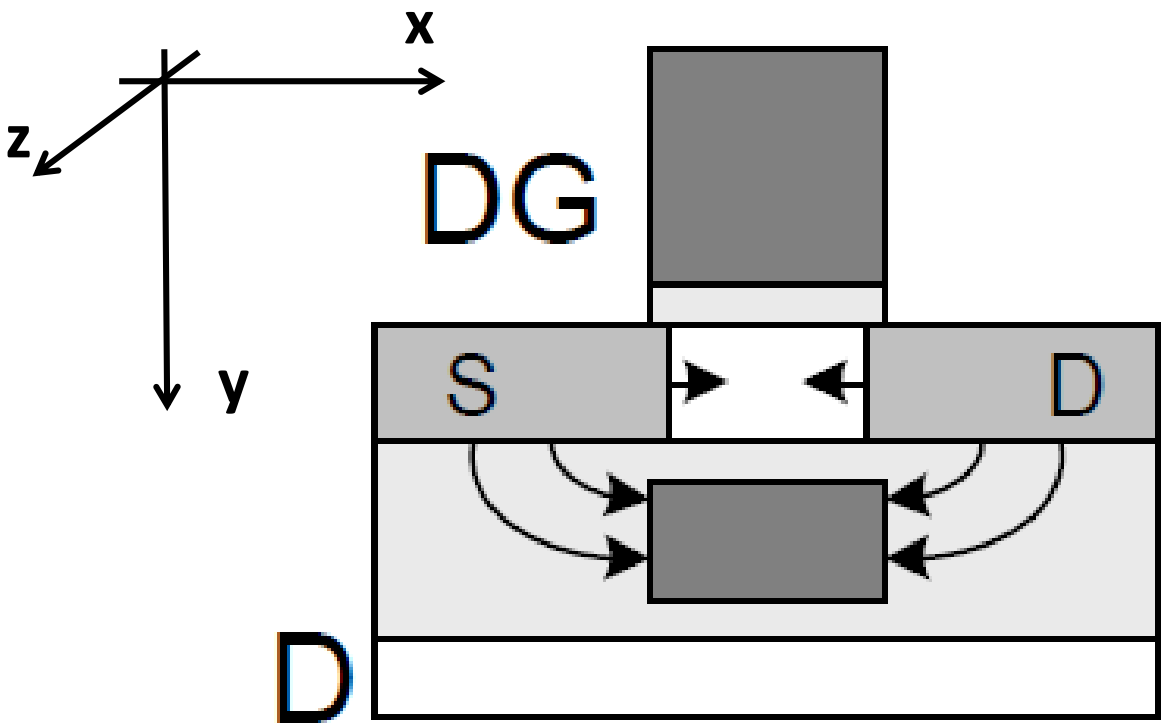
# Quantitative Analysis III

Result:

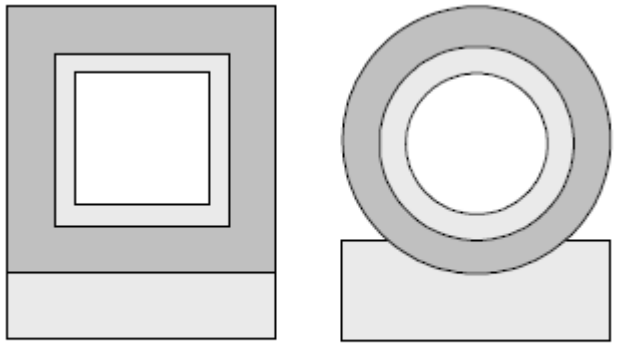
$$\Phi(x,0) \sim e^{-\frac{x}{\lambda}}$$

Natural length (eigenvalue):

$$\lambda \equiv \sqrt{\frac{\epsilon_{Si}}{m \cdot \epsilon_{OX}} t_{OX} t_{Si}}$$



# Natural Length



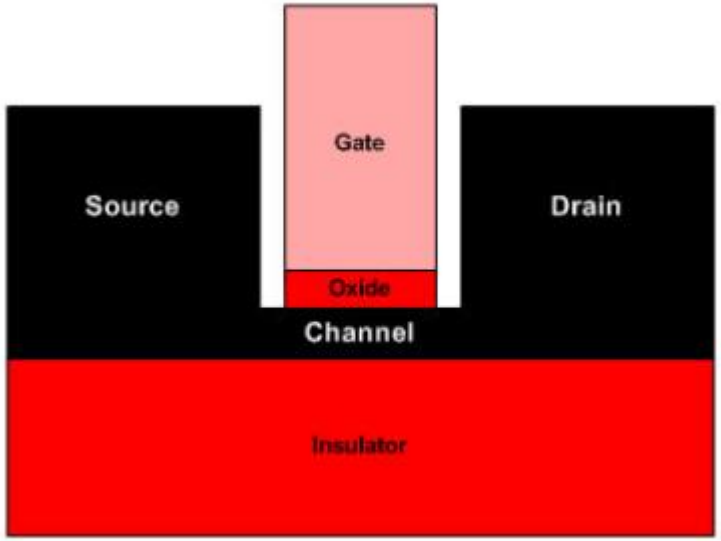
Quadruple gate FET

Cylindrical FET

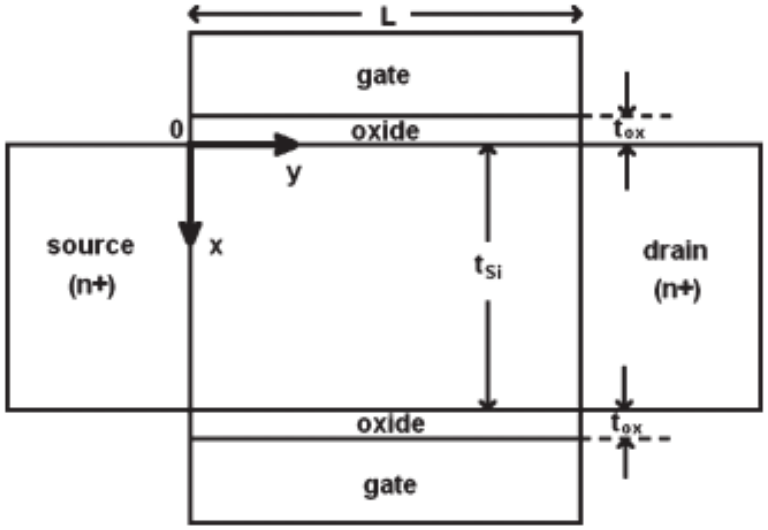
Table 1
Natural length in devices with different geometries

| | | | |
|---|---|---|---|
| Single-gate | $\lambda_1 = \sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{si} t_{ox}}$ [33] | – | |
| Double-gate | $\lambda_2 = \sqrt{\frac{\varepsilon_{si}}{2\varepsilon_{ox}} t_{si} t_{ox}}$ [33] | $\lambda_4 = \sqrt{\frac{\varepsilon_{si}}{2\varepsilon_{ox}} \left(1 + \frac{\varepsilon_{ox} t_{si}}{4\varepsilon_{si} t_{ox}}\right) t_{si} t_{ox}}$ [34] | |
| Surrounding-gate | $\lambda_3 \cong \sqrt{\frac{\varepsilon_{si}}{4\varepsilon_{ox}} t_{si} t_{ox}}$ (square-section) | $\lambda_5 = \sqrt{\frac{2\varepsilon_{si} t_{si}^2 \ln\left(1 + \frac{2t_{ox}}{t_{si}}\right) + \varepsilon_{ox} t_{si}^2}{16\varepsilon_{ox}}}$ (circular cross-section) | [35] |

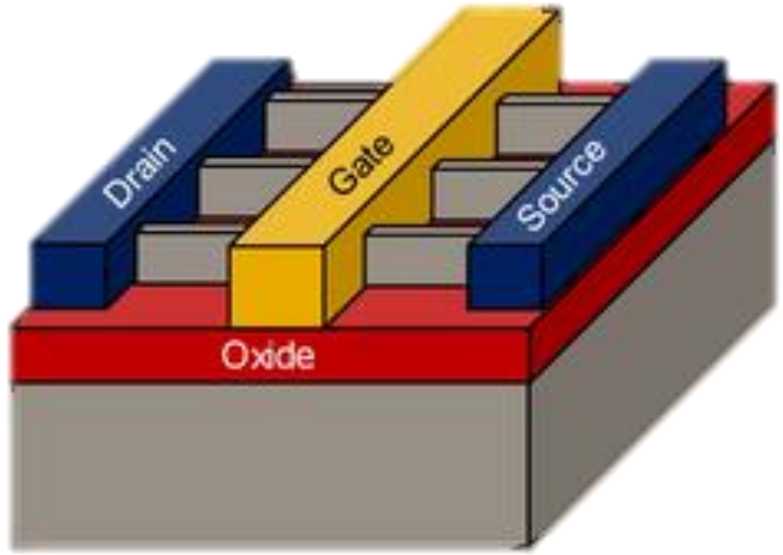
# MuGFET



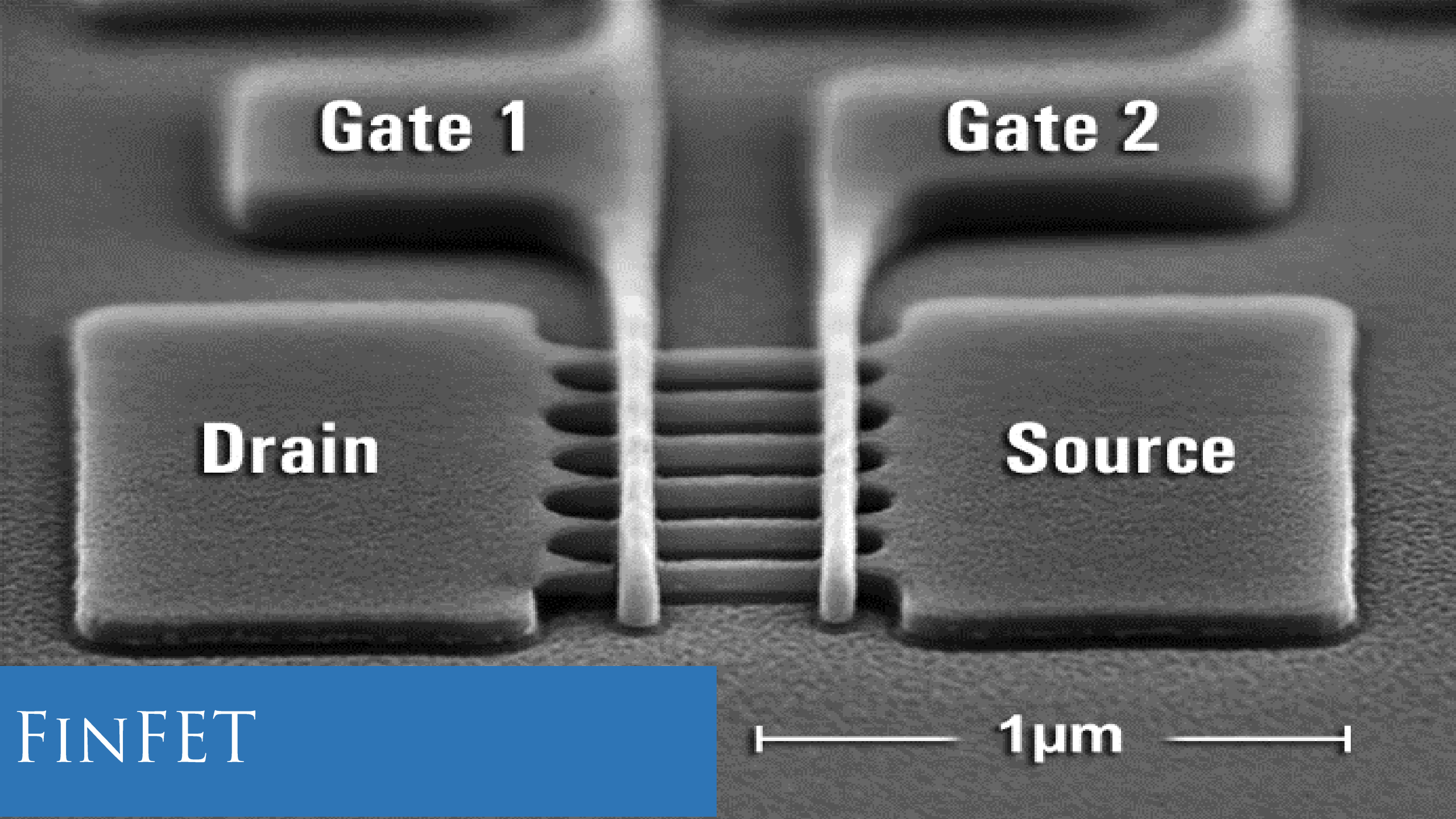

UTB SOI




Planar Double Gate SOI

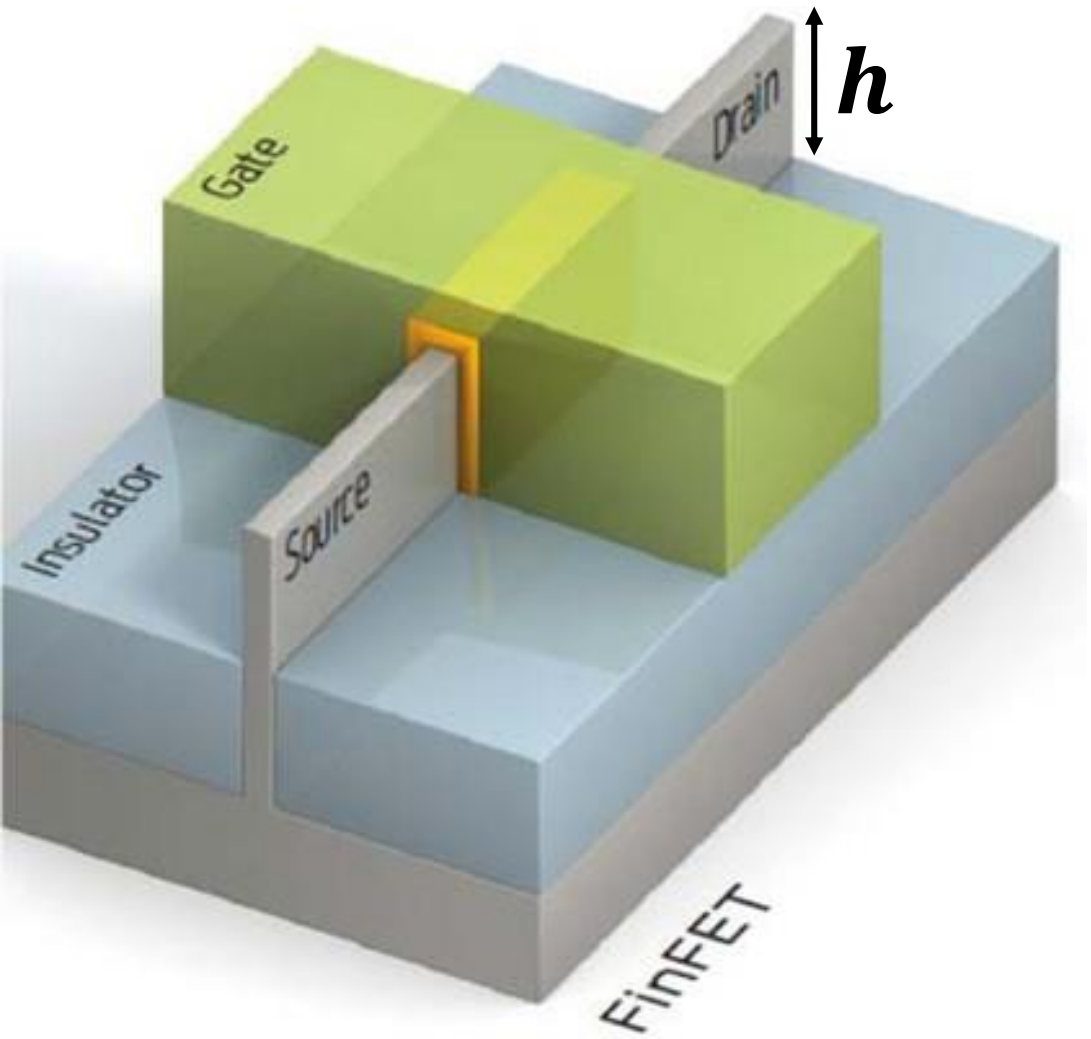


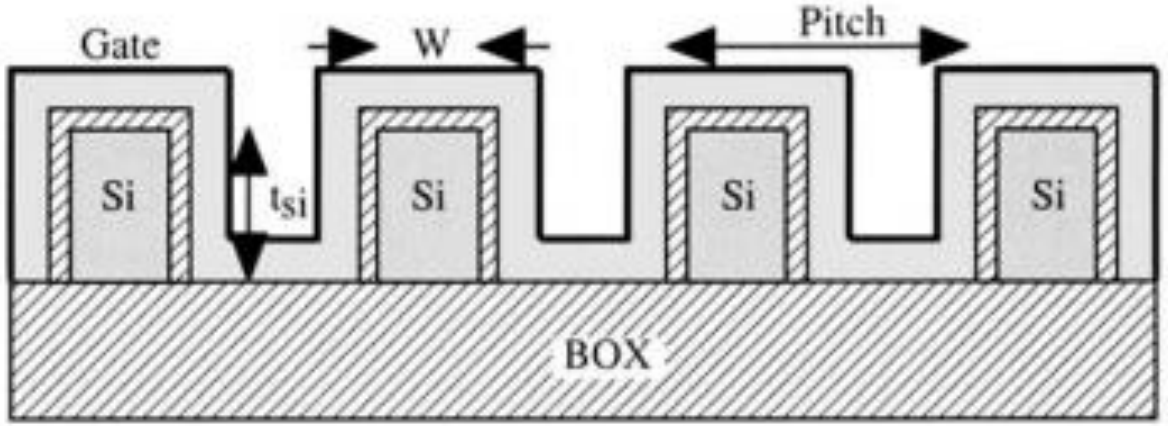

FinFET



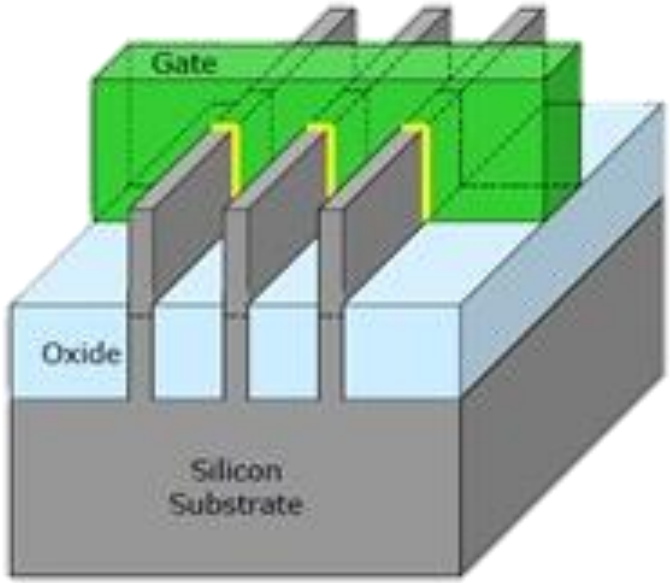

FinFET

# Design Considerations

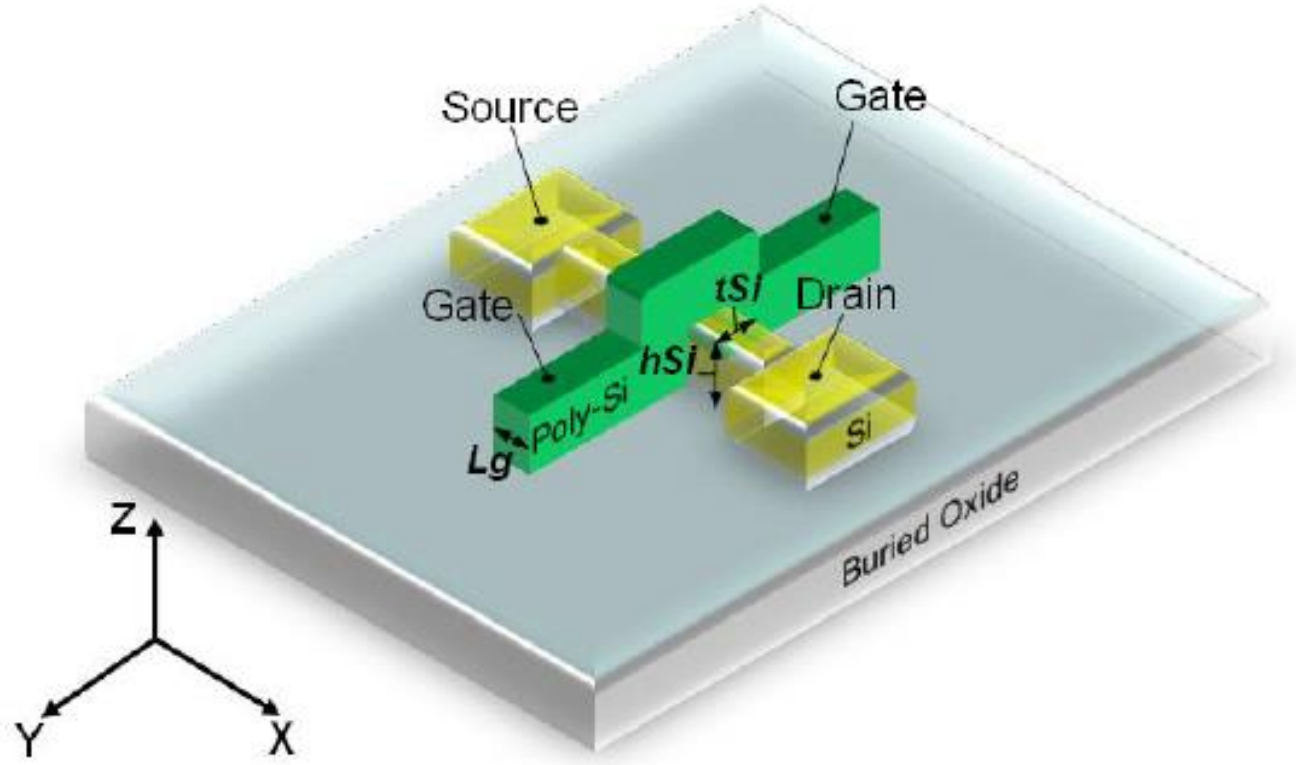


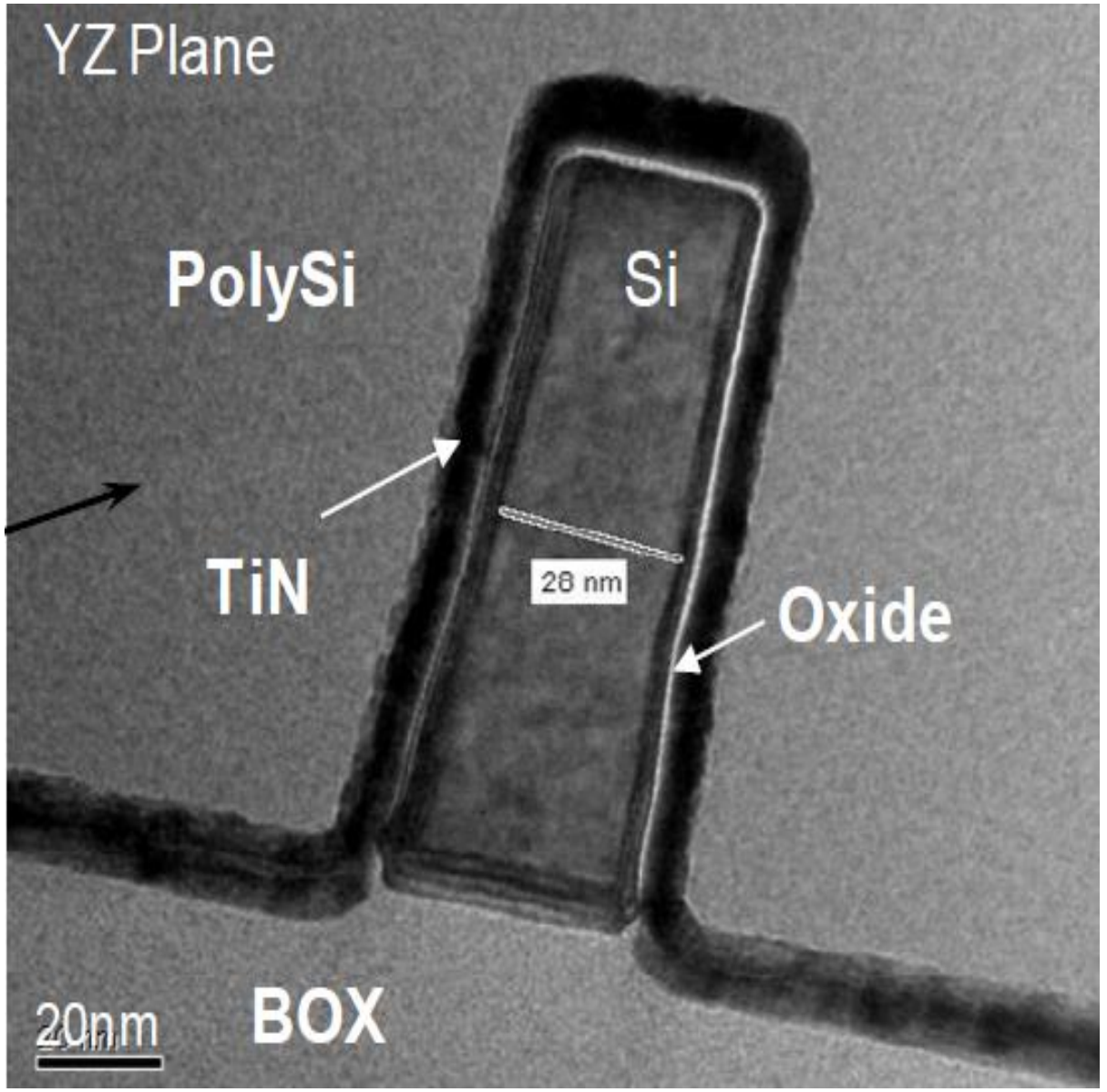




$$Active\ Gate\ Region = 2hn$$

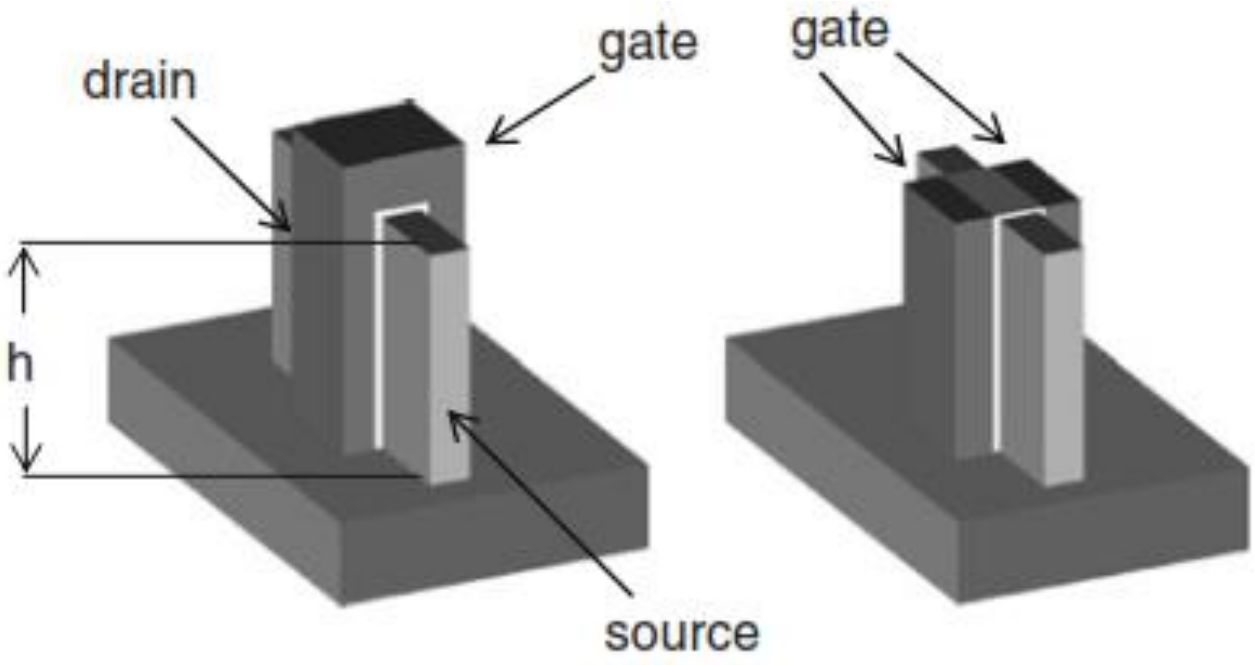


# Un-doped Channel



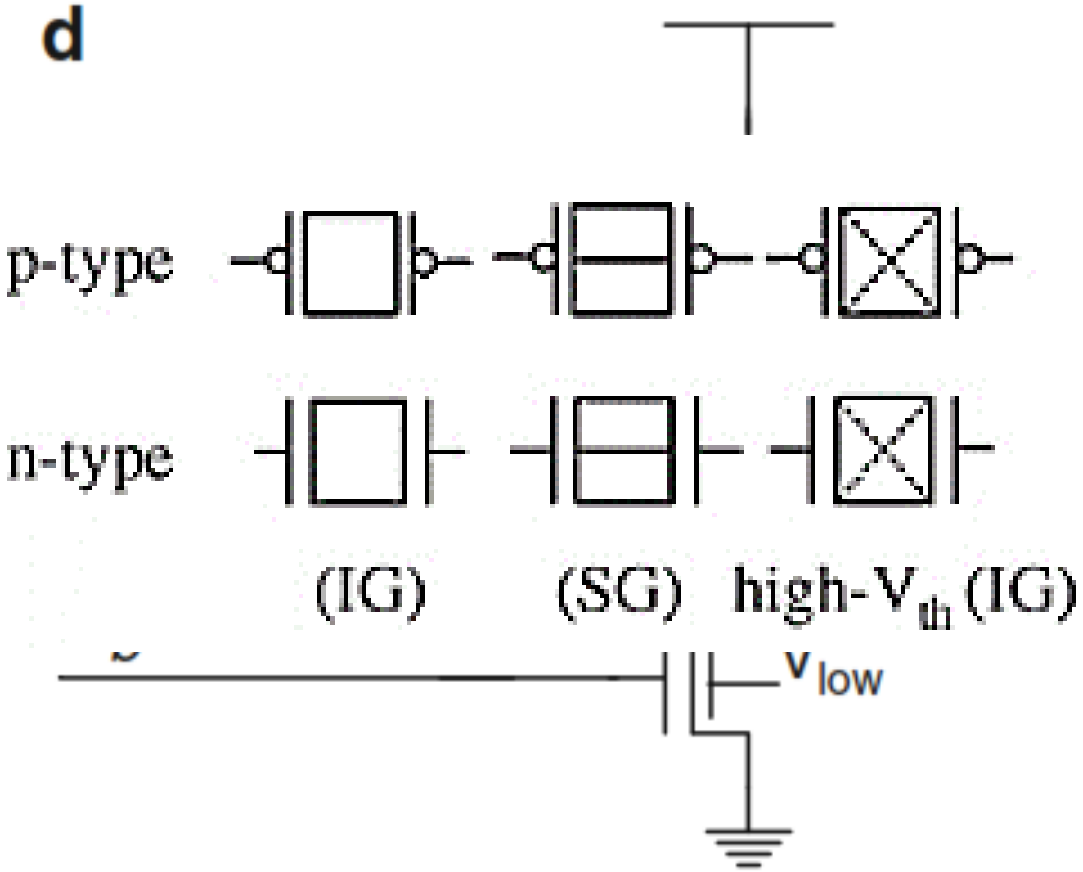



# Configurations

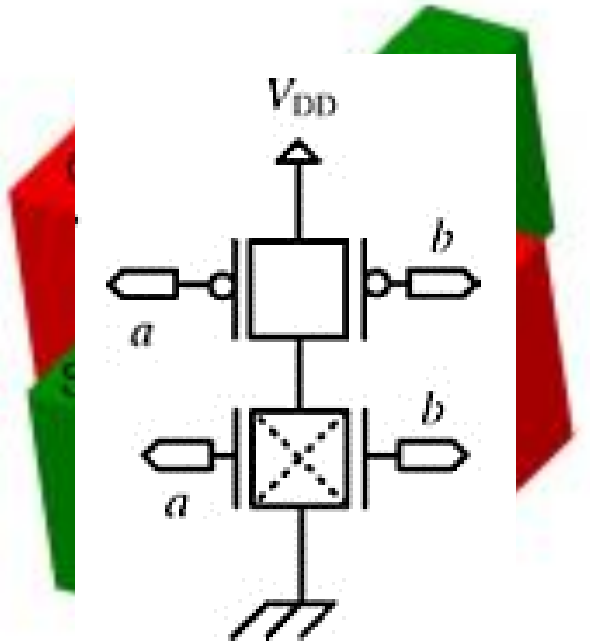



- Shorted Gate
- Independent Gate
  - Low Power

# Logic Design



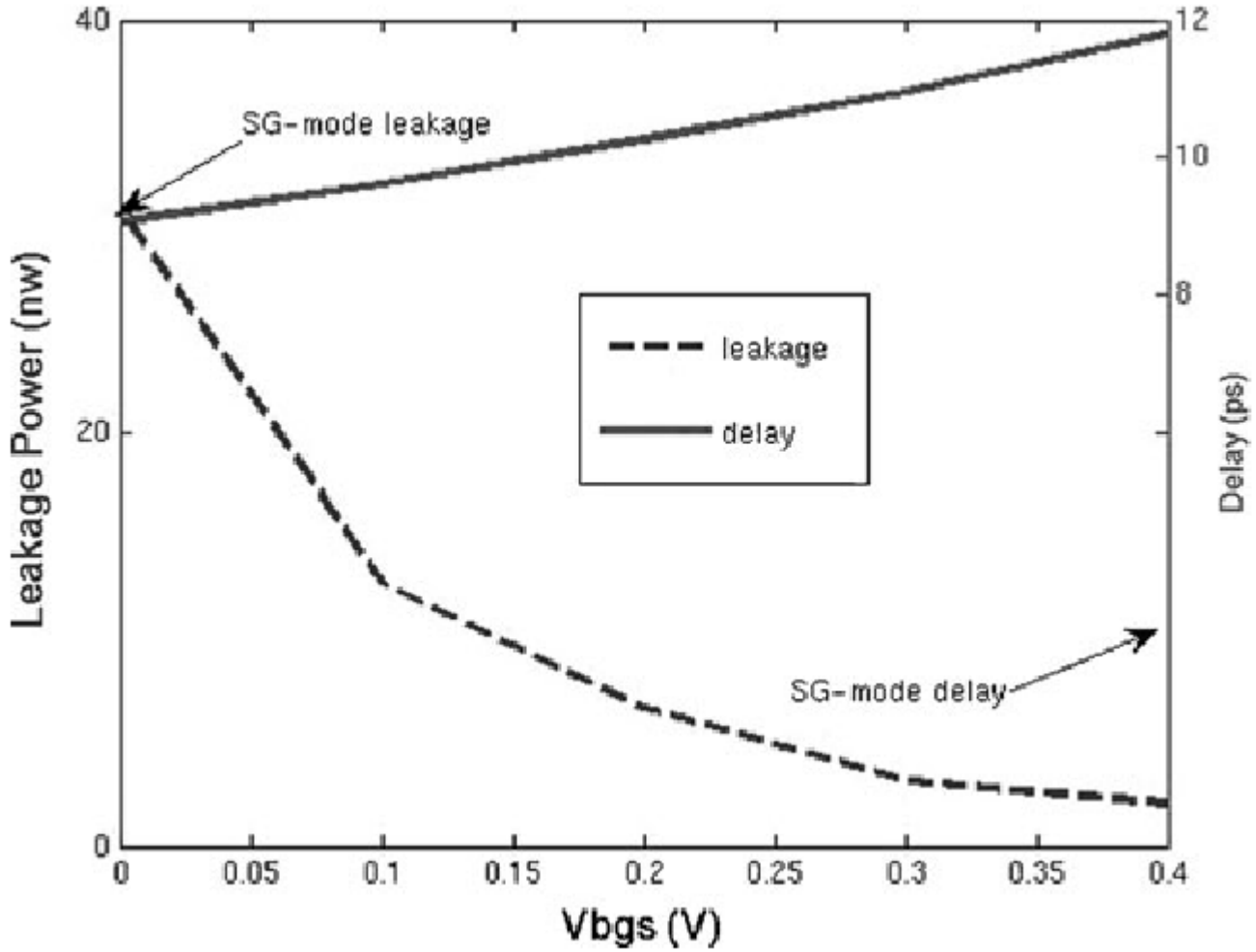

IG/LP-mode NAND



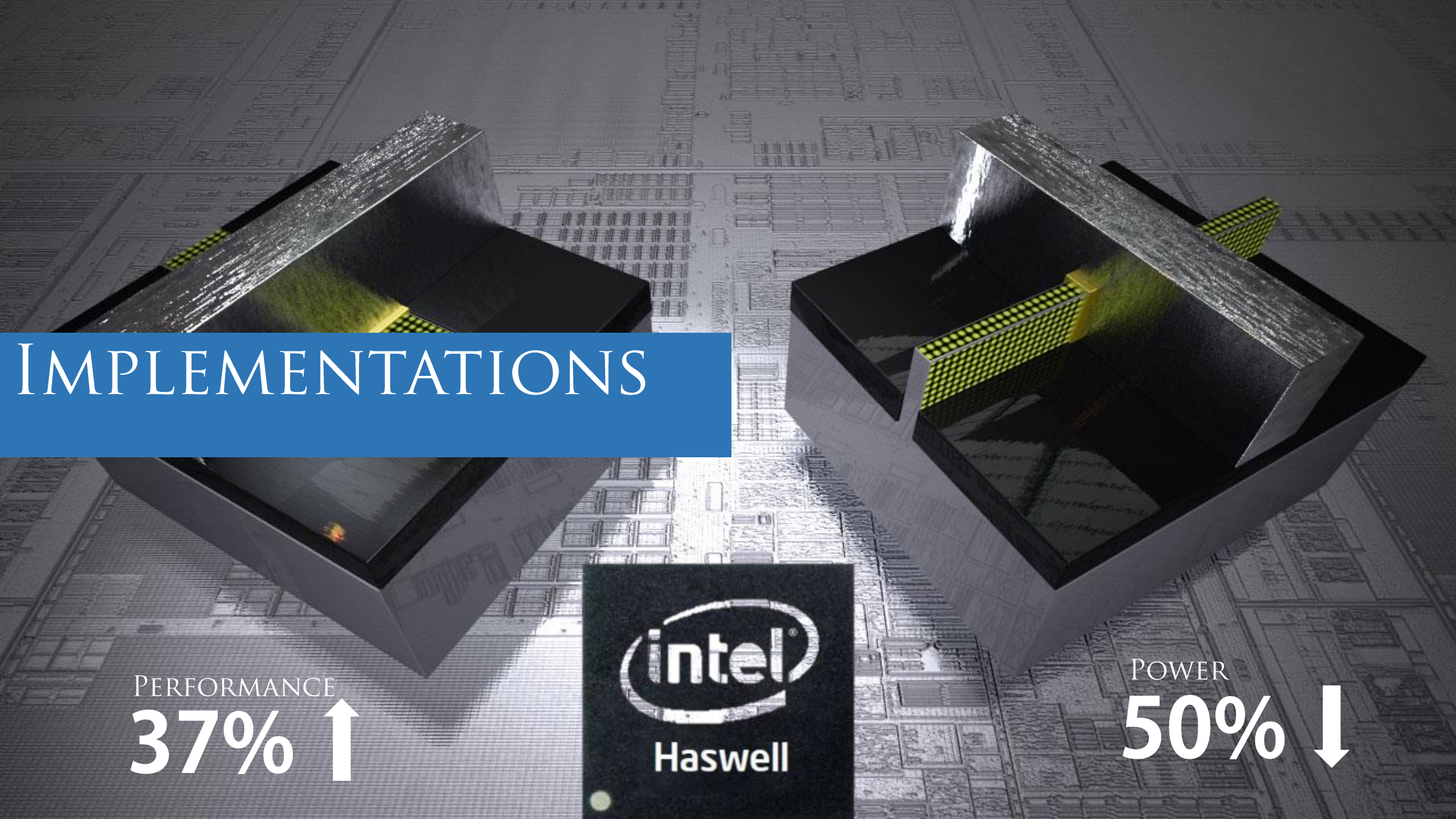

NAND2pdpu

Fin Width

# TCMS $I_{sub}$


SG-mode leakage
SG-mode delay
leakage
delay
Leakage Power (nw)
Delay (ps)
Vbgs (V)
0
20
40
0
0.05
0.1
0.15
0.2
0.25
0.3
0.35
0.4
8
10
12

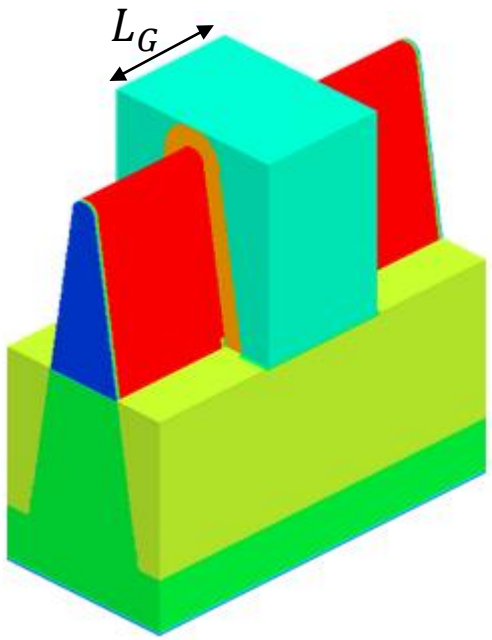
# Implementations

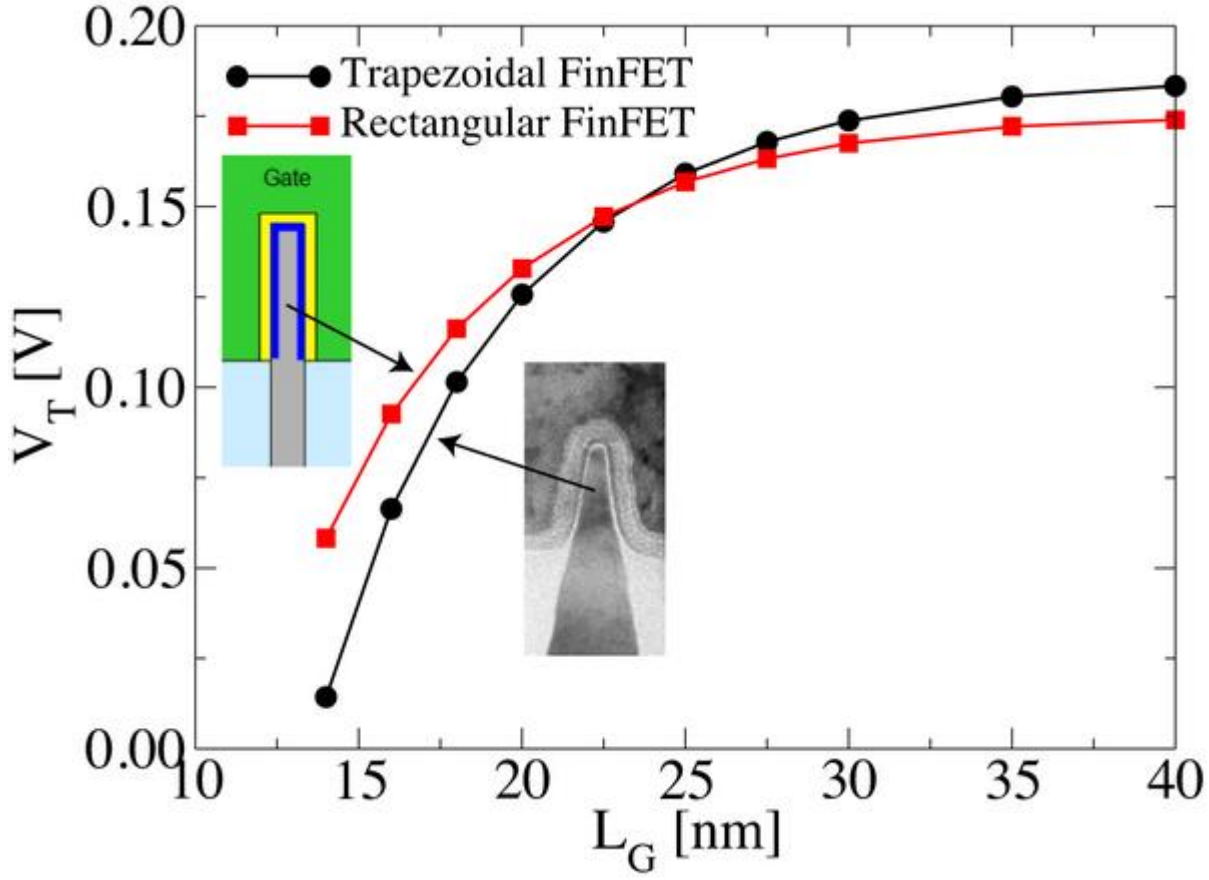


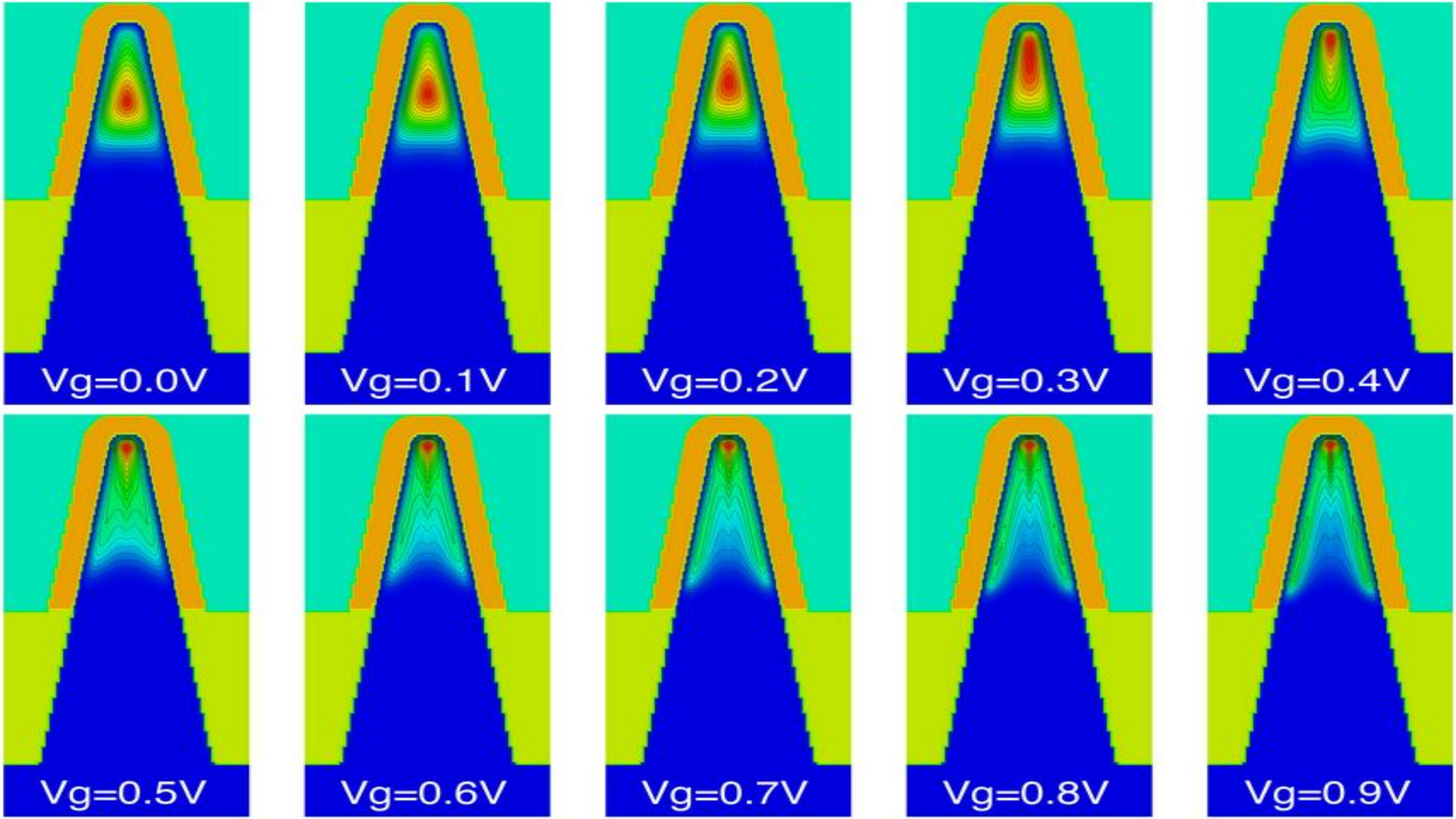

Performance
37% ↑

Power
50% ↓

# Intel Trapezoidal FinFET



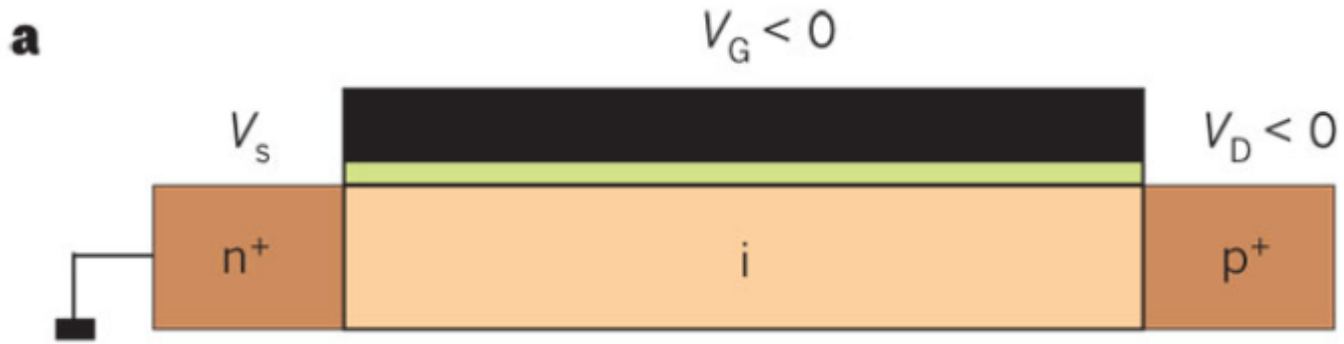

Vg=0.0V
Vg=0.1V
Vg=0.2V
Vg=0.3V
Vg=0.4V
Vg=0.5V
Vg=0.6V
Vg=0.7V
Vg=0.8V
Vg=0.9V

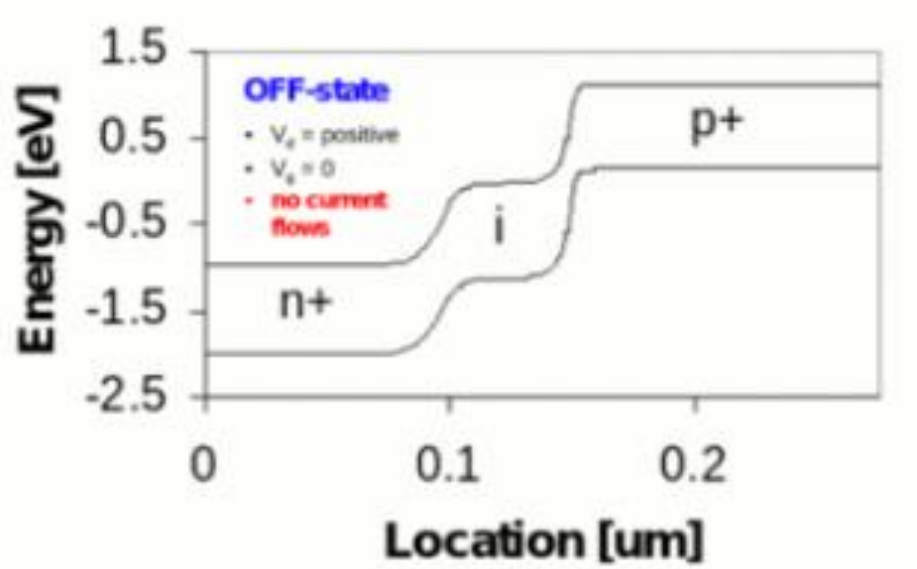
# Questions?

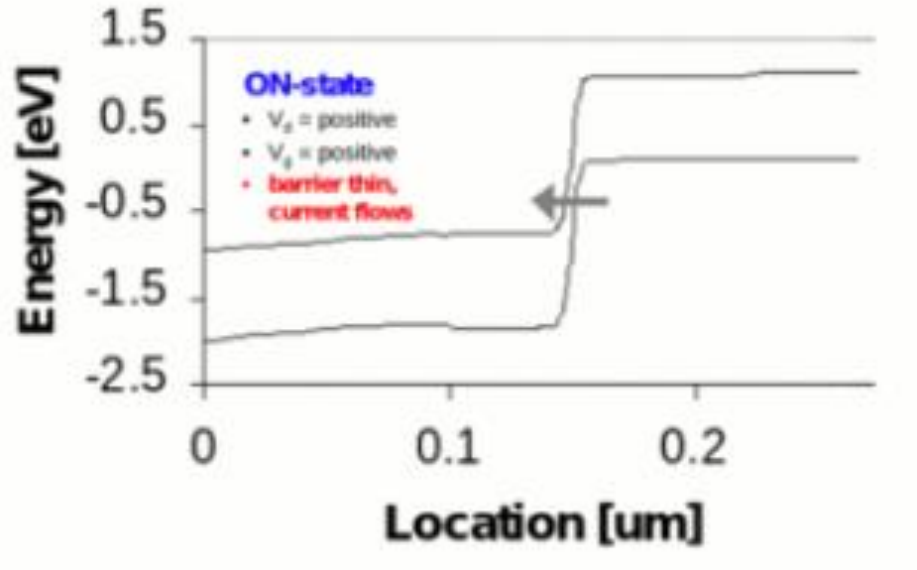
# References


1) M.G. Khazhinsky, M.M. Chowdhury, D. Tekleab, L. Matthew, and J.W. Miller, IEEE IRPS, 262 (2008).
2) P. Mishra, A. Muttreja, and N.K. Jha, *FinFET Circuit Design* (Springer, New York, 2011).
3) M. Rostami, K. Mohanram, IEEE Trans. Comput.-Aided Design Integr. Circuits Syst. **30**, 3 (2011).
4) C. Shin, X. Sun, T.-J. King Liu, IEEE Trans. Elecron Devices **56**, 7 (2009).
5) Y.-K. Choi, K. Asano, N. Lindert, V. Subramanian, T.-J. King, J. Bokor, and C. Hu, IEEE Electron Device Lett. **21**, 5 (2000).
6) http://intel.ly/167QQ9y

# Future: TFET


a
$V_G < 0$
$V_S$
$V_D < 0$
n+
i
p+


OFF-state
• $V_d$ = positive
• $V_g$ = 0
• no current flows
p+
i
n+
Energy [eV]
1.5
0.5
-0.5
-1.5
-2.5
0
0.1
0.2
Location [um]


ON-state
• $V_d$ = positive
• $V_g$ = positive
• barrier thin, current flows
Energy [eV]
1.5
0.5
-0.5
-1.5
-2.5
0
0.1
0.2
Location [um]

# Future: GFET