Digital Integrated Circuits – EECS 312

http://ziyang.eecs.umich.edu/~dickrp/eecs312/

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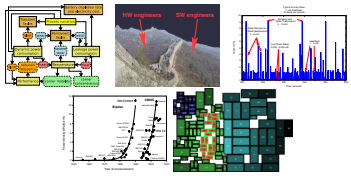

Misc.

- EECS 427.
- Missing name on Lab 4.
- Last new concept: generalized sizing.

Review

- What role do sense amplifiers play for
  - SRAM?
  - 3T DRAM?
  - 1T DRAM?
- What happens if we take a DRAM chip and CPU, and scramble the address lines?

Derive and explain.

Review of inverter chain sizing derivation

- For each i, find ${}^{\sigma t_{p,chain}}/_{\sigma C_{g,i}}$.
- Solve for ${}^{\sigma t_{p,chain}}/_{\sigma C_{g,i}} = 0, \forall_{i=1} N$.
- Result is $\frac{C_{g,i+1}}{C_{g,i}} = \frac{C_{g,i}}{C_{g,i-1}}$.
- Each stage size geometric mean of previous and next: $C_{g,i} = \sqrt{C_{g,i-1} C_{g,i+1}}$.
- Constant factor relates sizing of all adjacent gate pairs.
- Each stage has same delay.

Can this concept be generalized to more complex logic networks?

- Logical effort.
- Will introduce (enough to use) in EECS 312.
- More depth and general coverage in EECS 427.
- Do *not* read the textbook on this particular topic.

Logical effort

Expectations
- Definitions.
- Ability to use.

Coverage
- Definitions.
- Ability to use.
- Intuition.
- Proof of correctness.

Motivation and key concepts

- Multiplicative tapering works for inverter chains, but what happens for more complex circuits?
- Multi-input gates?
  - Stage logical effort.
- Fan-out?
  - Stage branching effort.

Definitions

- g_i: Gate logical effort. Ratio of input capacitor to equal on-resistance inverter.
- $G = \prod_{i=1}^{n} g_i$: Path logical effort.
- $H = \frac{C_{out}}{C_{in}}$: Path electrical effort.
- $b = \frac{C_{total}}{C_{useful}}$: Stage branching effort.
- $B = \prod_{i=1}^{n} b_i$: Path branching effort.
- $F = GBH$: Path effort.
- $\hat{f} = g_i h_i = \sqrt[n]{F}$: Optimal stage effort.
- $\hat{h}_i = \frac{\hat{f}}{g_i} = \frac{C_{i,out}}{C_{i,in}}$: Optimal stage electrical effort.
- $D_i = G_i h_i + p_i$: Stage delay.

Examples

- Simple chain.
- Tree.
- Reconverging paths.
- Optimal number of stages $\approx \log_4 F$.

Intuition

- Will post detailed written notes and examples to website.
- May not need to use, but may want to refer back to this in later courses, e.g., EECS 427.

Homework, deadlines, and schedule

- 9 December, Thursday: Wrap-up and review. Second midterm returned.
- 10 December, Friday: Wrap-up and review that Mr. Kim and I will both attend. Class standing email. Final practice assignment.
- 20 December, Monday: Final exam.

Special topics

Resonant tunneling devices

Baishun, Bo Zhu, and Terence

Memristors

Austin