Digital Integrated Circuits – EECS 312

http://ziyang.eecs.umich.edu/~dickrp/eecs312/

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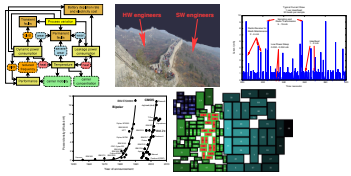


Review

- What are the different ways a floating-gate memory cell can be erased?
- What are the different ways a floating-gate memory cell can be programmed?
- What are the two main DRAM bit cell organizations, and their advantages?
- Why is it difficult to economically put DRAM on the same die as a processor?
- Why are decoders and MUXs used in memory arrays?

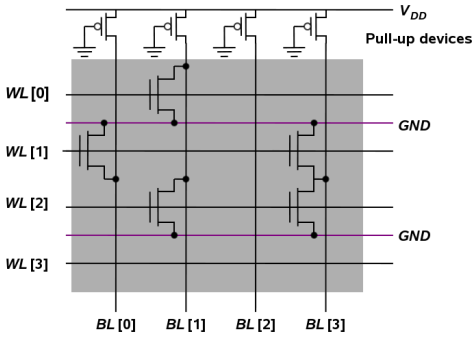
Derive and explain.

Final project building blocks

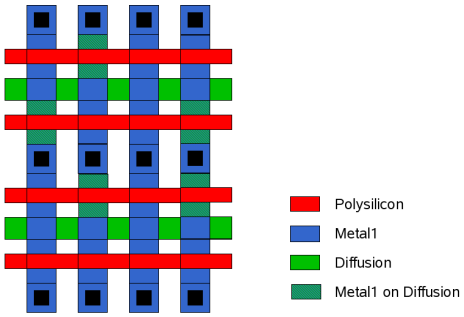
- D latch: TG and with sized feedback path.
- D flip-flop: two-stage.
- Counters.

Derive and explain.

NOR ROM schematic

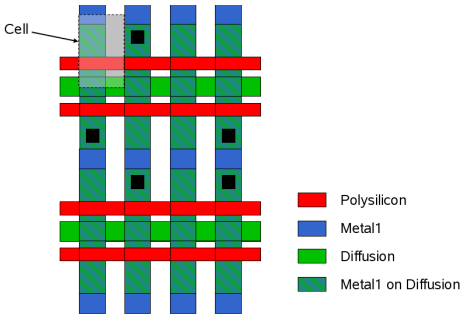


NOR ROM layout



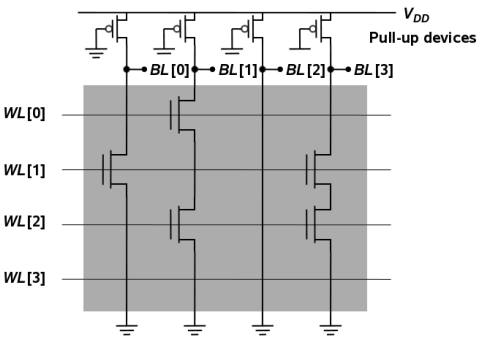
Program using active layer.

NOR ROM layout

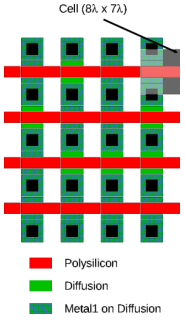


Program using contacts.

NAND ROM schematic

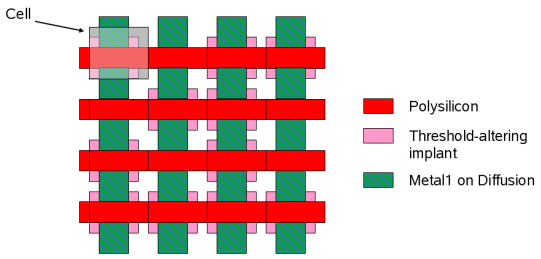


NAND ROM layout



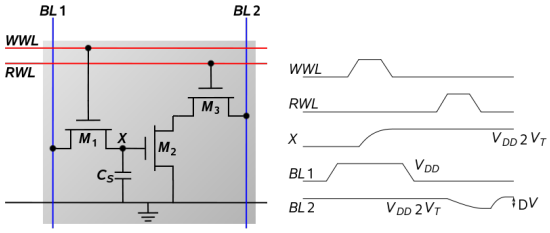
Program using metal layer.

NAND ROM layout

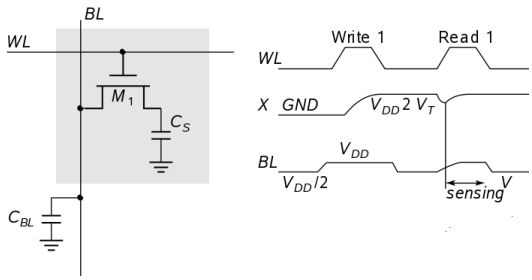


Program using implants.

DRAM

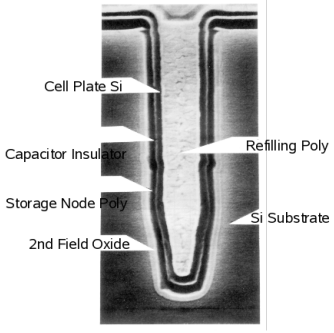


DRAM

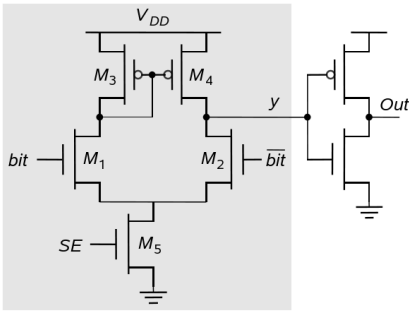


Write: C_S is charged or discharged by asserting WL and BL.

DRAM side view

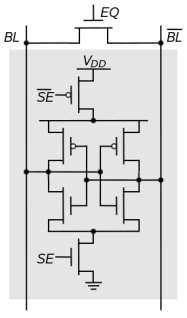


Differential sense amplifier



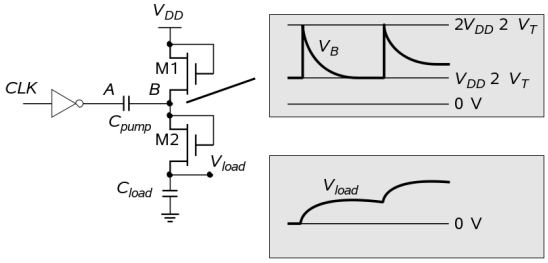
Useful for SRAM, can use two stages.

Latch sense amplifier



Useful for DRAM.

Charge pump



Homework, deadlines, and schedule

- 2 December, Thursday: Midterm exam.
- 7 December, Tuesday: Logical effort.
- 9 December, Thursday: Wrap-up and review.
- 10 December, Friday: Final project due (will post on 24 November).
- Any time: Review homework problems will be marked, but not graded (will post by 10 December).
- 20 December, Monday: Final exam.

Special topic: Novel materials in digital integrated circuits

Jiayi, Heesung, and Michael.