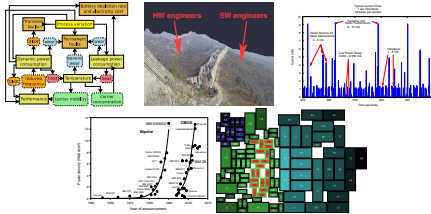


Digital Integrated Circuits – EECS 312

<http://robertdick.org/eeecs312/>

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Review

- What are the historical motivations that have driven changes in digital device implementation technologies?
- What is the difference between a combinational and sequential network?
- What substrates (device types) have been used for computation?
- What are the primary advantages of integrated circuits over these competing technologies?

Remember the ENIAC?

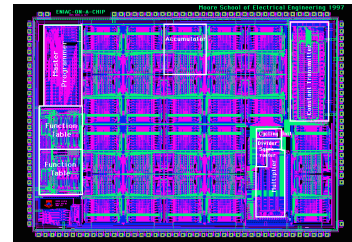
- 1946.
- 18,000 vacuum tubes.
- 30 tons.
- 100 kHz.
- Unreliable.



What impact would ICs have on it?

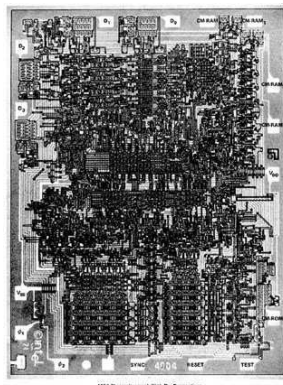
IC ENIAC

- 30 tons → 40 mm².
- 100 kHz → 20 MHz.
- Unreliable.



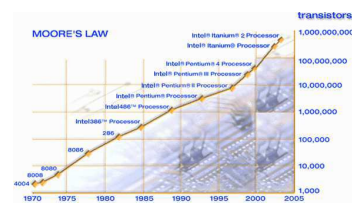
First microprocessor

- Intel 4004.
- 1971.
- 2,300 transistors.
- 12 mm².
- 740 kHz.
- 12-bit addresses, 8-bit instructions, 4-bit data words.



Trend for one company

- More than ten generations.
- Datapath: 4 bits → 64 bits.
- Frequency: 740 KHz → 3 GHz.
- In-order, cache-less → Architectural features for common-case performance.
- Uni-processor → Chip-multiprocessor (CMP).
- A few thousand transistors → Billions of transistors.

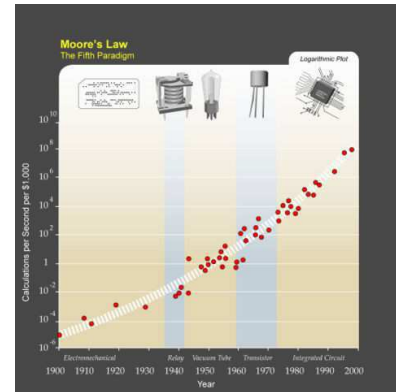


Moore's law

- 1965.
- The number of transistors in an IC doubles every 18–24 months.

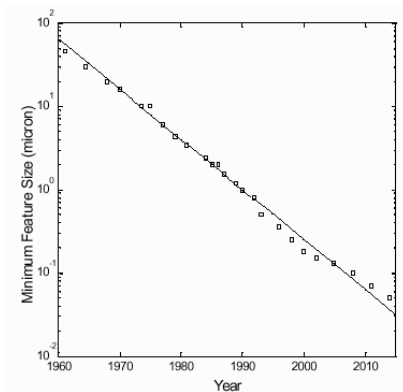
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Actual trend



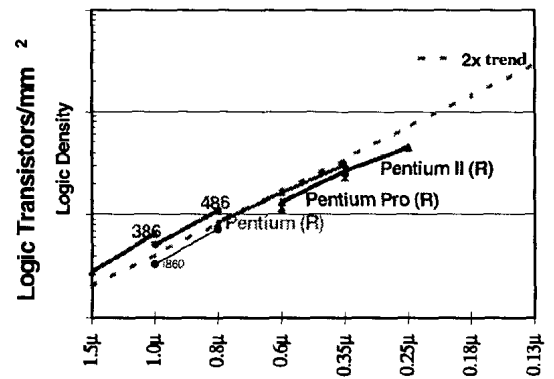
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Feature size trends



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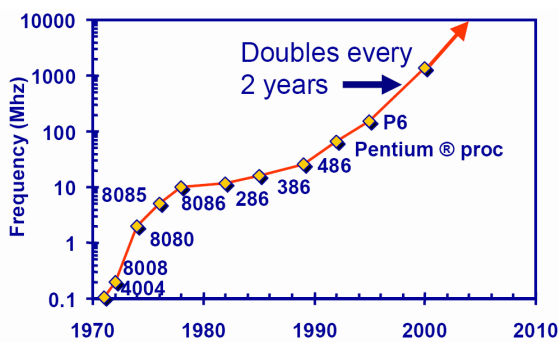
Logic density trends



11

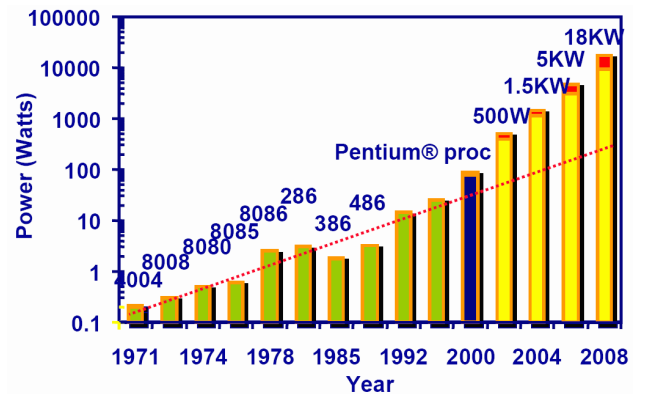
Frequency trends

- Technology scaling \downarrow delay by 30% and \uparrow frequency by 43%.
- Frequency $\propto 1/\text{Delay}$.



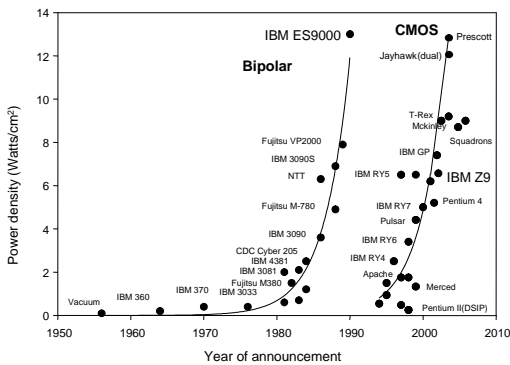
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Power trends



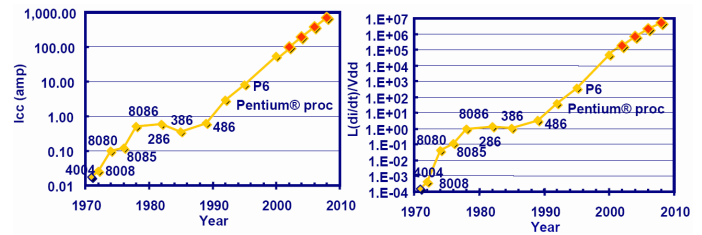
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Power density trends



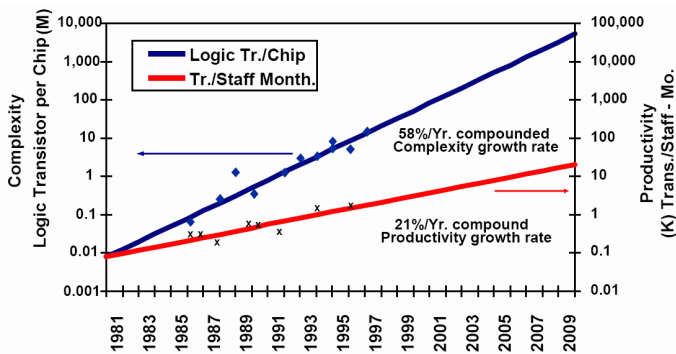
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Power supply trends



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Productivity trends



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Impact of power consumption and temperature

- Early ICs used bipolar transistors (BJT).
- Easier to manufacture reliably, faster.
- In the 1970s, integration densities rose.
- Each bipolar device consumes a lot of power.
- Eventually power became the limiting factor in moving from BJT to MOS devices.
- Currently CMOS dominates.
- Complementary MOS logic.
- Likely to dominate for the next decade.

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Power consumption trends

- Initial optimization at transistor level.
- Further research-driven gains at this level difficult.
- Research moved to higher levels, e.g., RTL.
- Trade area for performance and performance for power.
- Clock frequency gains linear.
- Voltage scaling V_{DD}^2 – important.

Power consumption in synchronous CMOS

$$P = P_{SWITCH} + P_{SHORT} + P_{LEAK}$$

$$P_{SWITCH} = C \cdot V_{DD}^2 \cdot f \cdot A$$

$$\dagger P_{SHORT} = \frac{b}{12} (V_{DD} - 2 \cdot V_T)^3 \cdot f \cdot A \cdot t$$

$$P_{LEAK} = V_{DD} \cdot (I_{SUB} + I_{GATE} + I_{JUNCTION} + I_{GIDL})$$

C : total switched capacitance V_{DD} : high voltage
 f : switching frequency A : switching activity
 b : MOS transistor gain V_T : threshold voltage
 t : rise/fall time of inputs

$$\dagger P_{SHORT} \text{ usually } \leq 10\% \text{ of } P_{SWITCH}$$

Smaller as $V_{DD} \rightarrow V_T$
 $A < 0.5$ for combinational nodes, 1 for clocked nodes.

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Wiring power consumption

- In the past, transistor power \gg wiring power.
- Process scaling \Rightarrow ratio changing.

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Other (related) design trends

- Smaller transistors.
- Bigger chips (die).
- Lower power consumption.
- Higher clock frequencies.
- More complex designs.
- Lower voltage.

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Other (related) design trends

- Smaller transistors.
- Bigger chips (die).
- Lower power consumption.
- Higher clock frequencies.
- More complex designs.
- Lower voltage.
- More cores.

Some of these trends are slowing.

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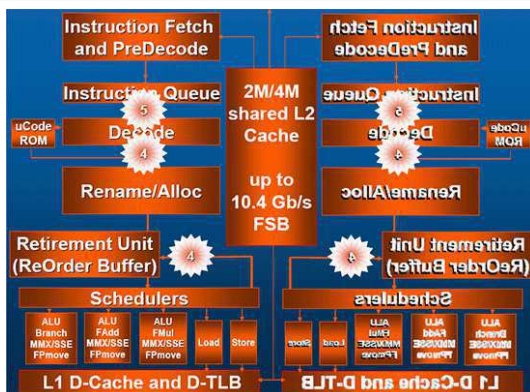
Current status

- Feature size: 22 nm.
- Integration: 700,000,000 transistors.
- Frequency: 2-4 GHz.
- Power: 100 W.

Only two of these characteristics have changes in the past few years.

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Multi-core processors



Intel Core 2 Duo

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Summary of recent IC history

- Process scaling improves device count, speed.
- Power density increases, eventually limiting further improvements.
- Current move to multi-core.
- Also considering new device technologies, but no clear winners now.

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Levels of abstraction

- Hardware–software system.
- Processor.
- Functional unit.
- Logic stage: flip-flop or combinational logic network.
- Gate.
- Transistor or wire.
- Physical material or doping regions.

Derive and explain.

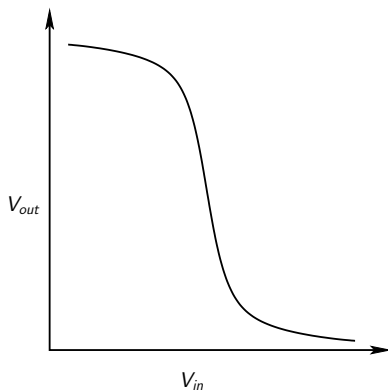
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What properties must a “digital” device have?

- What allows us to treat a device as digital, and still have the system work?
- Does this imply certain properties for the transfer function?

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Transfer function



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Completeness

- Technology should support implementation of arbitrary Boolean functions.
- Consider {AND2, OR2} and {NAND2}.

Derive and explain.

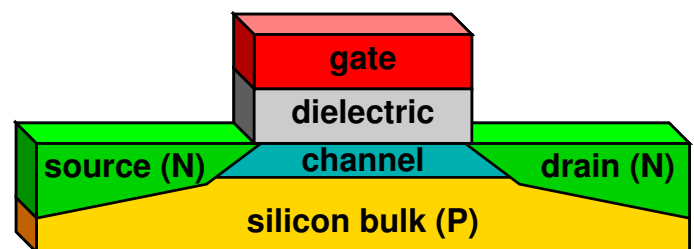
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CMOS

- Metal Oxide Semiconductor
- Positive and negative carriers
- Complimentary MOS
- PMOS gates are like normally closed switches that are good at transmitting only true (high) signals
- NMOS gates are like normally open switches that are good at transmitting only false (low) signals

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NMOSFET



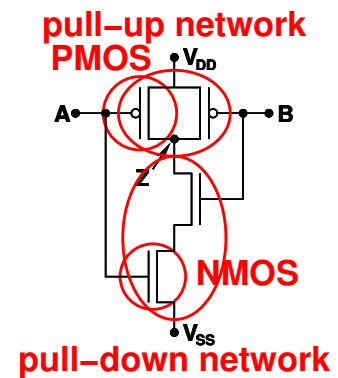
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CMOS

- NMOS turns on when the gate is high
- PMOS just like NMOS, with N and P regions swapped
- PMOS turns on when the gate is low
- NMOS good at conducting low (0s)
- PMOS good at conducting high (1s)
- Use NMOS and PMOS transistors together to build circuits
 - Complementary metal oxide semiconductor (CMOS)

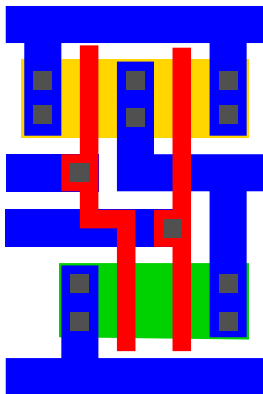
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CMOS NAND gate



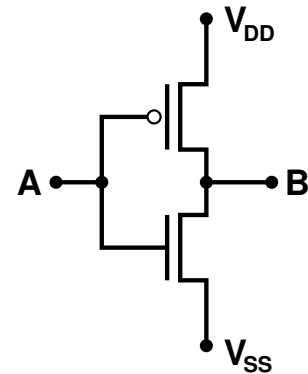
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What is this?



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What is this? How would we lay it out?



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Non-Credit quiz on material covered so far

- History of integrated circuits.
 - What happens as a result of process scaling?
 - What have the motivations for major changes in device technology been?
 - What is a digital system?
 - What is a general-purpose computer?
 - What is an embedded system?
 - What is an integrated circuit?
 - What is an ASIC?
 - What is an instruction processor?
 - What is an FPGA?
- What gate properties support use in digital systems?
 - What properties should $V_{out}-V_{in}$ curve have?
 - Describe completeness.

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Upcoming topics

Enough overview: time to start building!

- Diodes
- Transistor static behavior
- Transistor dynamic behavior

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Lab one challenges

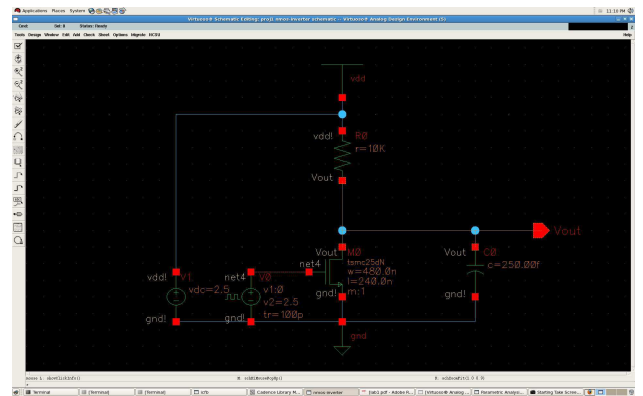
- Learning to use the tools (Friday).
- Understanding the circuits used in the lab (Tuesday).
- A note on the CAD tools market.

Derive and explain.

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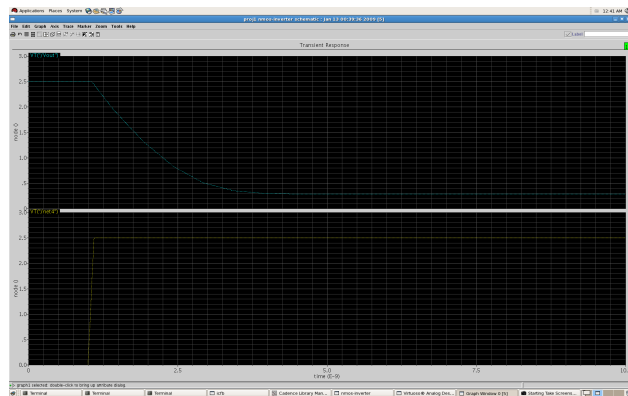
NMOS inverter schematic



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NMOS inverter simulation results



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Upcoming topics

- 6 September: Discussion in room 1620 BBB will focus on Lab 1.
- 10 September: MOSFETs.

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Homework assignment and announcement

- 5 September: Email topics of interest.
- 10 September: Read Sections 3.1, 3.2, and 3.3.1 in J. Rabaey, A. Chandrakasan, and B. Nikolic. *Digital Integrated Circuits: A Design Perspective*. Prentice-Hall, second edition, 2003.
- 17 September: Laboratory assignment one.

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