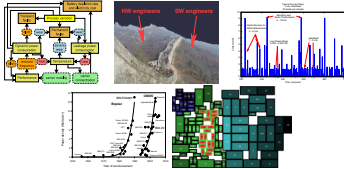


Digital Integrated Circuits – EECS 312

<http://ziyang.eecs.umich.edu/~dickrp/eecs312/>

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Memory array structures
Dynamic random access memory
Homework

Distributed loads and Elmore delay

Derive the propagation delay of an aluminum wire that is 2 cm long and 500 nm wide. Does using a lumped model introduce significant error? You may assume a sheet resistance of $0.075 \Omega/\square$. Derive the propagation delay of a copper wire with the same shape. State, and verify, any assumptions.

Derive and explain.

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Memory array structures
Dynamic random access memory
Homework

Volatile memory

- SRAM cell and architecture overview.
- DRAM cell and architecture overview.

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Memory array structures
Dynamic random access memory
Homework

Floating gate technology

- UV erase.
- Electrical erase.
- Block erase.

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Memory array structures
Dynamic random access memory
Homework

Review

- What are t_{su} and t_h ?
- Define
 - Level-sensitive.
 - Edge-triggered.
 - Latch.
 - Flip-flop.
- What is the symbol for a falling edge triggered D flip-flop?
- Show a circuit design for a Schmitt-trigger inverter.

Derive and explain.

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Memory array structures
Dynamic random access memory
Homework

More on transistor sizing

$$f(a, b, c) = \overline{ab + c}$$

Derive and explain.

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Memory array structures
Dynamic random access memory
Homework

Non-volatile memory

- ROM.
- EPROM.
- EEPROM.
- Flash.

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Memory array structures
Dynamic random access memory
Homework

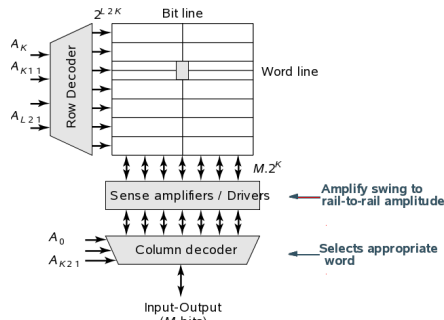
Hot floating gate implementation

- Was once difficult to design uniform-thickness thin oxide layers.
- Tunneling-based programming was difficult.
- Avalanche injection (hot electron) based programming used.
- UV erasure.
- Pure tunneling later became practical (EEPROM).
- Flash uses hot electrons for programming and tunneling for erasing.

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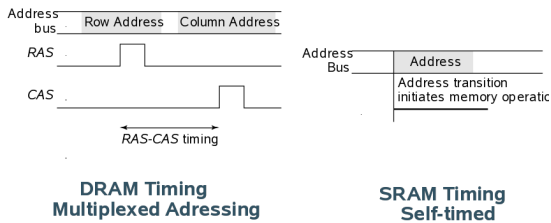
Memory array structures
Dynamic random access memory
Homework

Array memory architecture



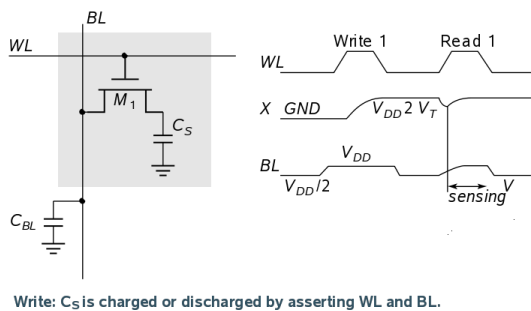
Memory array structures
Dynamic random access memory
Homework

Memory timing



Memory array structures
Dynamic random access memory
Homework

DRAM



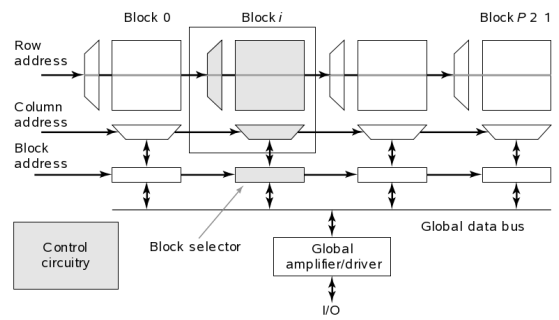
Memory array structures
Dynamic random access memory
Homework

Upcoming topics

- Sequential circuits.

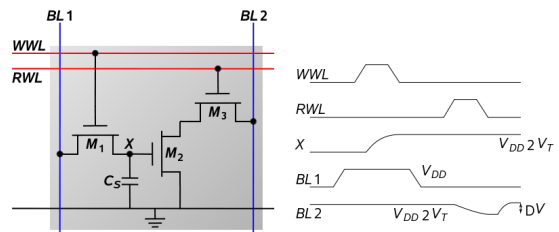
Memory array structures
Dynamic random access memory
Homework

Block-based memory architecture



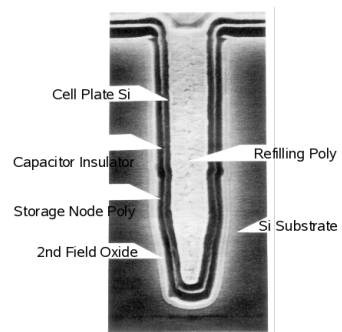
Memory array structures
Dynamic random access memory
Homework

DRAM



Memory array structures
Dynamic random access memory
Homework

DRAM side view



Memory array structures
Dynamic random access memory
Homework

Homework, deadlines, and schedule

- 25 November, Thursday: Office hours from 3:00–4:30. Call-ins and skype-ins welcome.
- 30 November, Tuesday: Read Section 12.2 in J. Rabaey, A. Chandrakasan, and B. Nikolic. *Digital Integrated Circuits: A Design Perspective*. Prentice-Hall, second edition, 2003.
- 2 December, Thursday: Midterm exam.
- 10 December, Friday: Final project due (will post on 24 November).
- Any time: Review homework problems will be marked, but not graded (will post by 10 December).

Special topic: Optical interconnect

Guanyu and Haishan.