Digital Integrated Circuits – EECS 312

http://ziyang.eecs.umich.edu/~dickrp/eecs312/

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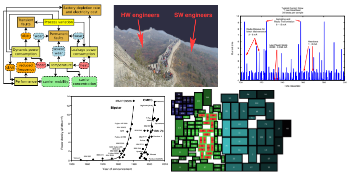


Travel

- Where were your teacher and teaching assistant?
- International Conference on Computer-Aided Design.
- Mr. Kim won the best-paper award at this top conference.
- I gave a tutorial on integrated circuit and embedded system reliability.
- My student gave a talk on dynamic control of V_{DD} to minimize energy consumption while meeting performance requirements.
- If curious, you can out about the research on the course website, at the "Excuse for absence" link.

Midterm exam 2

- Requested times for midterm exam.
- 30 November or 2 December.
- Received two replies that conflict.
- Coin flip.

Homework 3

- Was anybody unable to get help they needed on Homework 3?
- If so will not penalize assignments handed in by Friday.
- However, Lab 4 will be assigned today.

Lab 4

Derive and explain.

Review

- What is the purpose of a restorer in pass transistor logic?
- What happens if the restorer MOSFET is too wide?
- What happens if the restorer MOSFET is too narrow?
- What are the advantages of dynamic logic?
- What are the disadvantages of dynamic logic?

Examples

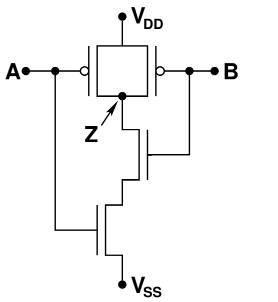
- $f(a) = a$.
- $f(a) = \overline{a}$
- $f(a, b) = a\overline{b}$
- $f(a, b) = ab$ (Check Figure 6-33 in J. Rabaey, A. Chandrakasan, and B. Nikolic. *Digital Integrated Circuits: A Design Perspective*. Prentice-Hall, second edition, 2003!)
- $f(a, b, c) = ab + \overline{b}c$ (try both ways).

Derive and explain.

Miller effect

- If V_D switches in the opposite direction of V_G, the effect of C_{GD} is doubled.
- Consider an inverter.
- Model by using a $2C_{GD}$ capacitor to ground.

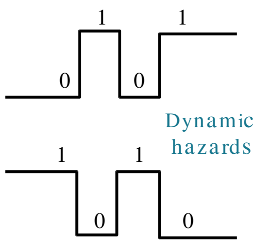
Stack effect



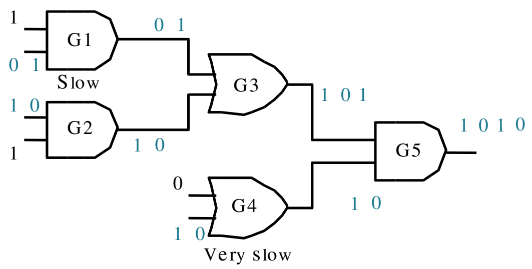
- Each series transistor drops the voltage seen by the next transistor.
- $V_T = T_{T0} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right)$
- $V_{Tn2} = V_{Tn0} + \gamma\left(\sqrt{|2\phi_F + V_{int}|} - \sqrt{|2\phi_F|}\right)$

Dynamic hazards

- Potential for two or more spurious transitions before intended transition
- Results from uneven path delays in some multi-level circuits



Dynamic hazards

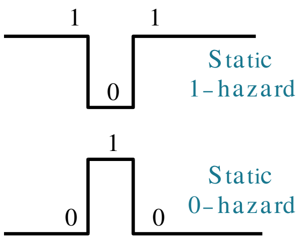


Eliminating dynamic hazards

- Some approaches allow preservation of multi-level structure
  - Quite complicated to apply
- Simpler solution – Convert to two-level implementation

Static hazards

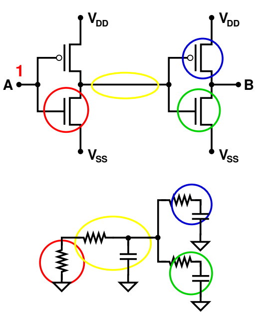
- Still have static hazards
- Potential for transient change of output to incorrect value



Problems with glitches

- These transitions result in incorrect output values at some times
- Also result in uselessly charging and discharging wire and gate capacitances through wire, gate, and channel resistances
  - Increase power consumption

Glitches increase power consumption



Detecting hazards

- The observable effect of a hazard is a glitch
  - A circuit that might exhibit a glitch has a hazard
- Whether or not a hazard is observed as a glitch depends on relative gate delays
- Relative gate delays change depending on a number of factors – Conditions during fabrication, temperature, age, etc.
- Best to use abstract reasoning to determine whether hazards might be observed in practice, under some conditions

Eliminating static hazards

- Ensure that the function has a term maintaining a 0 output for all 0→0 transitions.
- Ensure that the function has a term maintaining a 1 output for all 1→1 transitions.
- There are precisely defined algorithms for this, but they build on a knowledge of logic minimization.

Where do static hazards really come from?

- Static-0: $A\,\overline{A}$
- Static-1: $A + \overline{A}$
- Assume SOP form has no product terms containing a variable in complemented and uncomplemented forms
  - Reasonable assumption, if true, drop product term

Where do static hazards really come from?

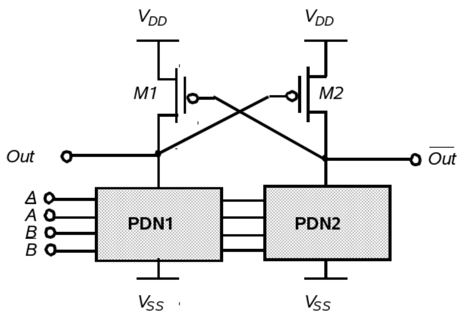
- Assume POS form has no sum terms containing a variable in complemented and uncomplemented forms
  - Reasonable assumption, if true, drop sum term
- Assume only one input switches at a time
- Conclusion: SOP has no 0-hazards and POS has no 1-hazards
  - In other words, if you are doing two-level design, you need not analyze the other form for hazards

Living with hazards

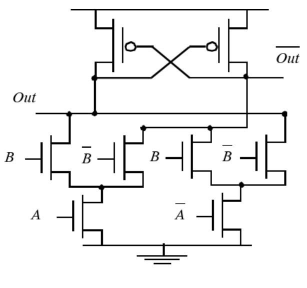
Sometimes hazards can be tolerated

- Combinational logic whose outputs aren't observed at all times
- Synchronous systems
- Systems without tight power consumption limits

Differential cascode voltage switch logic

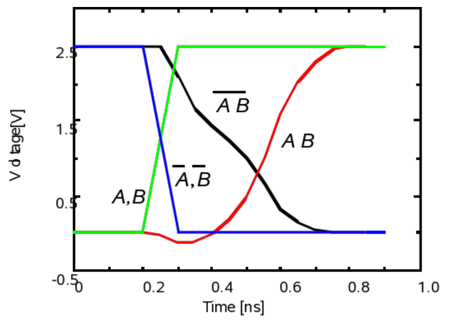


Differential cascode voltage switch logic example



XOR-NXOR gate

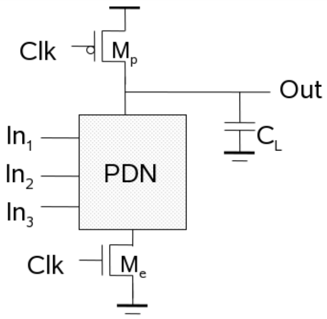
Differential cascode voltage switch logic response



Static vs. dynamic logic

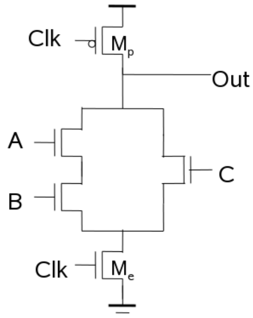
- Static logic relies only on steady-state behavior of system. Eventually the output converges to a correct result.
- Dynamic logic relies on transient behavior and is sensitive to timing. Reliable design is generally trickier. Why use it?
- Static logic requires $(k_P + k_N)$ transistors for k-input gate.
- Dynamic logic requires $k_N + 2$ transistors for k-input gate.

Dynamic logic



Two-phase operation.

Dynamic logic example



Dynamic logic operating principles I

1. Can only discharge output node once per clock period.
2. Inputs must make only one transition during evaluation.
3. Output can be in the high impedance state during and after evaluation.
4. Logic function is implemented by the pull-down network only.
5. Requires only $k_N + 2$ transistors.
6. Full swing outputs.
7. Non-ratioed - sizing of the devices does not affect the logic levels.
8. Reduced load capacitance due to lower input capacitance.
9. Reduced load capacitance due to smaller output loading. no Isc, so all the current provided by PDN goes into discharging CL.

Dynamic logic operating principles II

10. Power consumption usually higher than static CMOS.
    - Good: No static current.
    - Good: No glitching.
    - Bad: Higher transition probabilities.
    - Bad: More load on clock distribution network.
11. $V_M = V_{IH} = V_{IL} = V_{TN}$ so noise margin is low.
12. Needs precharge and evaluation cycle.

Upcoming topics

- Example problems on recently covered material.
- Latches and flip-flops.

Homework assignment

- 11 November, Thursday: Homework 3.
- 16 November, Tuesday: Read Sections 7.1, 7.2.1–7.2.3 in J. Rabaey, A. Chandrakasan, and B. Nikolic. *Digital Integrated Circuits: A Design Perspective*. Prentice-Hall, second edition, 2003.
- 22 November, Thursday: Lab 4.

Special topic: ALU design

Daniel Clifford and Ike Anyanetu