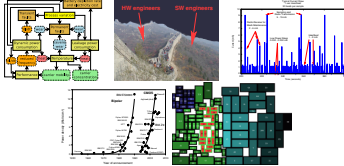


## Digital Integrated Circuits – EECS 312

<http://ziyang.eecs.umich.edu/~dickrp/eecs312/>

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### Lab 3

- Transistor sizing in logic gates.
- Due 12:00 midnight. Fine to establish completion time by emailing report, but please hand in hardcopy by Thursday.

Derive and explain.

### Power consumption in synchronous CMOS

$$P = P_{SWITCH} + P_{SHORT} + P_{LEAK}$$

$$P_{SWITCH} = C \cdot V_{DD}^2 \cdot f \cdot A$$

$$\dagger P_{SHORT} = \frac{b}{12} (V_{DD} - 2 \cdot V_T)^3 \cdot f \cdot A \cdot t$$

$$P_{LEAK} = V_{DD} \cdot (I_{SUB} + I_{GATE} + I_{JUNCTION} + I_{IDL})$$

$C$ : total switched capacitance       $V_{DD}$ : high voltage  
 $f$ : switching frequency       $A$ : switching activity  
 $b$ : MOS transistor gain       $V_T$ : threshold voltage  
 $t$ : rise/fall time of inputs

$$\dagger P_{SHORT} \text{ usually } \leq 10\% \text{ of } P_{SWITCH}$$

Smaller as  $V_{DD} \rightarrow V_T$

$A < 0.5$  for combinational nodes, 1 for clocked nodes.

### Fixed voltage charging

$$E_R^{step} = \int_{t=0}^{\infty} V_R(t) I_R(t) dt$$

$$E_R^{step} = \int_{t=0}^{\infty} V_R(t) \frac{V_R(t)}{R} dt$$

$$E_R^{step} = \int_{t=0}^{\infty} V_{DD} e^{-t/RC} \frac{V_{DD} e^{-t/RC}}{R} dt$$

$$E_R^{step} = \frac{V_{DD}^2}{R} \int_{t=0}^{\infty} e^{-2t/RC} dt$$

$$E_R^{step} = \frac{V_{DD}^2}{R} \left( -\frac{RC}{2} \right) \left( e^{-2t/RC} \right)_{t=0}^{\infty}$$

$$E_R^{step} = \frac{-V_{DD}^2 C}{2} (0 - 1)$$

$$E_R^{step} = \frac{V_{DD}^2 C}{2}$$

### Review

- How can the optimal number of inverters in a load-driving chain be determined?
- How can the optimal size of each inverter in the chain be decided?
- How do determine optimal sizes of logic gates in arbitrary structures?
  - May cover this near end of course.
- Do example problem.

Derive and explain.

### Speakers and topics

- 4 November: Katherine, Olga, and Matt. Atomic layer deposition.
- 11 November: Ike and Dan. ALU design alternatives.
- 16 November: Michael, Heesung, and Jiayi. Impact of materials on devices and circuits.
- Haishan and Guanyu. Optical interconnect.
- Tyler and Megan. Subthreshold circuit applications.
- Sui Yu, Zhenghong and Wang Yi. FinFETs.
- Bo Zhu, Terence, and Baishun. Resonant tunneling devices.
- Shaobing and Haoyu. Circuit Elements Improvement for Wireless Sensor Network.
- Austin: Memristors.

### Reasons for power consumption

- Dynamic
  - Charging and discharging RC loads.
  - $E_{dyn} = C_L V_{DD}^2$ .
  - $P_{dyn} = C_L V_{DD}^2 f$ .
  - But  $f \propto V_{DD}$ .
  - So  $P_{dyn} = C_L V_{DD}^3$ .
- Static
  - Sub-threshold leakage.
  - Gate leakage.
- Short-circuit: Pull-up and pull-down networks briefly both on.

### Fixed current charging

$$E_R^{ramp} = \int_{t=0}^{\infty} V_R(t) I_R(t) dt$$

Let  $T$  be the voltage ramp duration,  $I_R$  is fixed.  $V_R$  is fixed.

## Fixed current charging II

$$\Delta V = \frac{\Delta q}{C}$$

$$V_{DD} = \frac{I_R T}{C}$$

$$I_R = \frac{C V_{DD}}{T}$$

$$V_R = R I_R$$

$$E_R^{ramp} = \int_{t=0}^T V_R(t) \frac{C V_{DD}}{T} \frac{R C V_{DD}}{T} dt$$

$$E_R^{ramp} = \frac{R V_{DD}^2 C^2}{T^2} \int_{t=0}^T 1 dt$$

## Break-even point

$$E_R^{step} = E_R^{ramp}$$

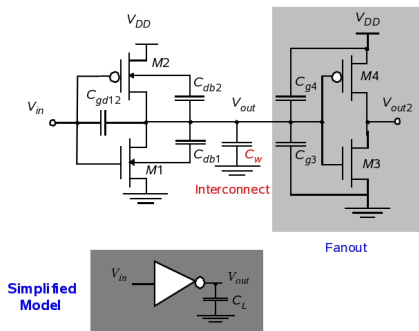
$$\frac{V_{DD}^2 C}{2} = \frac{V_{DD}^2 C 2RC}{2 T}$$

$$1 = \frac{2RC}{T}$$

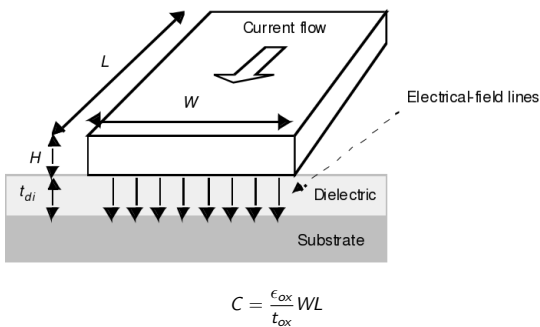
$$T = 2RC$$

- Properly controlling  $V_R(t)$ .
- Performance.
- In limit, permits reversible computation with low/no power consumption during charging and discharging.

## Capacitive load modeling



## Interconnect capacitance



## Fixed current charging III

$$E_R^{ramp} = \frac{V_{DD}^2 C^2 R}{T^2} T$$

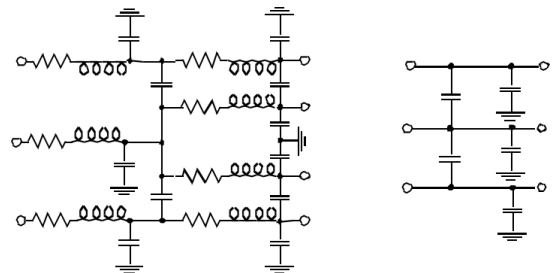
$$E_R^{ramp} = \frac{V_{DD}^2 C^2 R}{T}$$

$$E_R^{ramp} = \frac{V_{DD}^2 C 2RC}{2 T}$$

## Charging methods summary

- $I(t)$  influences energy consumption for same change in  $V$ .
- In theory, keeping voltage differences very small can permit extremely low-power operation.
- Leakage, current control, and preserving reversibility make this challenging.

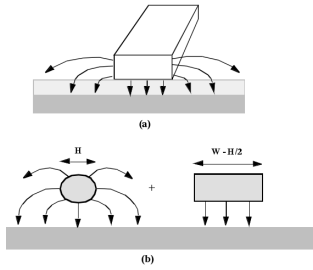
## Interconnect modeling



## Permittivity ( $k$ )

Material	$\epsilon$
Vacuum	1
Aerogels	~1.5
Polyimides	3-4
SiO <sub>2</sub>	3.9
Glass-epoxy	5
Si <sub>3</sub> N <sub>4</sub>	7.5
Alumina	9.5
Silicon	11.7

## Fringing



$$C_{\text{wire}} = C_{pp} + C_{\text{fringe}} = W \frac{\epsilon_{ox}}{t_{ox}} + \frac{2\pi\epsilon_{ox}}{\log(t_{ox}/H)}$$

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## Upcoming topics

- Alternative logic design styles.
- Latches and flip-flops.
- Memories.

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## Trends in interconnect design

- More metal layers.
- Higher aspect ratios.
  - More coupling.
- Smaller transistors, but similar-length global interconnect.

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## Homework assignment

- 4 November, Thursday: Read Sections 6.2.2 and 6.2.3 in J. Rabaey, A. Chandrakasan, and B. Nikolic. *Digital Integrated Circuits: A Design Perspective*. Prentice-Hall, second edition, 2003.
- 4 November, Thursday: First short talk.
- 11 November, Thursday: Homework 3.

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