Digital Integrated Circuits – EECS 312
http://robertdick.org/eecs312/

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Latches and flip-flops
Memory array structures
Memory array structures
Dynamic random access memory

Review

- What is charge sharing?
- Why are there two different expressions for the voltage to which \( V_{out} \) settles?
- Is leakage a significant factor in charge sharing?
- How can it be prevented?
- What is volatile memory?
- What is non-volatile memory?
- What is static memory?
- What is dynamic memory?

Derive and explain.

Combinational vs. sequential logic

- No feedback between inputs and outputs – combinational
  - Outputs a function of the current inputs, only
- Feedback – sequential

D flip-flops

plain old combinational logic

Sequential logic

- Outputs depend on current state and (maybe) current inputs
- Next state depends on current state and input
- For implementable machines, there are a finite number of states
- Synchronous
  - State changes upon clock event (transition) occurs
- Asynchronous
  - State changes upon inputs change, subject to circuit delays

Flip-flop introduction

- Stores, and outputs, a value.
- Puts a special clock signal in charge of timing.
- Allows output to change in response to clock transition.
- More on this later.
  - Timing and sequential circuits

Introduction to sequential elements

- Feedback and memory.
- Memory.
- Latches.
Feedback and memory

- Feedback or physical state are the root of memory.
- Can compose a simple loop from inverters.
- However, there is no way to switch the value.

TG and NOT-based memory

- Can break feedback path to load new value.
- However, potential for timing problems.

Reset/set latch

- Can break feedback path to load new value.
- How can this be made more area-efficient?
- Resize transistors, remove transistors, use state?

Reset/set timing

- Unstable state
- Unstable state
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Homework

Reset/set latches
Clocking conventions
Other memory elements

Clocking terms

- Clock – Rising edge, falling edge, high level, low level, period
- Setup time: Minimum time before clocking event by which input must be stable ($T_{SU}$)
- Hold time: Minimum time after clocking event for which input must remain stable ($T_{TH}$)
- Window: From setup time to hold time

Gated RS latch

Memory element properties

<table>
<thead>
<tr>
<th>Type</th>
<th>Inputs sampled</th>
<th>Outputs valid</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unclocked latch</td>
<td>Always</td>
<td>LFT</td>
</tr>
<tr>
<td>Level-sensitive latch</td>
<td>Clock high</td>
<td>LFT</td>
</tr>
<tr>
<td>Edge-triggered flip-flop</td>
<td>($T_{SU}$ to $T_{TH}$) around falling clock edge</td>
<td>Delay from rising edge</td>
</tr>
</tbody>
</table>

Clocking conventions

Active–high transparent

Active–low transparent

Positive (rising) edge

Negative (falling) edge

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### Timing for edge and level-sensitive latches

**D**, **Clk**, **Q edge**, **Q level**

- **Latch timing specifications**
  - Minimum clock width, \( T_W \)
    - Usually period / 2
  - Low to high propagation delay, \( P_{LH} \)
  - High to low propagation delay, \( P_{HL} \)
  - Worst-case and typical

**Example, negative (falling) edge-triggered flip-flop timing diagram**

- **Example, positive (rising) edge-triggered flip-flop timing diagram**

### RS latch states

<table>
<thead>
<tr>
<th>( S )</th>
<th>( R )</th>
<th>( Q^+ )</th>
<th>( \bar{Q}^+ )</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>( Q )</td>
<td>( \bar{Q} )</td>
<td>unstable</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**Notes**

- \( T_{su} \) ns
- \( T_{hi} \) ns
- \( T_{phl} \) ns
- \( T_{ph} \) ns

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Reset/set latches
Clocking conventions
D flip-flop
Other memory elements

Falling edge-triggered D flip-flop

- Use two stages of latches
- When clock is high
  - First stage samples input w/o. changing second stage
  - Second stage holds value
- When clock goes low
  - First stage holds value and sets or resets second stage
  - Second stage transmits first stage
  - \( Q^+ = D \)
- One of the most commonly used flip-flops

Edge triggered timing

RS clocked latch

- Storage element in narrow width clocked systems.
- Dangerous.
- Fundamental building block of many flip-flop types.

D flip-flop

- Minimizes input wiring.
- Simple to use.
- Common choice for basic memory elements in sequential circuits.

Toggle (T) flip-flops

- State changes each clock tick
- Useful for building counters
- Can be implemented with other flip-flops
  - D with XOR feedback

Asynchronous inputs

- How can a circuit with numerous distributed edge-triggered flip-flops be put into a known state?
- Could devise some sequence of input events to bring the machine into a known state.
  - Complicated.
  - Slow.
- Not necessarily possible, given trap states.
- Can also use sequential elements with additional asynchronous reset and/or set inputs.
Schmitt triggers

- A logic stage is an RC network
- Whenever a transition occurs, capacitance is driven through resistance
- Consider the implementation of a CMOS inverter

Debouncing

- Mechanical switches bounce!
- What happens if multiple pulses?
  - Multiple state transitions
  - Need to clean up signal

Latch and flip-flop equations

- RS
  \[ Q^+ = S + \overline{R} \cdot Q \]
- D
  \[ Q^+ = D \]
- T
  \[ Q^+ = T \oplus Q \]

Reason for gradual transition

- A logic stage is an RC network
- Whenever a transition occurs, capacitance is driven through resistance
- Consider the implementation of a CMOS inverter

Review

- What are \( t_{su} \) and \( t_{th} \)?
- Define
  - Level-sensitive.
  - Edge-triggered.
  - Latch.
  - Flip-flop.
- What is the symbol for a falling edge triggered D flip-flop?
- Show a circuit design for a Schmitt-trigger inverter.

Derive and explain.
Derive the propagation delay of an aluminum wire that is 2 cm long and 500 nm wide. Does using a lumped model introduce significant error? You may assume a sheet resistance of 0.075 $\Omega/\square$. Derive the propagation delay of a copper wire with the same shape. State, and verify, any assumptions.

Derive and explain.

\[ f(a, b, c) = ab + c \]

Non-volatile memory

- ROM.
- EEPROM.
- Flash.

Floating gate technology

- UV erase.
- Electrical erase.
- Block erase.

Hot floating gate implementation

- Was once difficult to design uniform-thickness thin oxide layers.
- Tunneling-based programming was difficult.
- Avalanche injection (hot electron) based programming used.
- UV erasure.
- Pure tunneling later became practical (EEPROM).
- Flash uses hot electrons for programming and tunneling for erasing.
Array memory architecture

Block-based memory architecture

Memory timing

Review

- What are the different ways a floating-gate memory cell can be erased?
- What are the different ways a floating-gate memory cell can be programmed?
- What are the two main DRAM bit cell organizations, and their advantages?
- Why is it difficult to economically put DRAM on the same die as a processor?
- Why are decoders and MUXs used in memory arrays?

Derive and explain.

NOR ROM schematic

NOR ROM layout

Program using active layer.
NOR ROM layout

Program using contacts.

NAND ROM schematic

Program using metal layer.

NAND ROM layout

Program using implants.

DRAM

Write: $C_s$ is charged or discharged by asserting WL and BL.
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Differential sense amplifier

Useful for SRAM, can use two stages.

Latch sense amplifier

Useful for DRAM.

Charge pump

Upcoming topics

- Theoretical foundations for sizing.

Homework assignment I

- 7 November: Project 4.
Homework assignment II


- 16 November: Homework 4.