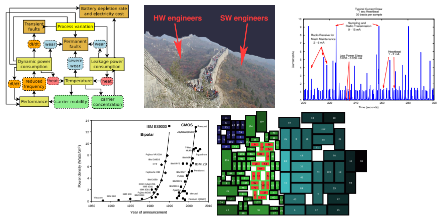
Digital Integrated Circuits – EECS 312

http://robertdick.org/eecs312/

Teacher:	Robert Dick	GSI:	Shengshou Lu
Office:	2417-E EECS	Office:	2725 BBB
Email:	dickrp@umich.edu	Email:	luss@umich.edu
Phone:	734–763–3329		
Cellphone:	847–530–1824		



Review

- When are the advantages and disadvantages of fixed-voltage charging?
- When are the advantages and disadvantages of fixed-current charging?
- In what situation is each of the following models important?
  - Ideal.
  - C.
  - RC.
  - RLC.
- What are dI/dt effects? Under what circumstances do they cause the most trouble?

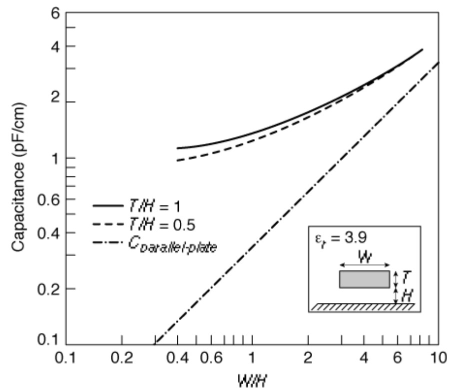
Derive and explain.

Rent's rule

$$T = ak^p$$

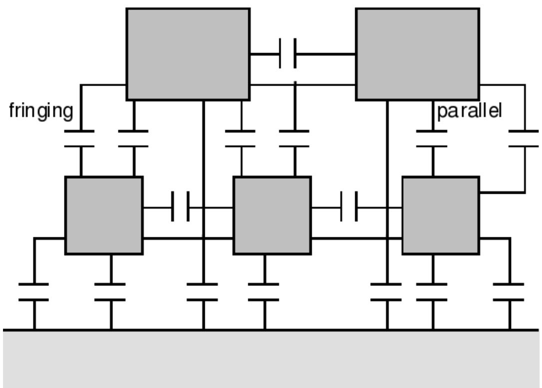
- T: Number of terminals.
- a: Average number of terminals per block.
- k: Number of blocks within chip.
- p: Rent's exponent, ≤ 1, generally around 0.7.

Fringe vs. parallel plate capacitance

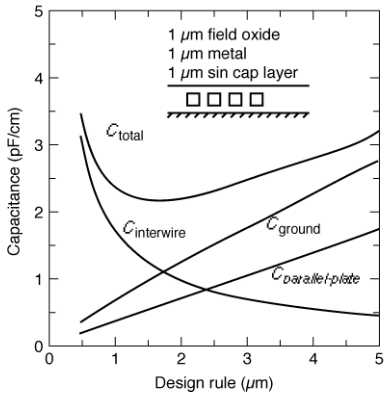


Plot of C_{total} for different gap ratios.

Inter-wire capacitance



Impact of inter-wire capacitance



Wire resistance

- $R = \frac{\rho L}{HW}$.
- Consider fixed-height, fixed-ρ square material, i.e., $L/W = 1$.
- $R = \frac{\rho}{H}$.

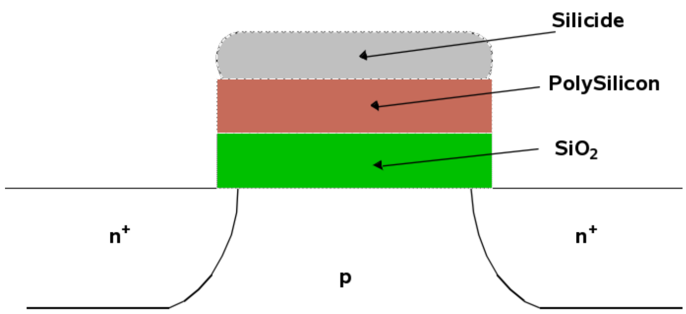
Interconnect resistance

Material	ρ (Ω m) $\times 10^{-8}$
Silver	1.6
Copper	1.7
Gold	2.2
Aluminum	2.7
Tungsten	5.5

Reducing resistance

- Higher interconnect aspect ratios
- Material selection
  - Copper
  - Silicides
  - Carbon nanotubes
- Structural changes
  - More interconnect layers
  - 3-D integration

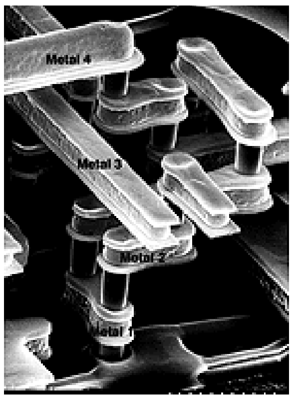
Silicides



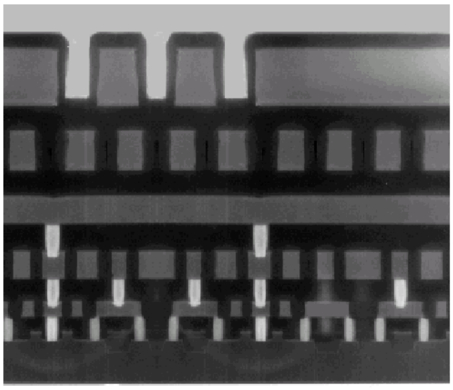
Resistances

Material	Sheet resistance ($\Omega/\square$)
n- or p-well diffusion	1,000–1,500
n^+ or p^+ diffusion	50–150
silicided n^+ or p^+ diffusion	3–5
doped polysilicon	150–200
doped silicides polysilicon	4–5
Aluminum	0.05–0.1

Multi-layer interconnect



Side view of interconnect



Interconnect summary

- It is important to know which interconnect model to use in which situation.
  - Ideal.
  - C.
  - RC.
  - RLC.
- dI/dt effects are particularly important in power delivery networks.
- Capacitive coupling complicates design.
- Cu and silicides can be used to reduce resistance.

Delay modeling

- Single-node lumped model inaccurate.
- Full detailed accurate model intractable for manual analysis and slow for automated analysis.
- Elmore delay model permits rapid analysis with often adequate accuracy.

Elmore delay

Problem definition

- Goal: Determine τ for RC path.
- Note: Source node is implicit.
- C_i: Self-capacitance of node i.
- R_{ii}: Path resistance from source to node i.
- R_{ik}: Shared resistance from source to both nodes i and k.

$$\tau_i = \sum_{k=1}^{N} C_k R_{ik}$$

Derive and explain.

Special case: RC chains

- Consider π network.
- $\tau_n = \sum_{i=1}^{n} C_i \sum_{j=1}^{i} R_j$.
- Use homogeneous discretization.
- $\forall_{i=2}^{N} C_i = C_1$

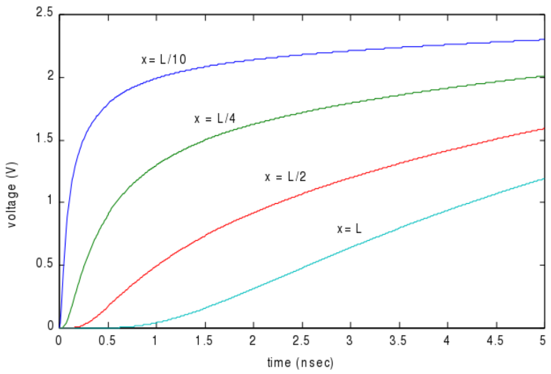
$$\begin{aligned}\tau &= \sum_{k=1}^{N} C R_{nk} \\ &= \frac{L}{N} c \frac{L}{N} r \frac{N(N+1)}{2} \\ &= rcL^2 \frac{N+1}{2N}\end{aligned}$$

What if $N \to \infty$? $\tau \to rcL^2/2$.

Underlying continuous physical model

$$cr\frac{\delta V}{\delta t} = \frac{\delta^2 V}{\delta x^2}$$

Response to step function over time and space



Power delivery network considerations

- IR drop.
- dI/dt effects.
- Location of parasitic inductance.
- Methods to correct power delivery network non-idealities.

Simplifying assumptions

- Ignore wire RC delay when wire delay does not much exceed that of the driving gate, i.e.,
$$L_{crit} \gg \sqrt{\frac{t_{p,gate}}{0.38rc}}$$
- Ignore wire RC when rise time greater than RC delay.
- Ignore for high-resistance wires: $R > 0.2C$.
- Ignore when time of flight is large compared to rise or fall time: $t_{rise,fall} < 2.5 t_{flight}$.

Elmore delay summary

- Pick simplest model for intended purpose: C, RC, or RLC.
- Capacitive coupling complicates timing analysis.
- Transition direction impacts C magnitude in simplified ground-cap model.
- Learn Elmore delay. It is a good first-order approximation of network delay.

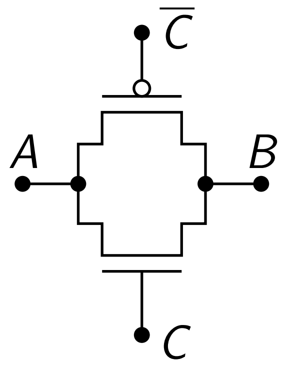
Static CMOS design styles and components

- Logic gates
- Switch-based design
- MUX
- DEMUX
- Encoder
- Decoder

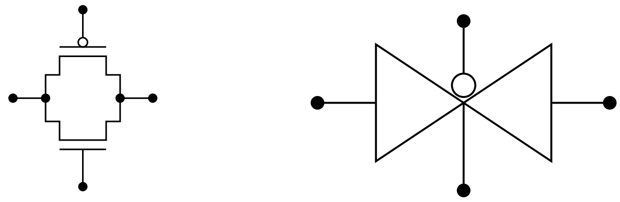
Transistor sizing review

- Goal: equal τ for worst-case pull-up and pull-down paths.
- Observations
  - Adding duplicate parallel path halves resistance.
  - Adding duplicate series path doubles resistance.
  - Doubling width halves resistance.
- Consider logic gate examples.

CMOS transmission gate (TG)



Other TG diagram



Multiplexer (MUX) definitions

- Also called *selectors*
- 2^n inputs
- n control lines
- One output

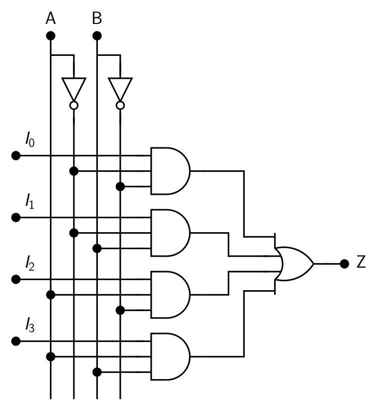
MUX functional table

C	Z
0	I_0
1	I_1

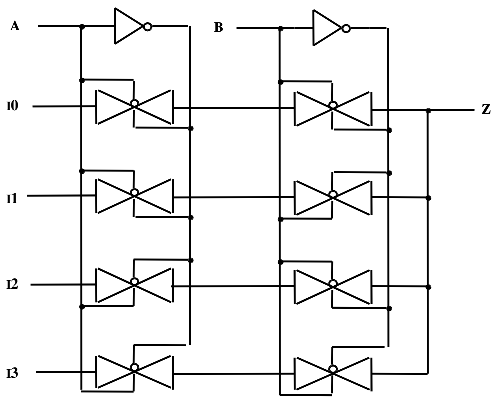
MUX truth table

I_1	I_0	C	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

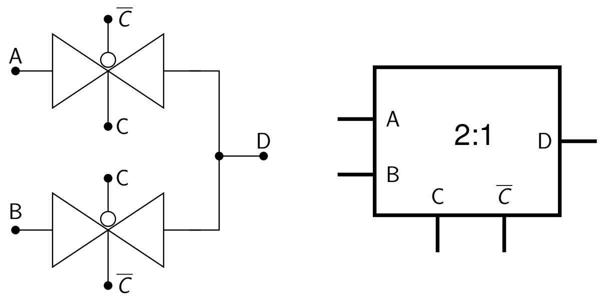
MUX using logic gates



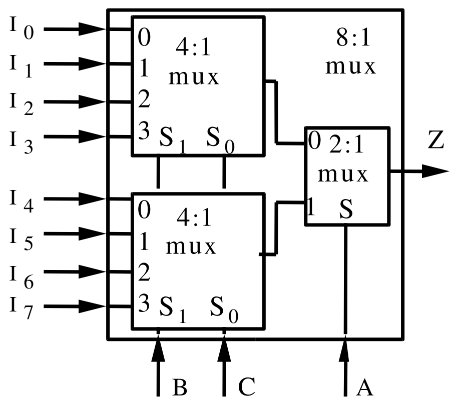
MUX using TGs



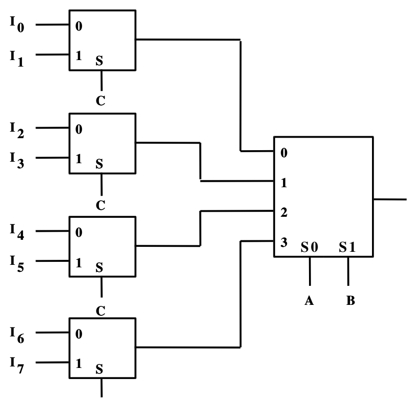
MUX



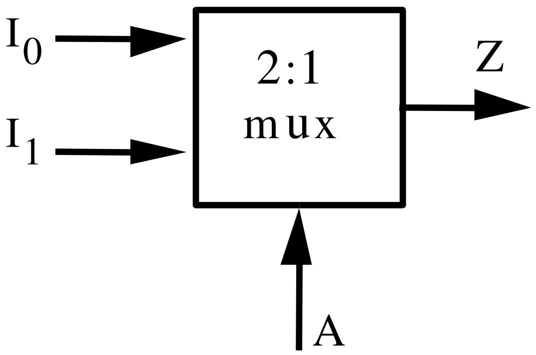
Hierarchical MUX implementation



Alternative hierarchical MUX implementation

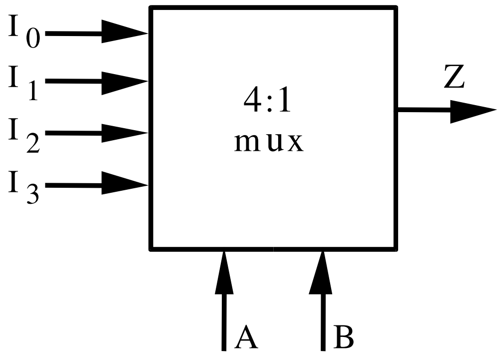


MUX examples



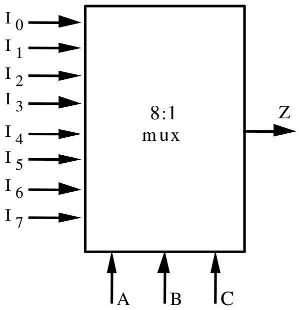
$Z = \overline{A} I_0 + A I_1$

MUX examples



$Z = \overline{A}\,\overline{B} I_0 + \overline{A} B I_1 + A \overline{B} I_2 + A B I_3$

MUX examples



$$Z = \overline{A}\,\overline{B}\,\overline{C} I_0 + \overline{A}\,\overline{B} C I_1 + \overline{A} B \overline{C} I_2 + \overline{A} B C I_3 + A \overline{B}\,\overline{C} I_4 + A \overline{B} C I_5 + A B \overline{C} I_6 + ABC I_7$$

MUX properties

- A $2^n : 1$ MUX can implement any function of n variables
- A $2^{n-1} : 1$ can also be used
  - Use remaining variable as an input to the MUX

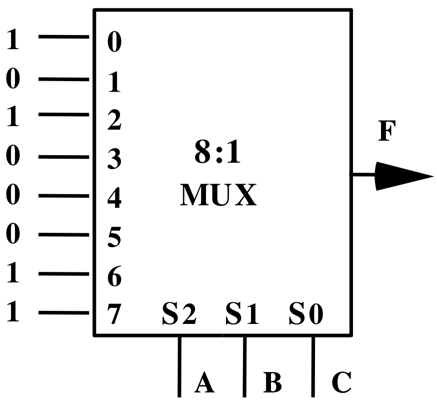
MUX example

$$F(A, B, C) = \sum(0, 2, 6, 7)$$
$$= \overline{A}\,\overline{B}\,\overline{C} + \overline{A} B \overline{C} + A B \overline{C} + ABC$$

Truth table

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Lookup table implementation



MUX example

$$F(A, B, C) = \sum(0, 2, 6, 7)$$
$$= \overline{A}\,\overline{B}\,\overline{C} + \overline{A} B \overline{C} + A B \overline{C} + ABC$$

Therefore,

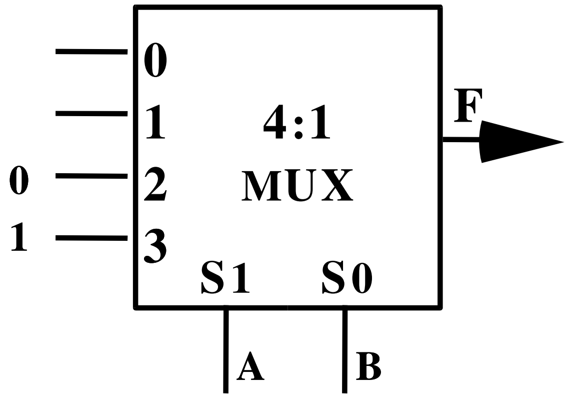
$$\overline{A}\,\overline{B} \rightarrow F = \overline{C}$$
$$\overline{A} B \rightarrow F = \overline{C}$$
$$A \overline{B} \rightarrow F = 0$$
$$AB \rightarrow F = 1$$

Truth table

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

$F = \overline{C}$

Lookup table implementation



Logic design summary

- Logic gate, transmission gate, and pass transistor design each have applications.
- MUX-based design provides a good starting point for transmission gate and pass transistor based design.

Examples

Instead of flying through a bunch of slides, let's try examples.

- $f(a) = a$.
- $f(a) = \overline{a}$
- $f(a, b) = a\overline{b}$
- $f(a, b) = ab$ (Check Figure 6-33 in J. Rabaey, A. Chandrakasan, and B. Nikolic. *Digital Integrated Circuits: A Design Perspective.* Prentice-Hall, second edition, 2003!)
- $f(a, b, c) = ab + \overline{b}c$ (try both ways).

Derive and explain.

Upcoming topics

- Alternative logic design styles.
- Latches and flip-flops.
- Memories.

Homework assignment

- 22 October: Read sections 4.4.1, 4.4.4, and 9.3.3 in J. Rabaey, A. Chandrakasan, and B. Nikolic. *Digital Integrated Circuits: A Design Perspective.* Prentice-Hall, second edition, 2003.
- 24 October: Read sections 6.2.2 and 6.2.3 in J. Rabaey, A. Chandrakasan, and B. Nikolic. *Digital Integrated Circuits: A Design Perspective.* Prentice-Hall, second edition, 2003.
- 25 October: Lab 3.
- 29 October: Homework 3.