# Digital Integrated Circuits – EECS 312

http://robertdick.org/eecs312/

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|---|---|---|---|
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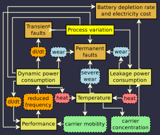
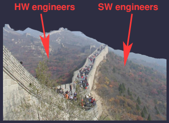
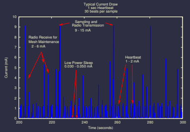
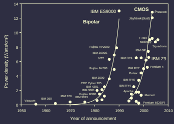
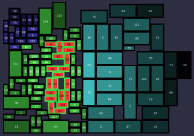

Battery depletion rate and electricity cost
Transient faults
Process variation
dI/dt
wear
Permanent faults
wear
Dynamic power consumption
severe wear
Leakage power consumption
dI/dt
reduced frequency
heat
Temperature
heat
Performance
carrier mobility
carrier concentration









# Announcement

1. I will be in Montreal on Tuesday presenting a research paper at Embedded Systems Week.
2. I will lecture at the Friday discussion time and location.
3. Mr. Lu will hold discussion at the Tuesday lecture time slot and location.

# Review

1. How many metal layers are there in modern processes?
2. What is the problem with isotropic etching?
3. Explain a method of anisotropic etching.
4. Why Cu?
5. Why damascene?
6. What is CMP?
7. What is DRC?

# Example low-k dielectric materials

- Still active area.
- Porous $SiO_2$.
- Carbon-doped $SiO_2$.
- Polymer.

# Synchronous integrated circuit organization

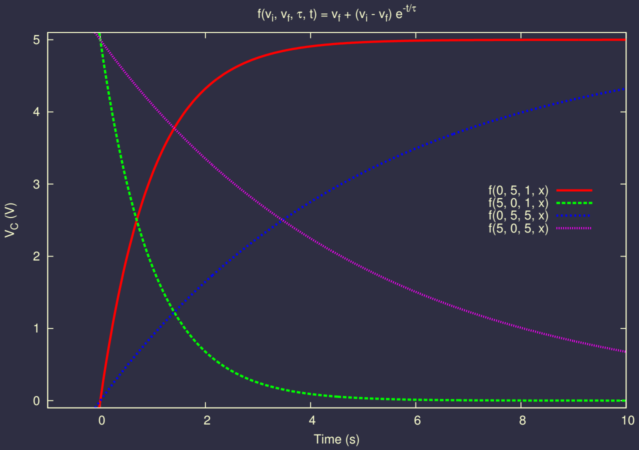
- Combinational networks separated by memory elements.
- When memory elements clocked, changed signals race through next stage.
- Clock frequency must be low enough to allow signal to propagate along worst-case combinational path in circuit.

Derive and explain.

# Lecture plan

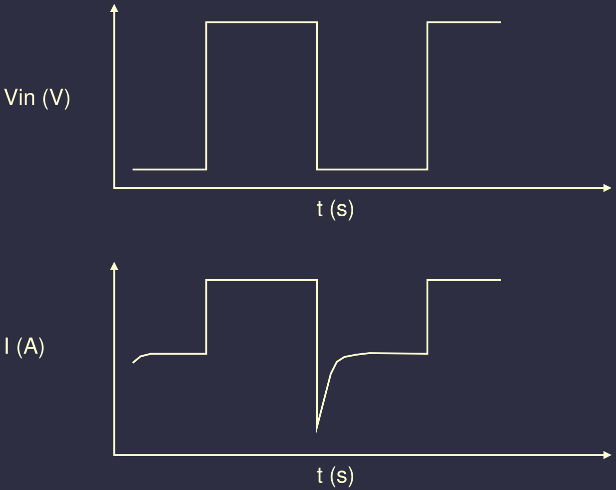
1. Transistor dynamic behavior
2. Inverter switch model
3. Inverter transfer curves and parameter optimization
4. Homework

# RC curves

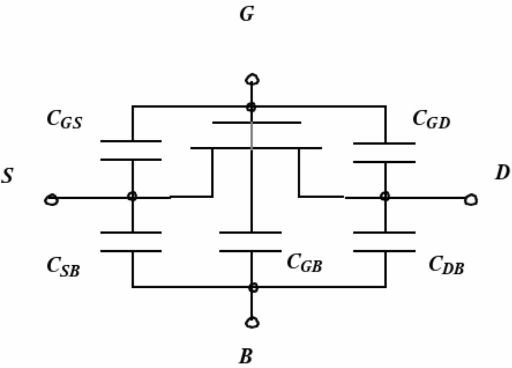


$$v(t) = v_f + (v_i - v_f)e^{-t/RC}$$

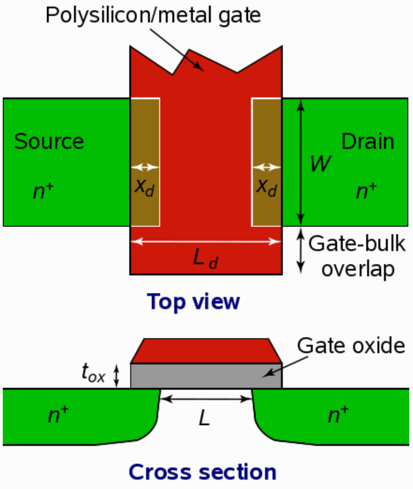
# Diode dynamic behavior



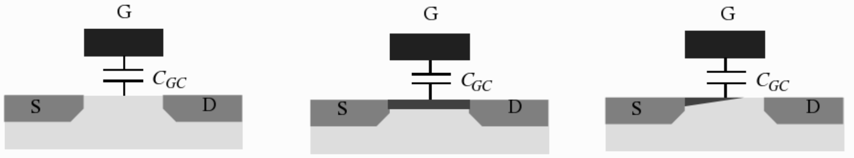
# MOSFET capacitances



# Gate capacitance



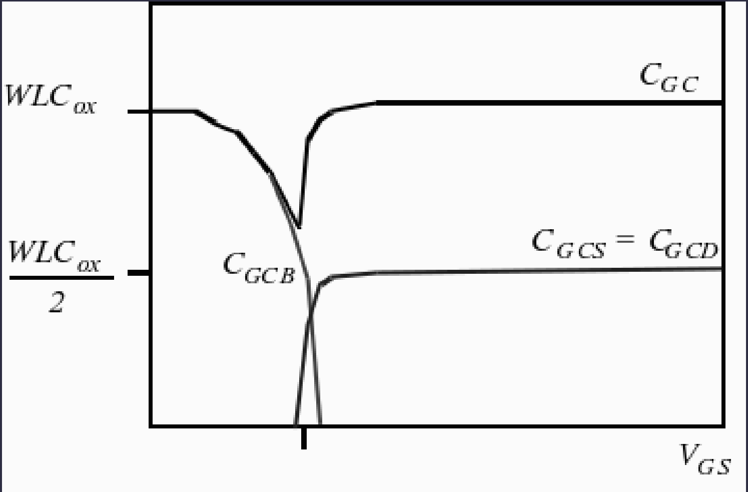
# Gate capacitance schematic



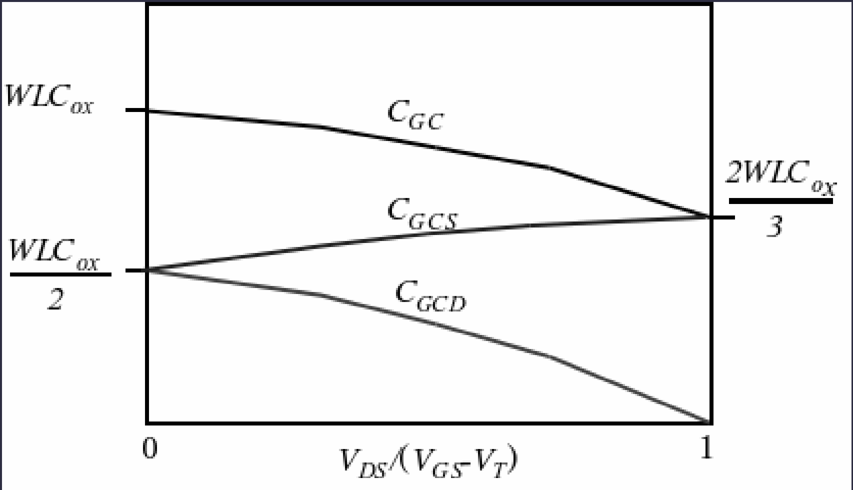
| Mode | $C_{GCB}$ | $C_{GCS}$ | $C_{GCD}$ | $C_G$ |
|---|---|---|---|---|
| Cutoff | $C_{ox}WL$ | 0 | 0 | $C_{ox}WL + 2C_OW$ |
| Triode | 0 | $C_{ox}WL/2$ | $C_{ox}WL/2$ | $C_{ox}WL + 2C_OW$ |
| Saturation | 0 | $^2/_3 C_{ox}WL$ | 0 | $^2/_3 C_{ox}WL + 2C_OW$ |

$C_O$ is the overlap capacitance.

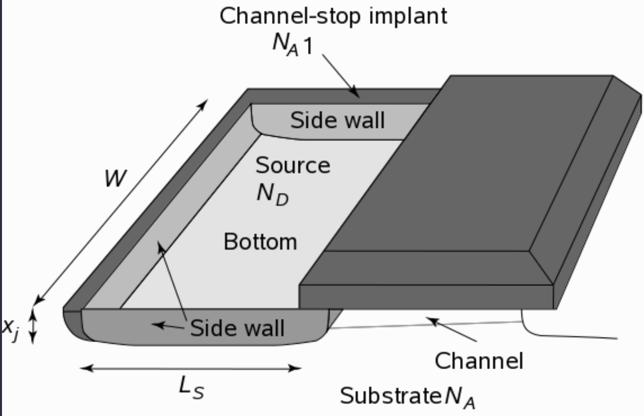
# Gate capacitance variation with $V_{GS}$



# Gate capacitance variation with saturation



# Diffusion capacitance diagram



# Diffusion capacitance expression

$$\begin{aligned}
C_{diff} &= C_{bot} + C_{sw} \\
C_{diff} &= C_j A + C_{jsw} P \\
C_{diff} &= C_j L_S W + C_{jsw}(2L_S + W)
\end{aligned}$$

- $C_{bot}$: Bottom capacitance to substrate.
- $C_{sw}$: Side-wall capacitances for three non-channel sides.
- $C_j$: Junction capacitance constant in $\mathrm{F/m^2}$ (base units).
- $A$: Diffusion area.
- $C_{jsw}$: Junction side-wall capacitance constant in F/m.
- $P$: Perimeter for three non-channel sides.
- $L_S$: Length of diffusion region.
- $W$: Width of diffusion region (and transistor).

# Junction capacitance

- $C_{jsw}$ is actually the diode capacitance we considered before.
- What happens as reverse bias increases?
- Can use worst-case approximation.

# Capacitance linearization I

- Can approximate variable capacitance as fixed capacitance.
- Uses fitting.

$$C_{eq} = \frac{\Delta Q_j}{\Delta V_D}$$

$$C_{eq} = \frac{Q_j\left(V_{high}\right) - Q_j\left(V_{low}\right)}{V_{high} - V_{low}}$$

$$C_{eq} = K_{eq} C_{j0}$$

$$K_{eq} = \frac{-\phi_0^m}{\left(V_{high} - V_{low}\right)\left(1 - m\right)} \left(\left(\phi_0 - V_{high}\right)^{1-m} - \left(\phi_0 - V_{low}\right)^{1-m}\right)$$

# Capacitance linearization II

- $C_{j0}$: Capacitance when voltage bias of diode is 0 V.
- $m$: Grading coefficient used to model effects of sharp (0.5) or linear (0.33) junction transition (see Page 82 in textbook).
- $\phi_0 = \phi_T \ln\left(\frac{N_A N_D}{{n_i}^2}\right)$: Built-in potential, i.e., voltage across junction due to diffusion at drift–diffusion equalibrium.

# Capacitance parameters for default 0.25 µm process technology

| | $C_{OX}$ (fF/µm$^2$) | $C_O$ (fF/µm) | $C_j$ (fF/µm$^2$) |
|---|---|---|---|
| NMOS | 6 | 0.31 | 2 |
| PMOS | 6 | 0.27 | 1.9 |

| | $m_j$ | $\phi_b$ (V) | $C_{jsw}$ (fF/µm) | $m_{jsw}$ | $\phi_{bsw}$ (V) |
|---|---|---|---|---|---|
| NMOS | 0.5 | 0.9 | 0.28 | 0.44 | 0.9 |
| PMOS | 0.48 | 0.9 | 0.22 | 0.32 | 0.9 |

Properties of bottom and sidewall.

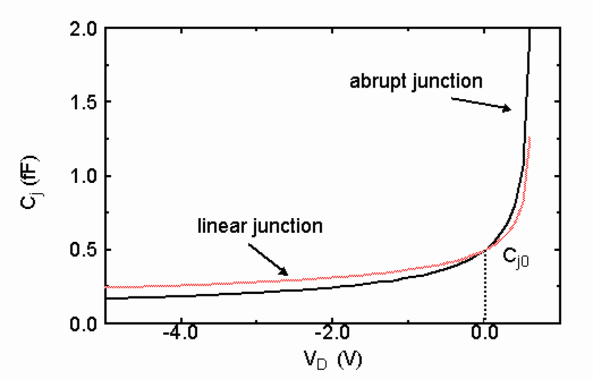
# Upcoming topics

- MOSFET dynamic behavior.
- Wires.
- CMOS inverters.

# Review

- What are the five most important to model capacitances for MOSFETs?
- Explain their locations/sources.
- How do they depend on operating region?
- How are drain and source capacitances calculated?

# Review: diode capacitance



$$C_J = \frac{C_{J0}}{(1 - V_D/\Phi_0)^m}$$

$m = 0.5$ for abrupt junctions, $m = 0.33$ for linear junctions

# A change to gate insulation

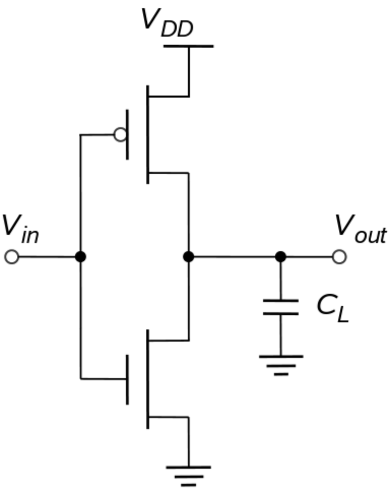
- Mark T. Bohr, Robert S. Chau, Tahir Ghani, and Kaizad Mistry.

  The High-k Solution.
  *IEEE Spectrum*, October 2007.
- What was the problem?
- What was its cause?
- What was the solution?
- Key concepts: gate leakage, tunneling, high-$\kappa$ dielectric, charge traps, single atomic layer deposition, and threshold voltage control.

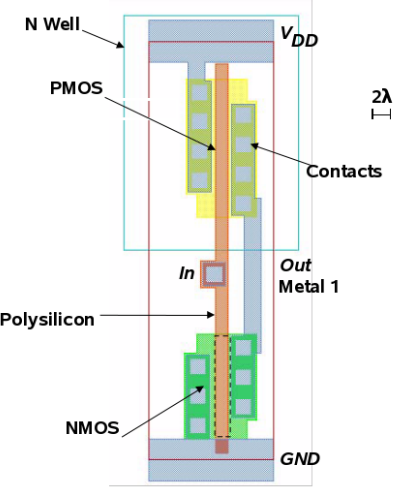
# Lecture plan

1. Transistor dynamic behavior
2. Inverter switch model
3. Inverter transfer curves and parameter optimization
4. Homework

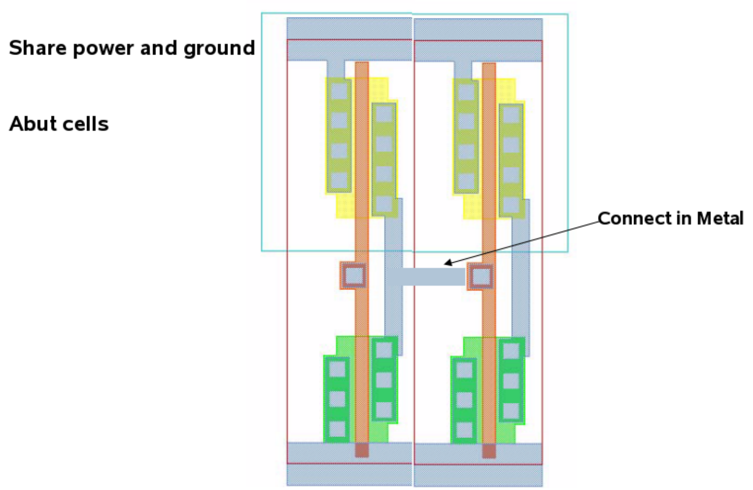
# Simple inverter context



# Inverter layout



# Implications of cell-based design



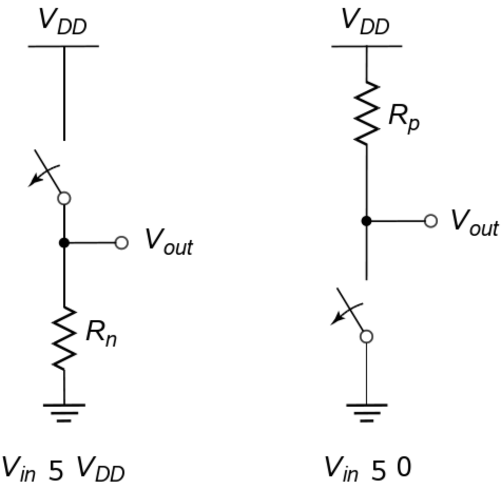
**Share power and ground**

**Abut cells**

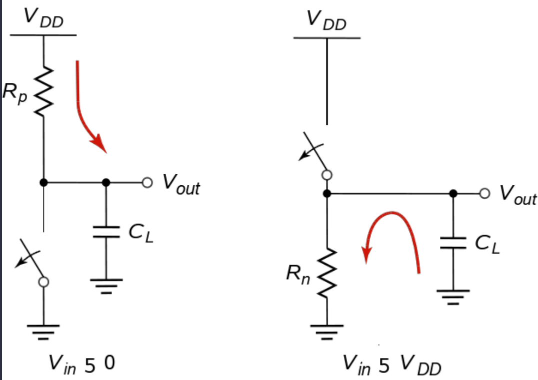
**Connect in Metal**

Power and ground sharing breaks isolation.

# Simplest switch model of inverter



# Switch model transient behavior



- Repeatedly charging/discharging load $C$.
- $t_{pHL} = f(R_{on} C_L)$.
- Why?

# Inverter switch model $t_{pHL}$ derivation

Both $t_{pHL}$ and $t_{pLH}$ defined as time from $0.5\,\mathrm{V_{DD}}$ input crossing to $0.5\,\mathrm{V_{DD}}$ output crossing. Assume step function on input.

$$V_C = V_{DD} e^{-t/RC} \tag{1}$$

Solve for $V_C = V_{DD}/2$.

$$V_{DD}/2 = V_{DD} e^{-t/RC} \tag{2}$$

$$1/2 = e^{-t/RC} \tag{3}$$

$$\ln\left(1/2\right) = -t/RC \tag{4}$$

$$t = -RC \cdot -0.69 \tag{5}$$

$$t = 0.69RC = 0.69\tau \tag{6}$$

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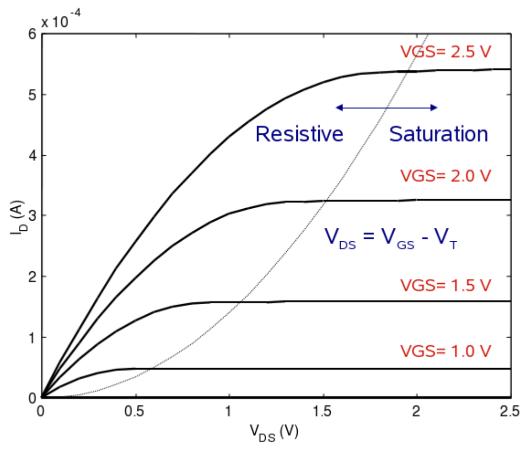
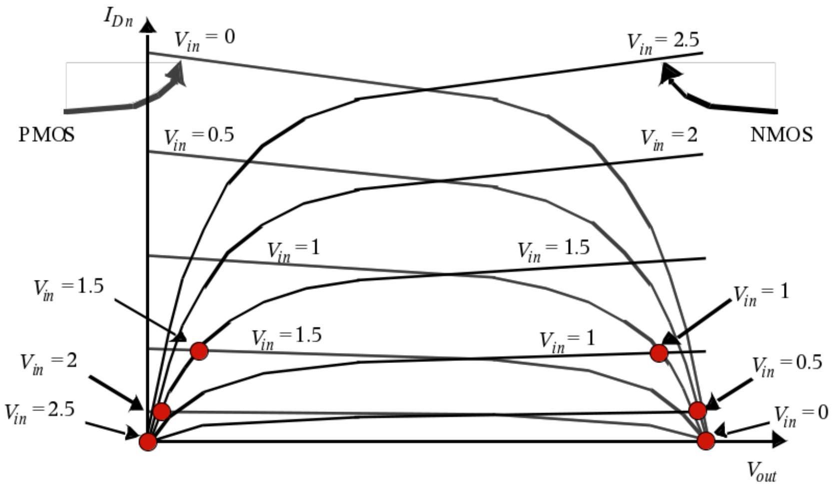
# NMOSFET I–V characteristics

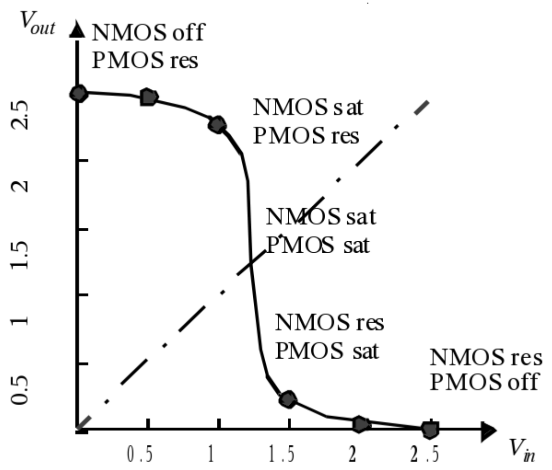


Review: Is this a velocity-saturated short-channel device? How can you tell?

# Inverter load characteristics



# CMOS inverter transfer curve



# Switching threshold derivation I

Find voltage for which $V_{in} = V_{out}$. Known: Both NMOSFET and PMOSFET saturated at this point. Recall that

$$I_{DSAT} = \mu C_{ox} \frac{W}{L} \left( \left( V_{GS} - V_T \right) V_{DSAT} - \frac{{V_{DSAT}}^2}{2} \right) \tag{1}$$

# Switching threshold derivation II

Working to find $V_M$. Find $V_{GS}$ at which NMOSFET and PMOSFET $I_D$ values equal.

$$= kV_{DSAT}\left(V_{GS} - V_T\right) - \frac{V_{DSAT}}{2} \tag{2}$$

$$\begin{aligned} 0 = {} & k_n V_{DSATn}\left(V_M - V_{Tn} - \frac{V_{DSATn}}{2}\right) + \\ & k_p V_{DSATp}\left(V_M - V_{Tp} - \frac{V_{DSATp}}{2}\right) \end{aligned} \tag{3}$$

# Switching threshold derivation III

Solve for $V_M$.

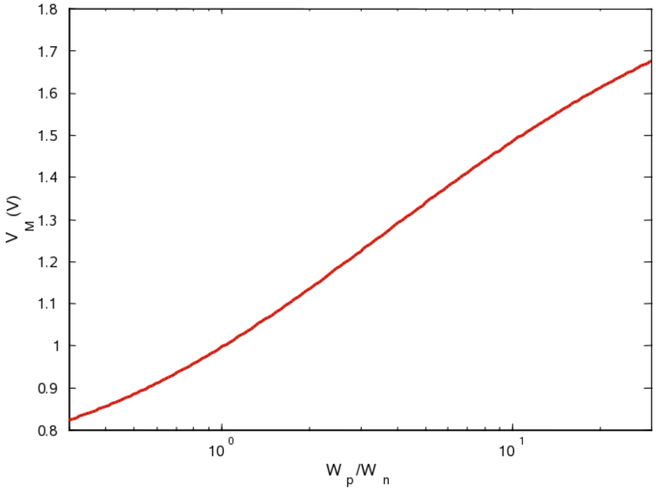
$$V_M = \frac{\left(V_{Tn} + \frac{V_{DSATn}}{2}\right) + r\left(V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2}\right)}{1+r}. \tag{4}$$

$$r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}} = \frac{\nu_{satp} W_p}{\nu_{satn} W_n} \tag{5}$$

$$\nu = \frac{\mu\xi}{1 + \xi/\xi_c} \tag{6}$$

- $\nu$: Charge carrier speed.
- $\xi$: Field strength.
- $\xi_c$: Field strength at which scattering limits further increase in carrier speed.

# Inverter threshold dependence on transistor conductance ratio



# Upcoming topics

- CMOS inverter dynamic behavior.
- Logic gates.

# Lecture plan

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# Homework assignment

- 1 October: Read sections 3.3.3, 5.1, 5.2, 1.3.2, and 1.3.3 in

  J. Rabaey, A. Chandrakasan, and B. Nikolic. *Digital Integrated Circuits: A Design Perspective*.
  Prentice-Hall, second edition, 2003. Read as much as you can by 27 September.
- 26 October: Extended Homework 1 due date due to difficulty getting help during office hours.
- 3 October: Lab 2.