Digital Integrated Circuits – EECS 312
http://robertdick.org/eecs312/

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Typical Current Draw
1 sec Heartbeat: 30 beats per sample
Sampling and Radio Transmission: 9 - 15 mA
Heartbeat: 1 - 2 mA
Radio Receive for Mesh Maintenance: 2 - 6 mA
Low Power Sleep: 0.030 - 0.050 mA

Year of announcement:

Power density (Watts/cm²):
0 2 4 6 8 10 12

Bipolar, CMOS
Vacuum IBM 360
IBM 370 IBM 3033
IBM ES9000
Fujitsu VP2000
IBM 3090S
NTT Fujitsu M-780
IBM 3090
CDC Cyber 205
IBM 4381
IBM 3081
Fujitsu M380
IBM RY5
IBM GP
IBM RY6
IBM RY4
Apache
Pulsar
Merced
IBM RY7
IBM Z9

Prescott
Jayhawk (dual)
Mckinley
Pentium II (DSIP)
T-Rex
Squadrons
Pentium 4
IBM RY5
IBM RY6
IBM RY7
IBM Z9
Lecture plan

1. Lab one

2. Desired transistor behavior

3. Homework
Lab one challenges

- Learning to use the tools (last Friday).
- Understanding the circuits used in the lab (today).
- A note on the CAD tools market.

Derive and explain.
NMOS inverter schematic
Resistance

\[ R = \rho \frac{L}{W} \quad (1) \]
\[ G = \sigma \frac{W}{L} \quad (2) \]
\[ G = \frac{1}{R} \quad (3) \]
\[ \sigma = \frac{1}{\rho} \quad (4) \]

- Assuming fixed height.
- \( R \): resistance.
- \( \rho \): resistivity.
- \( L \): length.
- \( W \): width.
- \( G \): conductance.
NMOS inverter simulation results
**RC network**

\[ V_c = V_{final} + (V_{init} - V_{final}) e^{-\frac{t}{\tau}} \]  \hspace{1cm} (5)

\[ \tau = RC \]  \hspace{1cm} (6)
NMOS $\rightarrow$ CMOS inverter

- How does structure change?
- What impact does transistor width have? Why different widths?
- How does response change?
- What are advantages?
- What are disadvantages?

Derive and explain.
Review questions and note

- What are digital systems built from?
- What gate properties are required for use in digital systems? Why?
- What have the major effects of process scaling been? What challenges does it face in the future?
- What are the physical structures and symbols of (N/P)MOSFETs? How do they work?
Lecture plan

1. Lab one

2. Desired transistor behavior

3. Homework
Desired and actual properties of transistors

Desired properties
- Perfect digital signal transfer.
- No parasitics.

Actual properties
- Imperfect transfer function.
  - Fortunately, has gain and capable of signal regeneration (restoration).
- Parasitic resistance and capacitance.
- Leakage.
Brief introduction to Boolean algebra

- The only values are 0 (or false) and 1 (or true).
- One can define operations/functions/gates.
  - Boolean values as input and output.
- A truth table enumerates output values for all input value combinations.
AND

<table>
<thead>
<tr>
<th>a</th>
<th>b</th>
<th>a ∧ b</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

\[ a \land b = a \wedge b = a \cdot b \]
### OR

<table>
<thead>
<tr>
<th>a</th>
<th>b</th>
<th>a + b</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

\[ a \ OR \ b = a \ \lor \ b = a + b \]
**NOT**

<table>
<thead>
<tr>
<th>a</th>
<th>(\bar{a})</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

\[ NOT \ a = \bar{a} \]
CMOS inverter operation
CMOS inverter operation

\[ V_{DD} \]

\[ V_{SS} \]

\[ A = 0 \]

\[ B = 1 \]

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CMOS inverter operation
CMOS inverter operation

- Input A = 1
- Input B = 0
CMOS inverter operation

\[ \text{A} \quad V_{DD} \quad \overline{\text{A}} \quad V_{SS} \quad \text{B} \]
CMOS inverter operation

\[ V_{DD} \]

\[ A=? \]

\[ B=? \]

\[ V_{SS} \]
NAND operation

A = 0, B = 0 → Z = 1

A = 0, B = 1 → Z = 0

A = 1, B = 0 → Z = 0

A = 1, B = 1 → Z = 1

V_{SS} → Z → V_{DD}
NAND operation
NAND operation

\[ A = 0 \]

\[ B = 1 \]

\[ Z = 1 \]

\[ V_{SS} \]

\[ V_{DD} \]
NAND operation

\[ A \quad \text{and} \quad B \rightarrow Z \]

\[ V_{DD} \quad \text{and} \quad V_{SS} \]

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NAND operation

\[ \text{A} = 1 \quad \text{V}_{\text{SS}} \quad \text{V}_{\text{DD}} \quad \text{Z} = 1 \quad \text{B} = 0 \quad \text{blocked} \quad \text{A} = 1 \quad \text{V}_{\text{SS}} \]
NAND operation

Diagram showing a NAND gate with inputs A and B, and output Z. The diagram includes voltage annotations for V_{SS} and V_{DD}.
NAND operation

A = 1

B = 1

Z = 0

V_{DD}

V_{SS}
NAND operation

A B

V_{DD} V_{SS}

Z
Therefore, *NAND* and *NOR* gates are used in CMOS design instead of *AND* and *OR* gates.
Therefore, *NAND* and *NOR* gates are used in CMOS design instead of *AND* and *OR* gates.
NAND layout
NOR operation
NOR operation
NOR operation

In the NOR operation, when A = 0, the transistor is blocked, and the output is high (VDD). When B = 1, the transistor is also blocked, and the output is high (VDD).
NOR operation

\[ \text{NOR operation} \]

[Diagram of a NOR gate with inputs A and B, and output Z, labeled with V_{DD}, V_{SS}, and V_{SS}.]
NOR operation

A = 1

B = 0

Z = 0

Blocked
NOR operation
NOR operation

![NOR Circuit Diagram]

- A = 1
- B = 1
- Z = 0

V<sub>DD</sub> and V<sub>SS</sub> represent the power supply voltages.
CMOS transmission gates (switches)

- NMOS is good at transmitting 0s
  - Bad at transmitting 1s
- PMOS is good at transmitting 1s
  - Bad at transmitting 0s
- To build a switch, use both: CMOS
CMOS transmission gate (TG)
CMOS transmission gate (TG)

\[ \overline{C} = 0 \]
\[ \overline{C} = 1 \]
CMOS transmission gate (TG)
CMOS transmission gate (TG)

\[ \overline{C} = 0 \quad B = A \]

\[ \overline{C} = 1 \]

\( A \)

\( B \)

\( C \)
CMOS transmission gate (TG)
CMOS transmission gate (TG)
CMOS transmission gate (TG)

\[ \text{blocked} \quad \overline{C} = 1 \]

\[ \text{blocked} \quad C = 0 \]
CMOS transmission gate (TG)

- When $C = 1$, the gate is blocked.
- When $C = 0$, the gate is unblocked.
- $B = \text{High-Z}$

Diagram:

```
+---+     +---+
|   |     |   |
|   |     |   |
+---+     +---+
    |     |   |
    |     |   |
    +-----+-----+
```

- Red arrows indicate the blocked states.

**Homework**

CMOS transmission gate (TG)
CMOS transmission gate (TG)
Other TG diagram
Logic gates vs. TGs

- What can each be used to implement?
- How to decide which to use?
Upcoming topics

- Diodes.
- Transistor static behavior.
- Transistor dynamic behavior.
Lecture plan

1. Lab one

2. Desired transistor behavior

3. Homework
Homework assignment and announcement

- 17 September: Laboratory assignment one.