Digital Integrated Circuits – EECS 312

http://ziyang.eecs.umich.edu/~dickrp/eecs312/

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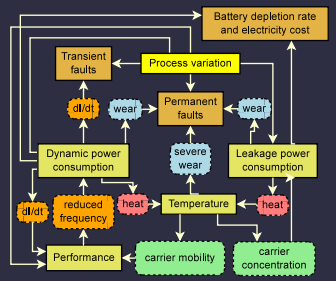
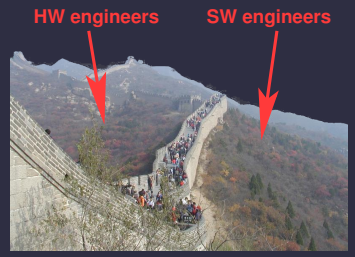
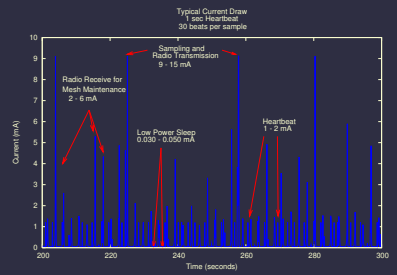
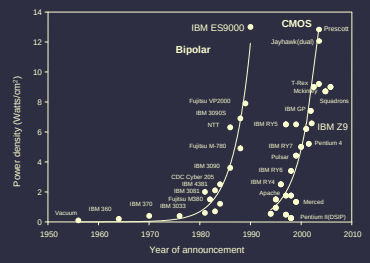
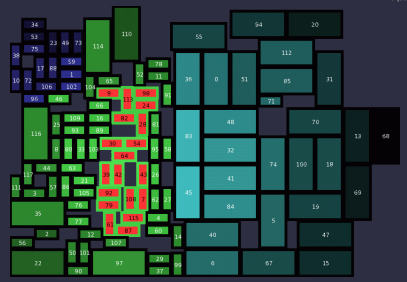










Review

- What are t_{su} and t_h?
- Define
  - Level-sensitive.
  - Edge-triggered.
  - Latch.
  - Flip-flop.
- What is the symbol for a falling edge triggered D flip-flop?
- Show a circuit design for a Schmitt-trigger inverter.

Derive and explain.

Distributed loads and Elmore delay

Derive the propagation delay of an aluminum wire that is 2 cm long and 500 nm wide. Does using a lumped model introduce significant error? You may assume a sheet resistance of $0.075\,\Omega/\square$. Derive the propagation delay of a copper wire with the same shape. State, and verify, any assumptions.

Derive and explain.

More on transistor sizing

$$f(a, b, c) = \overline{ab + c}$$

Derive and explain.

Lecture plan

1. Memory array structures
2. Dynamic random access memory
3. Homework

Volatile memory

- SRAM cell and architecture overview.
- DRAM cell and architecture overview.

Non-volatile memory

- ROM.
- EPROM.
- EEPROM.
- Flash.

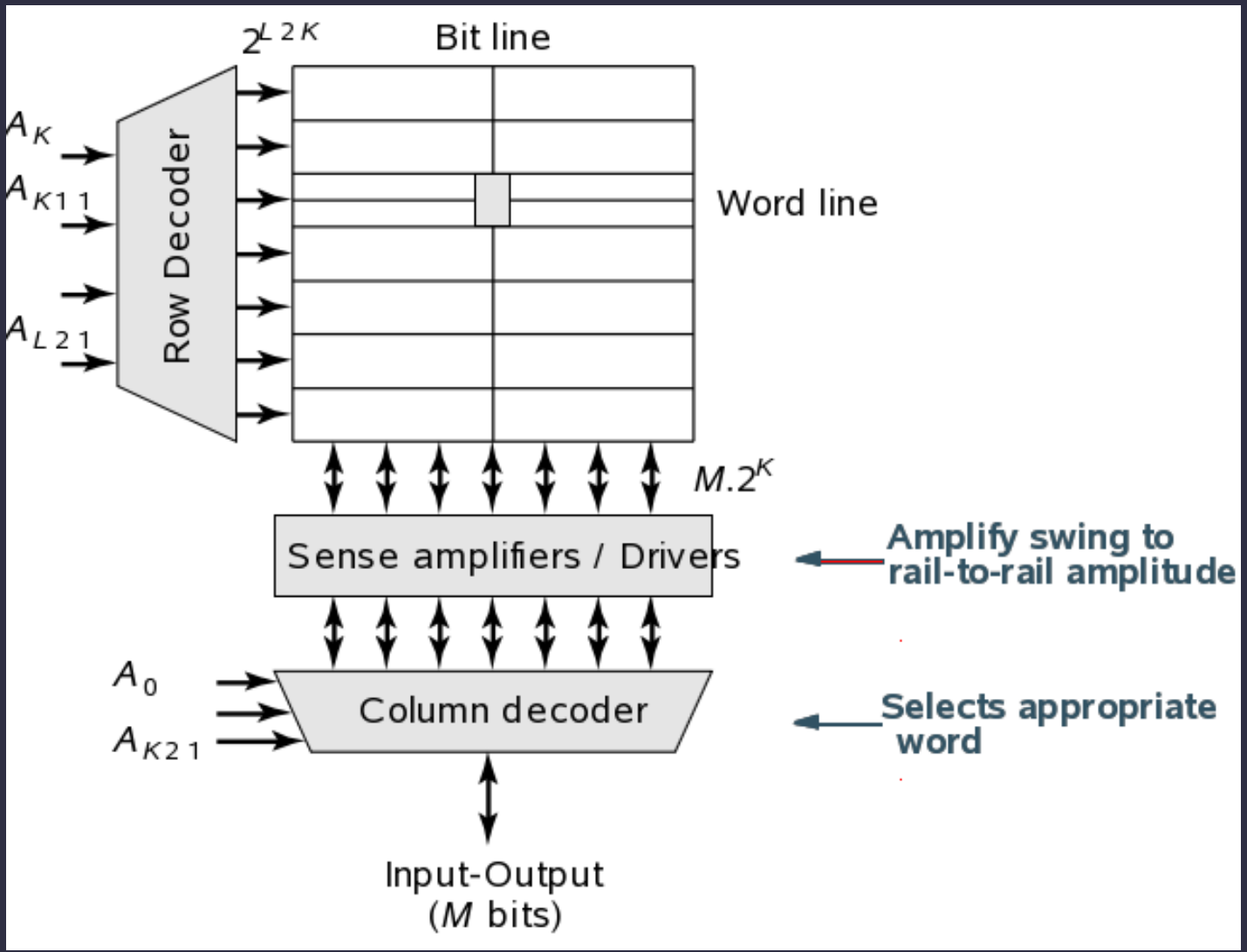
Floating gate technology

- UV erase.
- Electrical erase.
- Block erase.

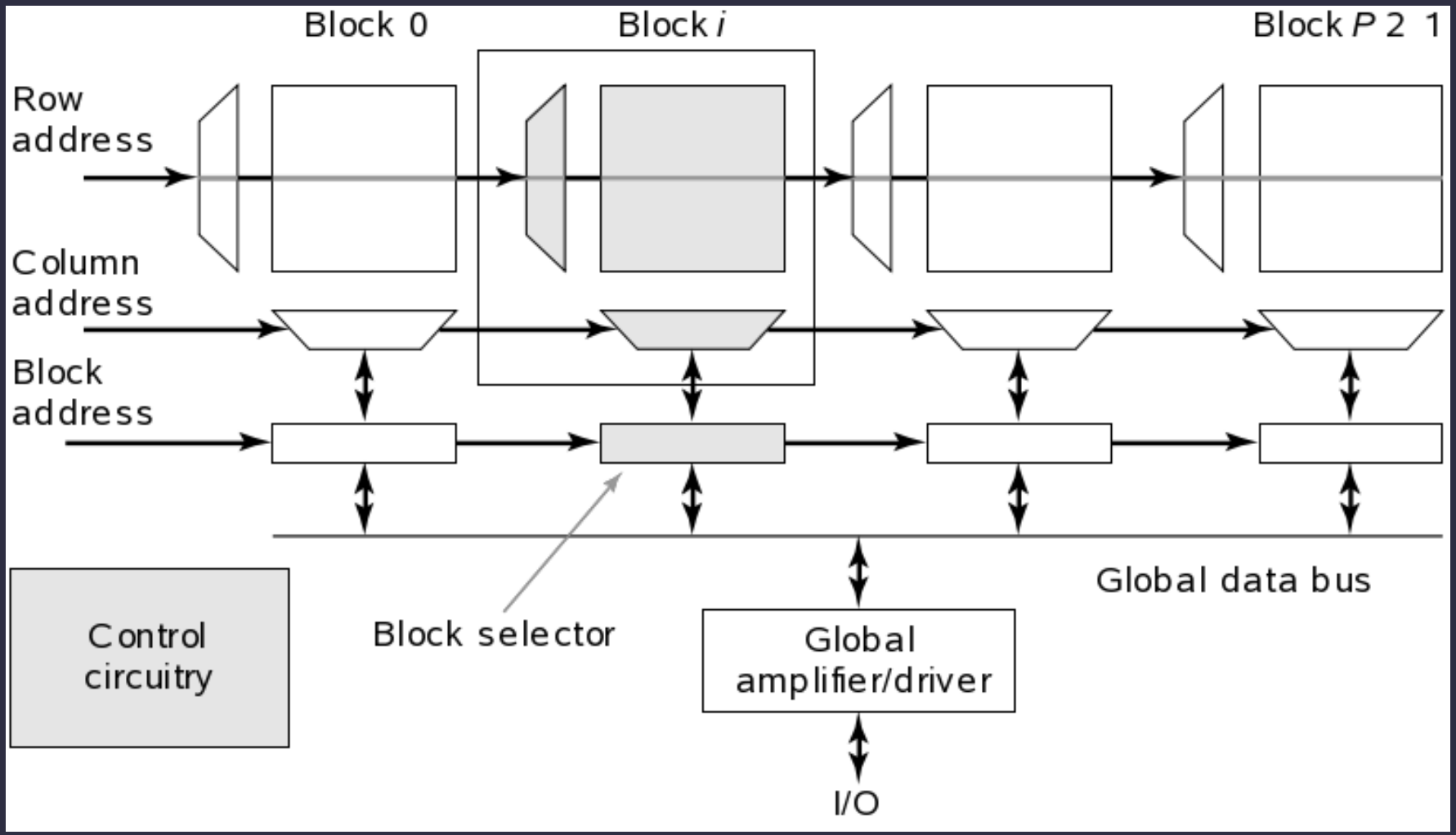
Hot floating gate implementation

- Was once difficult to design uniform-thickness thin oxide layers.
- Tunneling-based programming was difficult.
- Avalanche injection (hot electron) based programming used.
- UV erasure.
- Pure tunneling later became practical (EEPROM).
- Flash uses hot electrons for programming and tunneling for erasing.

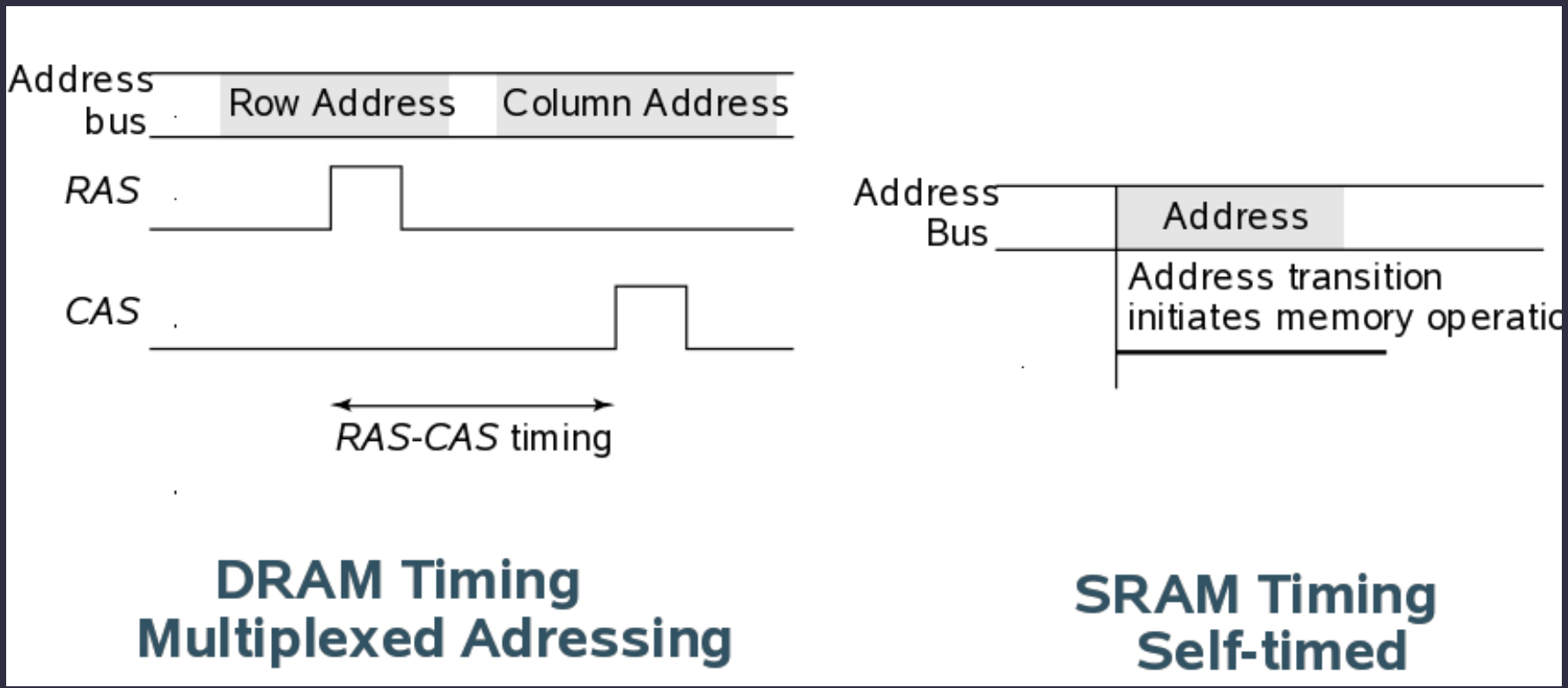
Array memory architecture



Block-based memory architecture



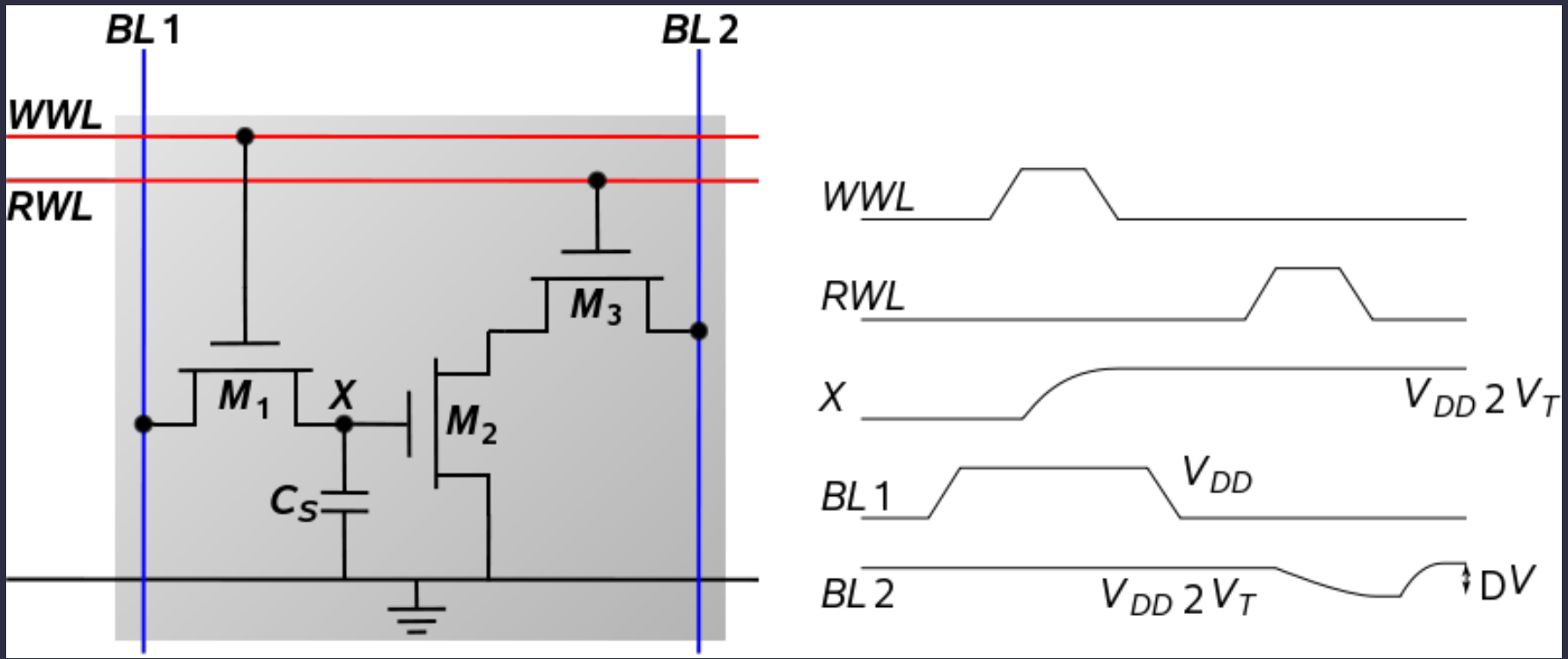
Memory timing



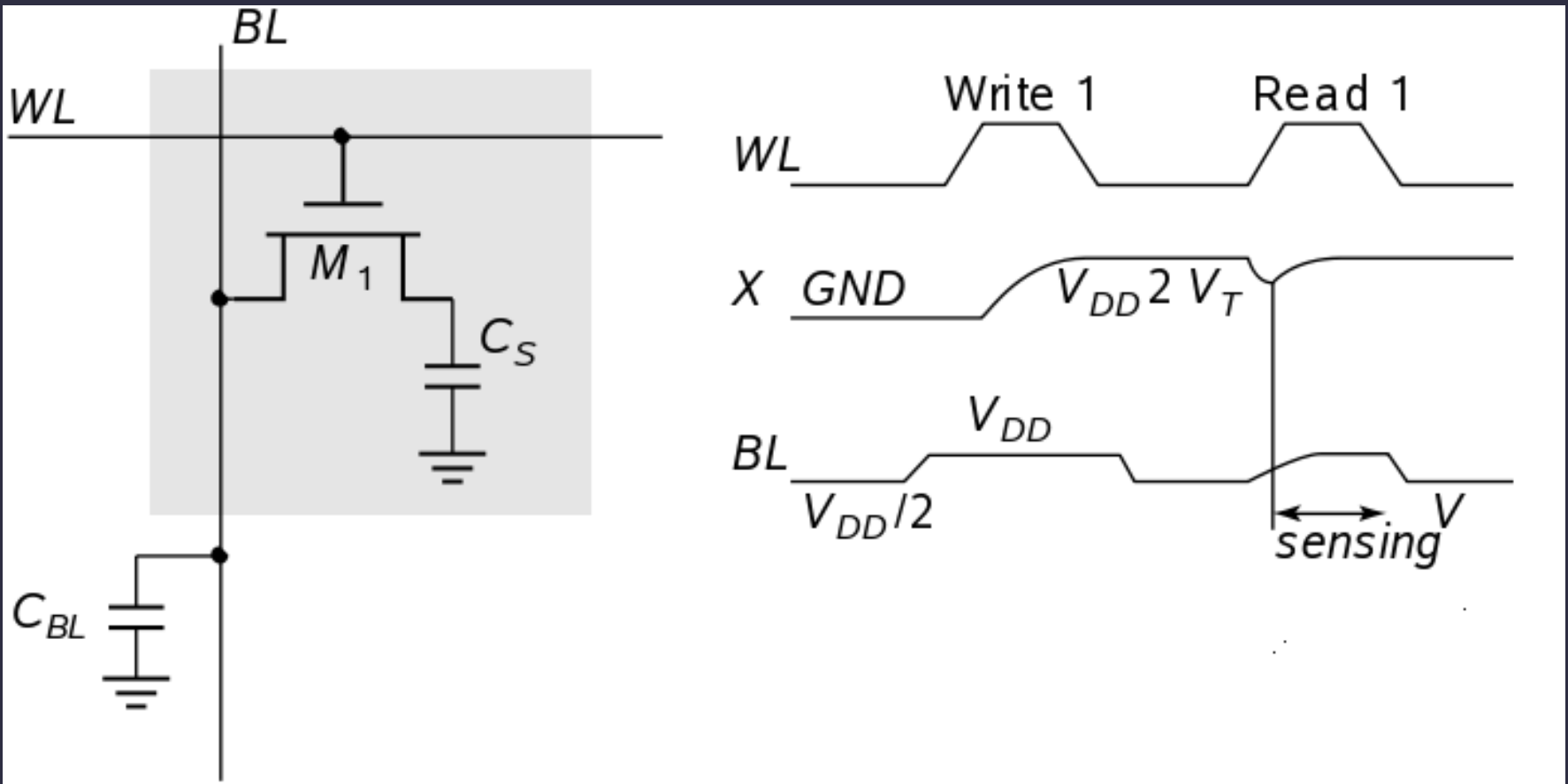
Lecture plan

1. Memory array structures
2. Dynamic random access memory
3. Homework

DRAM

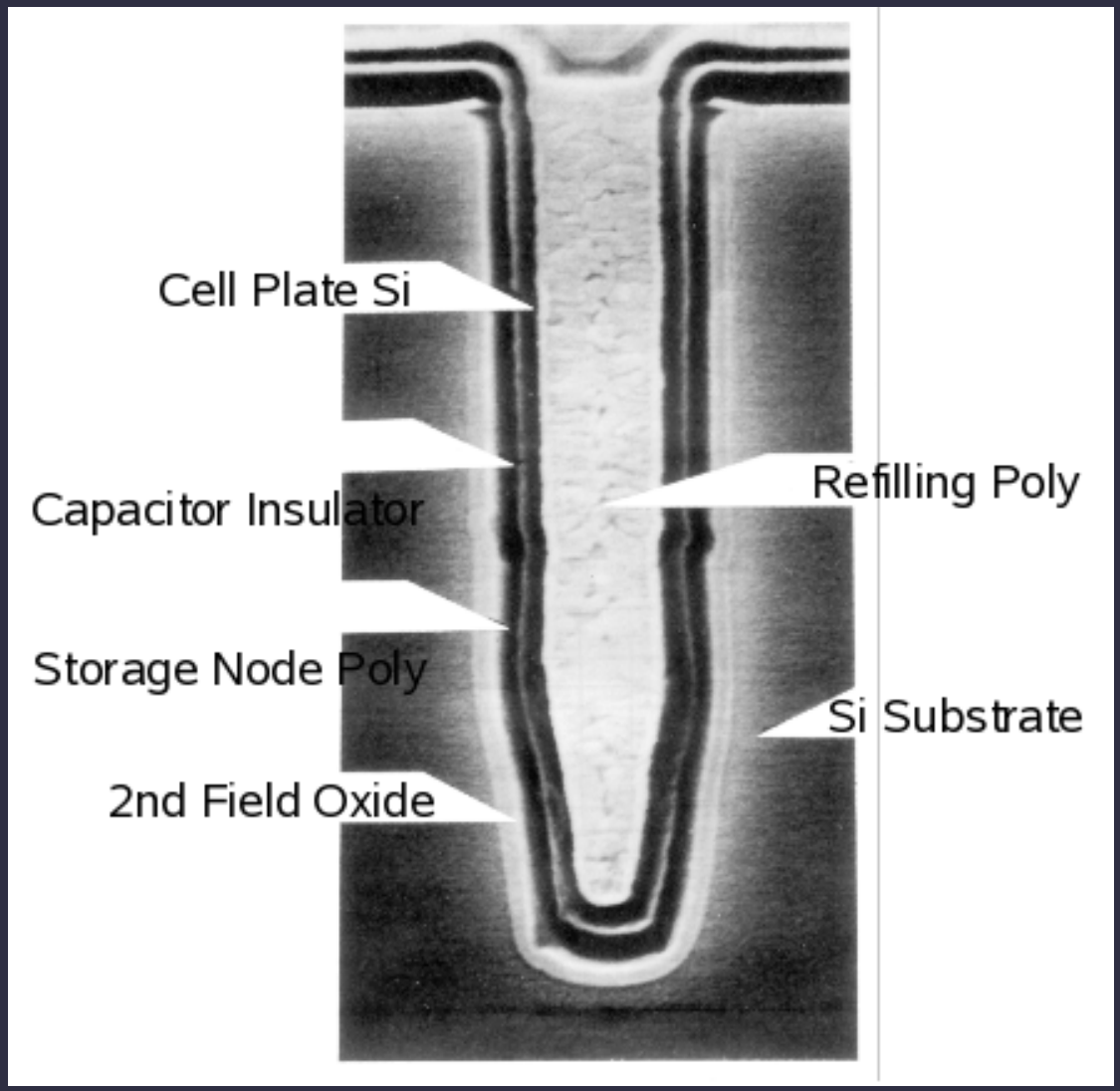

BL 1
BL 2
WWL
RWL
M3
M1
X
M2
CS
WWL
RWL
X
VDD 2 VT
BL 1
VDD
BL 2
VDD 2 VT
DV

DRAM



Write: C_S is charged or discharged by asserting WL and BL.

DRAM side view



Upcoming topics

- Sequential circuits.

Lecture plan

1. Memory array structures
2. Dynamic random access memory
3. Homework

Homework, deadlines, and schedule

- 25 November, Thursday: Office hours from 3:00–4:30. Call-ins and skype-ins welcome.
- 30 November, Tuesday: Read Section 12.2 in J. Rabaey, A. Chandrakasan, and B. Nikolic. *Digital Integrated Circuits: A Design Perspective*. Prentice-Hall, second edition, 2003.
- 2 December, Thursday: Midterm exam.
- 10 December, Friday: Final project due (will post on 24 November).
- Any time: Review homework problems will be marked, but not graded (will post by 10 December).

Special topic: Optical interconnect

Guanyu and Haishan.