Digital Integrated Circuits – EECS 312

http://ziyang.eecs.umich.edu/~dickrp/eecs312/

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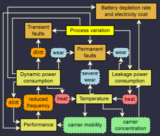
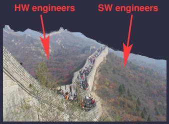
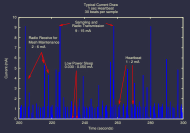
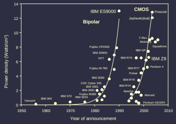
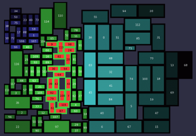










Lab 4

- Can assume first stage is like an inverter, then experiment.
- A few simulation runs are fine.
- Not expecting exhaustive search.
- Capacitance of first gate? Can assume that $\gamma = 1$.
  - If not clear, email discussion list today so Mr. Kim and I know to make more suggestions.

Derive and explain.

Review

- What is charge sharing?
- Why are there two different expressions for the voltage to which V_{out} settles?
- Is leakage a significant factor in charge sharing?
- How can it be prevented?
- What is volatile memory?
- What is non-volatile memory?
- What is static memory?
- What is dynamic memory?

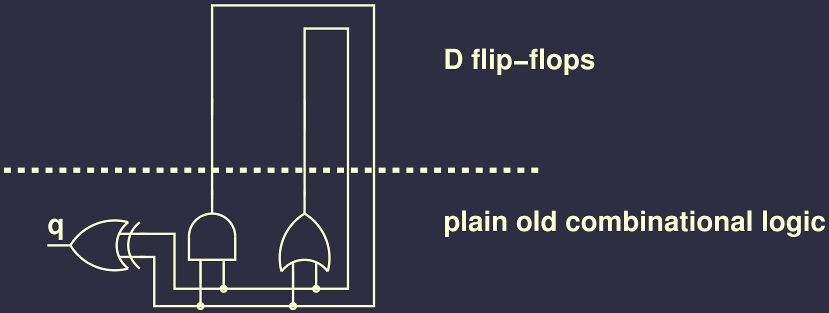
Derive and explain.

Lecture plan

1. Latches and flip-flops
2. Homework

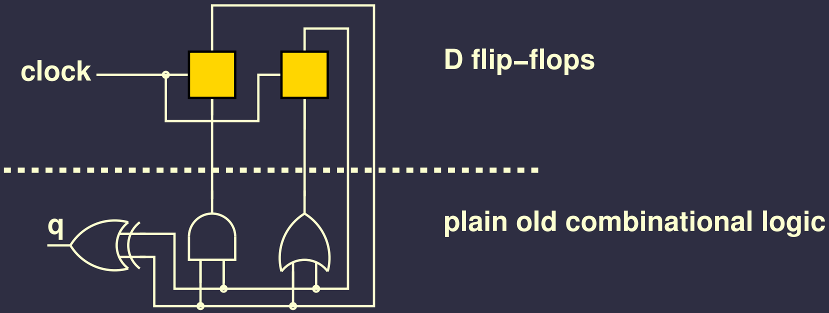
Combinational vs. sequential logic

- No feedback between inputs and outputs – combinational
  - Outputs a function of the current inputs, only



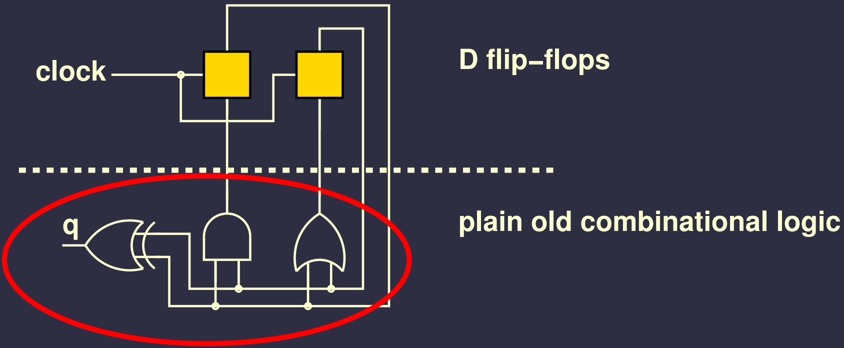
Combinational vs. sequential logic

- No feedback between inputs and outputs – combinational
  - Outputs a function of the current inputs, only
- Feedback – sequential



Combinational vs. sequential logic

- No feedback between inputs and outputs – combinational
  - Outputs a function of the current inputs, only



Sequential logic

- Outputs depend on current state and (maybe) current inputs
- Next state depends on current state and input
- For implementable machines, there are a finite number of states
- Synchronous
  - State changes upon clock event (transition) occurs
- Asynchronous
  - State changes upon inputs change, subject to circuit delays

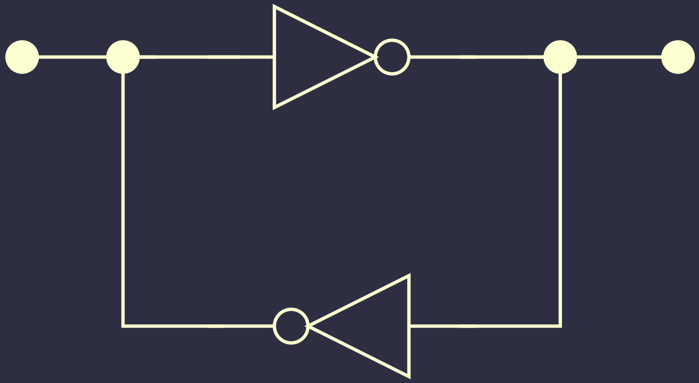
Flip-flop introduction

- Stores, and outputs, a value.
- Puts a special clock signal in charge of timing.
- Allows output to change in response to clock transition.
- More on this later.
  - Timing and sequential circuits

Introduction to sequential elements

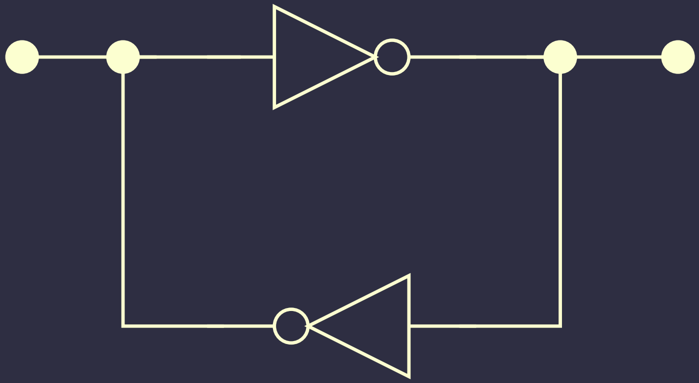
- Feedback and memory.
- Memory.
- Latches.

Feedback and memory



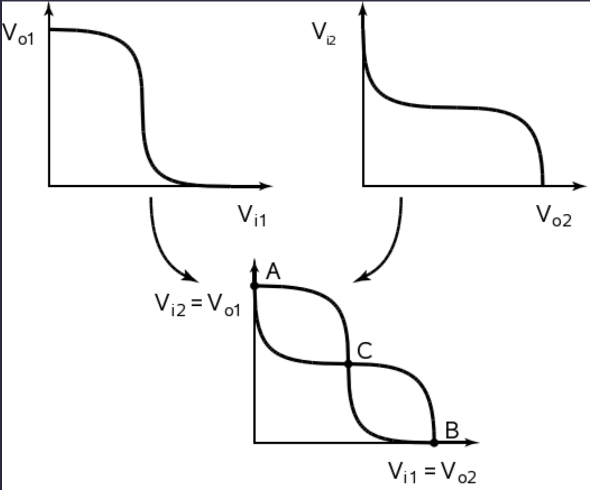
- Feedback or physical state are the root of memory.
- Can compose a simple loop from inverters.

Feedback and memory

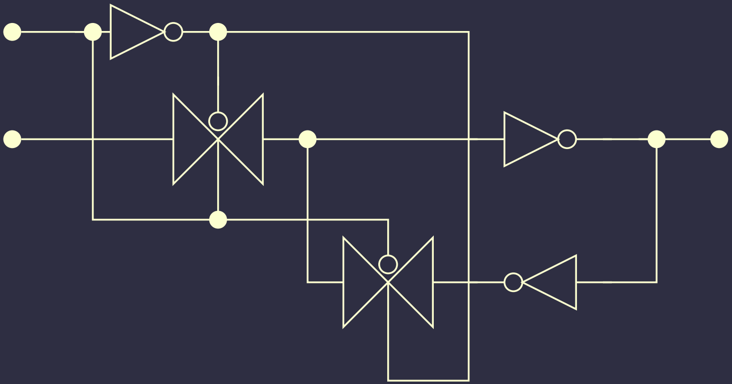


- Feedback or physical state are the root of memory.
- Can compose a simple loop from inverters.
- However, there is no way to switch the value.

Bistability

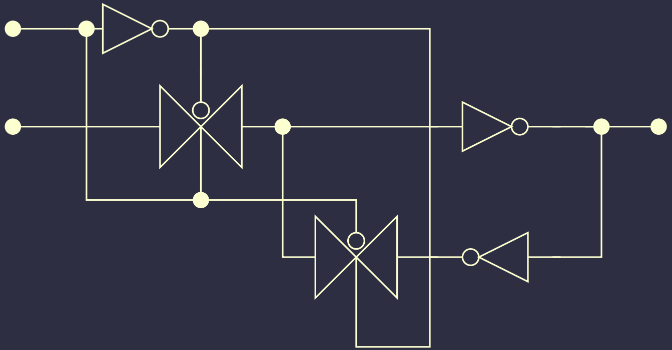


TG and NOT-based memory



- Can break feedback path to load new value
- However, potential for timing problems

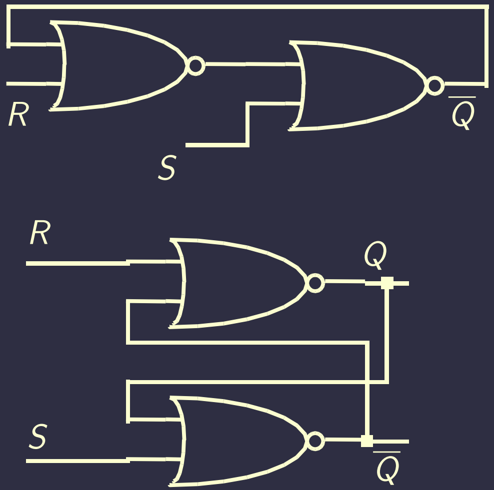
One-bit volatile cell



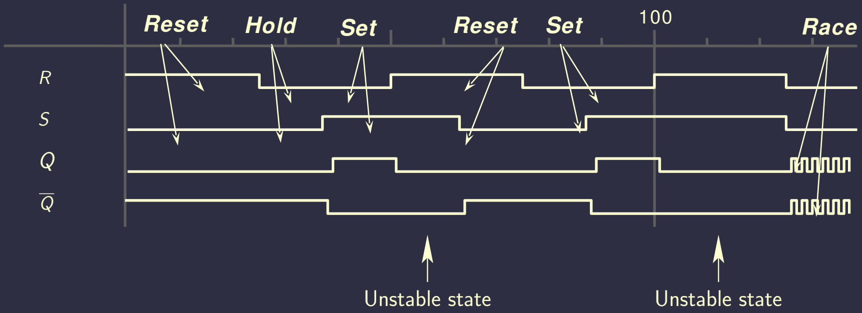
- Can break feedback path to load new value.
- How can this be made more efficient?
- Resize transistors, remove transistors, use state?

Section outline

Reset/set latch

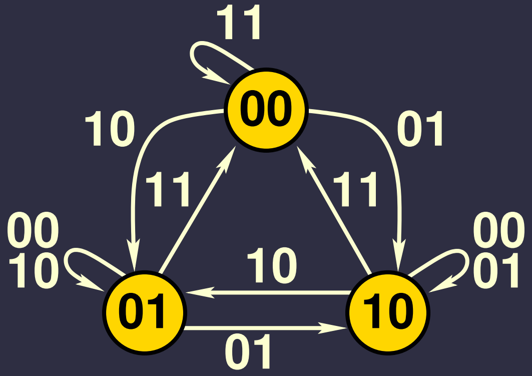


Reset/set timing

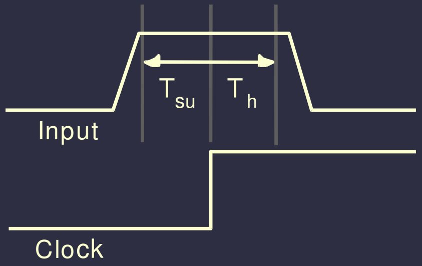


RS latch state diagram

output=$Q\ \overline{Q}$
input=$R\ S$

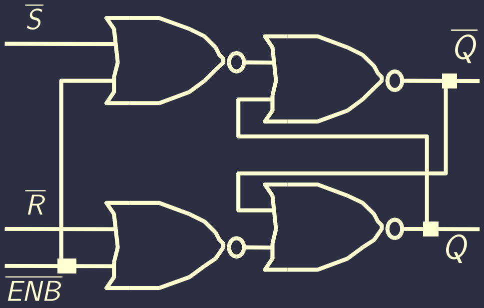


Clocking terms

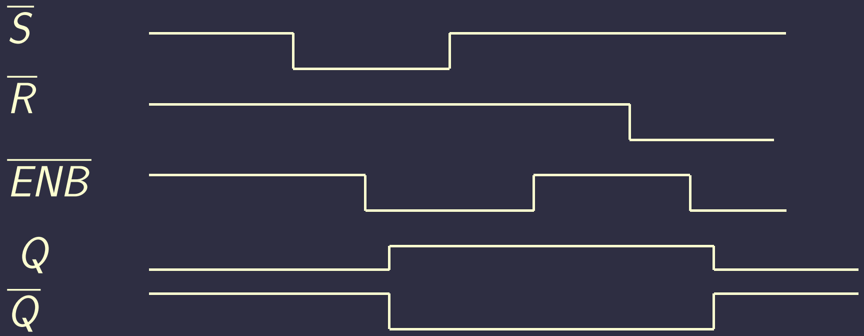


- Clock – Rising edge, falling edge, high level, low level, period
- Setup time: Minimum time before clocking event by which input must be stable (T_{SU})
- Hold time: Minimum time after clocking event for which input must remain stable (T_H)
- Window: From setup time to hold time

Gated RS latch



Gated RS latch



Memory element properties

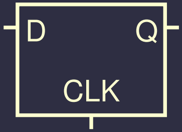
Type	Inputs sampled	Outputs valid
Unclocked latch	Always	LFT
Level-sensitive latch	Clock high (T_{SU} to T_H) around falling clock edge	LFT
Edge-triggered flip-flop	Clock low-to-high transition (T_{SU} to T_H) around rising clock edge	Delay from rising edge

Section outline

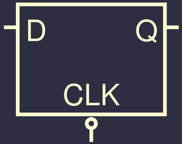
1. Latches and flip-flops
    - Reset/set latches
    - Clocking conventions
    - D flip-flop
    - Other memory elements

Clocking conventions

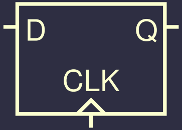
Active–high transparent



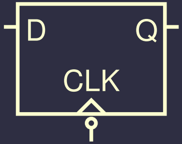
Active–low transparent



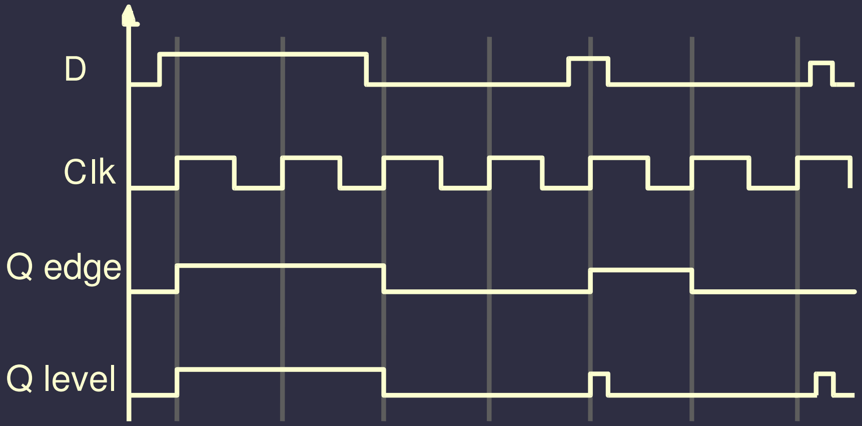
Positive (rising) edge



Negative (falling) edge



Timing for edge and level-sensitive latches

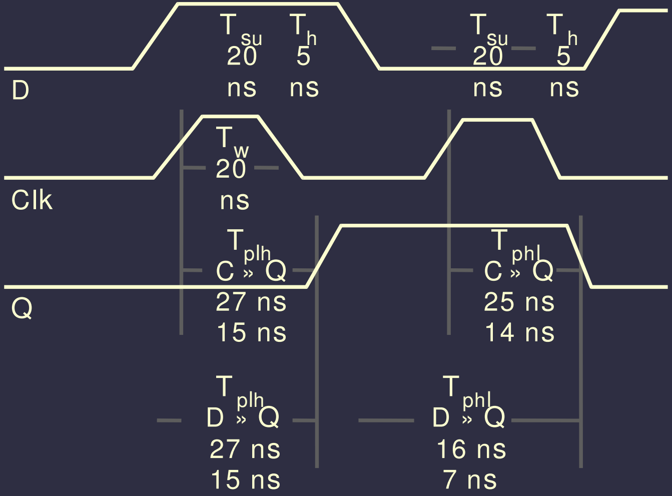


Latch timing specifications

- Minimum clock width, T_W
  - Usually period / 2
- Low to high propegation delay, P_{LH}
- High to low propegation delay, P_{HL}
- Worst-case and typical

Latch timing specifications

Example, negative (falling) edge-triggered flip-flop timing diagram

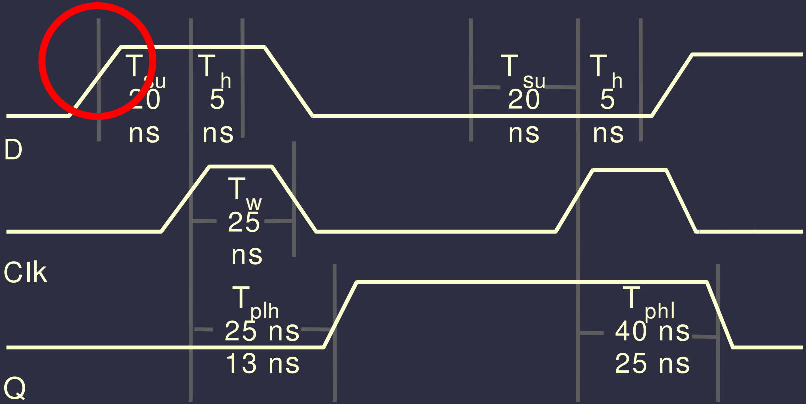


FF timing specifications

- Minimum clock width, T_W
  - Usually period / 2
- Low to high propagation delay, P_{LH}
- High to low propagation delay, P_{HL}

FF timing specifications

Example, positive (rising) edge-triggered flip-flop timing diagram



RS latch states

S	R	Q^+	$\overline{Q}^+$	Notes
0	0	Q	$\overline{Q}$	
0	1	0	1	
1	0	1	0	
1	1	1	1	unstable

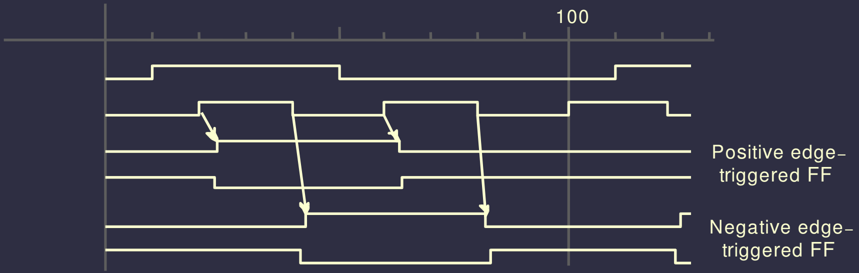
Section outline

1. Latches and flip-flops
   - Reset/set latches
   - Clocking conventions
   - D flip-flop
   - Other memory elements

Falling edge-triggered D flip-flop

- Use two stages of latches
- When clock is high
  - First stage samples input w.o. changing second stage
  - Second stage holds value
- When clock goes low
  - First stage holds value and sets or resets second stage
  - Second stage transmits first stage
- $Q^+ = D$
- One of the most commonly used flip-flops

Edge triggered timing



RS clocked latch

- Storage element in narrow width clocked systems.
- Dangerous.
- Fundamental building block of many flip-flop types.

D flip-flop

- Minimizes input wiring.
- Simple to use.
- Common choice for basic memory elements in sequential circuits.

Toggle (T) flip-flops

- State changes each clock tick
- Useful for building counters
- Can be implemented with other flip-flops
  - D with XOR feedback

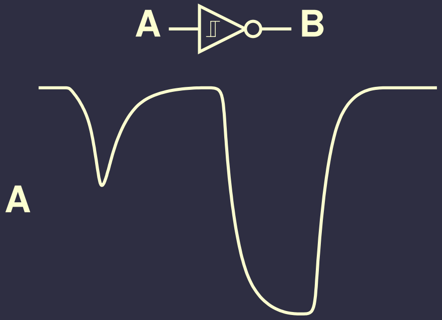
Asynchronous inputs

- How can a circuit with numerous distributed edge-triggered flip-flops be put into a known state?
- Could devise some sequence of input events to bring the machine into a known state.
  - Complicated.
  - Slow.
  - Not necessarily possible, given trap states.
- Can also use sequential elements with additional asynchronous reset and/or set inputs.

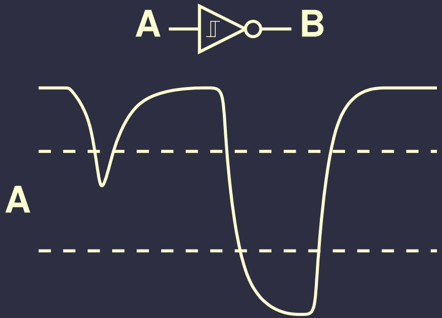
Section outline

1. Latches and flip-flops
   - Reset/set latches
   - Clocking conventions
   - D flip-flop
   - Other memory elements

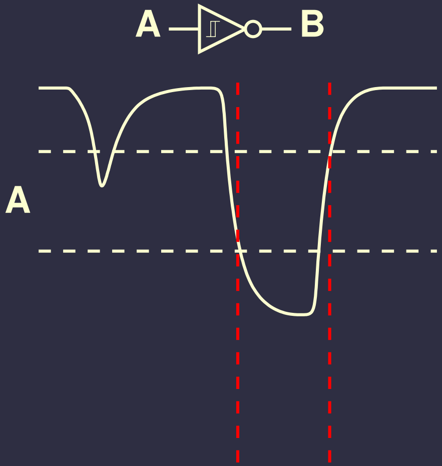
Schmitt triggers



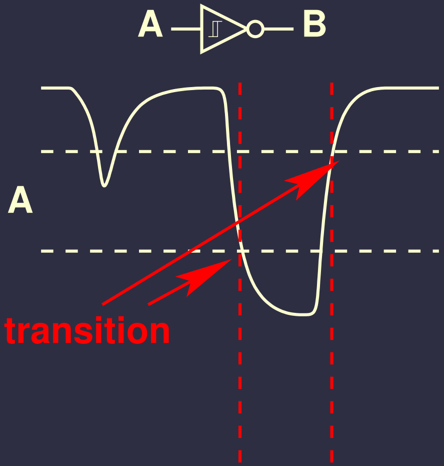
Schmitt triggers



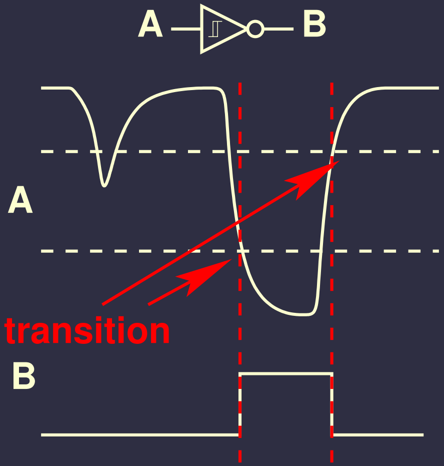
Schmitt triggers



Schmitt triggers



Schmitt triggers



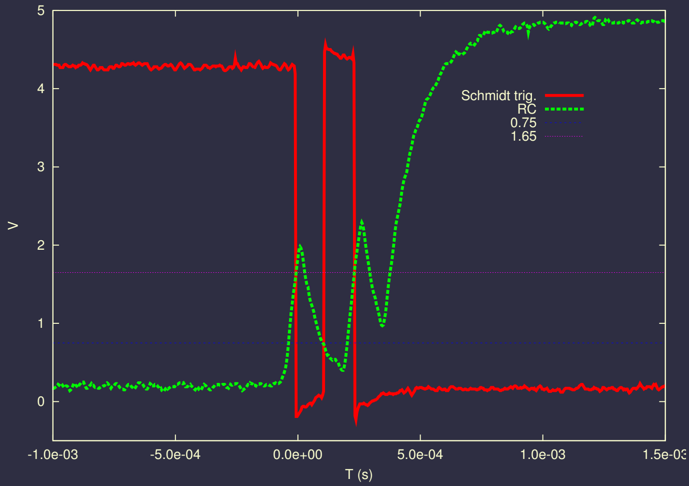
Reason for gradual transition

- A logic stage is an RC network
- Whenever a transition occurs, capacitance is driven through resistance
- Consider the implementation of a CMOS inverter

Debouncing

- Mechanical switches bounce!
- What happens if multiple pulses?
  - Multiple state transitions
- Need to clean up signal

Debouncing


5
4
3
2
1
0
V
-1.0e-03
-5.0e-04
0.0e+00
5.0e-04
1.0e-03
1.5e-03
T (s)
Schmidt trig.
RC
0.75
1.65

Latch and flip-flop equations

RS

$$Q^+ = S + \overline{R}\ Q$$

D

$$Q^+ = D$$

T

$$Q^+ = T \oplus Q$$

Upcoming topics

- Sequential circuits.
- Theoretical foundations for sizing.

Lecture plan

1. Latches and flip-flops
2. Homework

Homework assignment

- 22 November, Monday: Lab 4.
- 23 November, Tuesday: Read Sections 12.1 in J. Rabaey, A. Chandrakasan, and B. Nikolic. *Digital Integrated Circuits: A Design Perspective*. Prentice-Hall, second edition, 2003.
- 30 November, Tuesday: Read Sections 12.2 in J. Rabaey, A. Chandrakasan, and B. Nikolic. *Digital Integrated Circuits: A Design Perspective*. Prentice-Hall, second edition, 2003.

Special topic: Subthreshold circuit applications

Megan and Tyler.