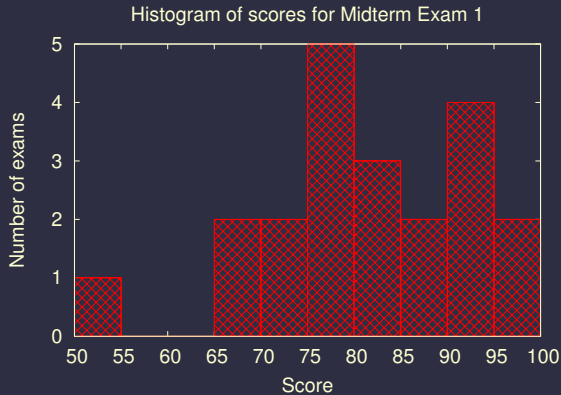




# Midterm exam 1 I



# Midterm exam 1 II

Average: 80%.

## Common problems

- 1 Trouble interpreting layout: We can work on this a bit more in help sessions and class.
- 2 Maybe not enough time understanding some of the questions.  
Question: Was there a lot of time pressure?
- 3 Option: How about another short midterm after Thanksgiving break?
  - Advantage: Less time pressure on final exam.
  - Advantage: Less probability of a “bad day” messing up course score.
  - Disadvantage: More stress and work.

# Homework 3 walkthrough

Derive and explain.

## Review

- When are the advantages and disadvantages of fixed-voltage charging?
- When are the advantages and disadvantages of fixed-current charging?
- In what situation is each of the following models important?
  - Ideal.
  - $C$ .
  - $RC$ .
  - $RLC$ .
- What are  $di/dt$  effects? Under what circumstances do they cause the most trouble?

Derive and explain.

# Lecture plan

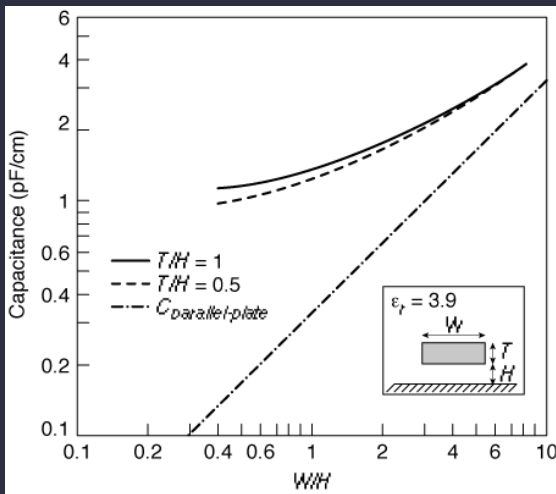
1. Interconnect: Rent's rule and coupling capacitance
2. Elmore delay modeling
3. Logic design
4. Homework

## Rent's rule

$$T = ak^p$$

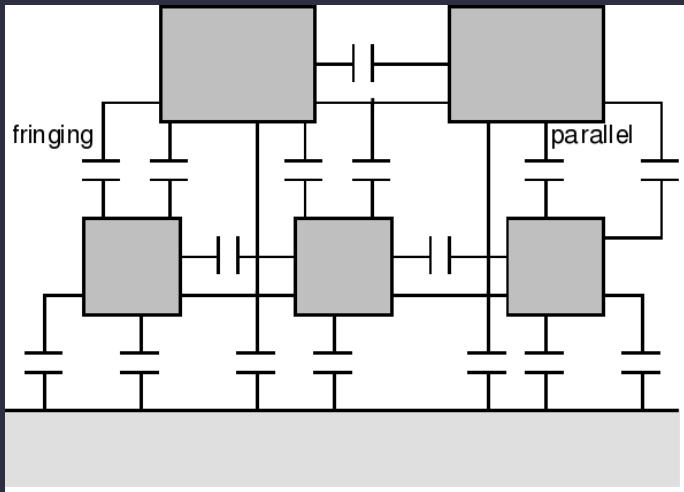
- $T$ : Number of terminals.
- $a$ : Average number of terminals per block.
- $k$ : Number of blocks within chip.
- $p$ : Rent's exponent,  $\leq 1$ , generally around 0.7.

## Fringe vs. parallel plate capacitance

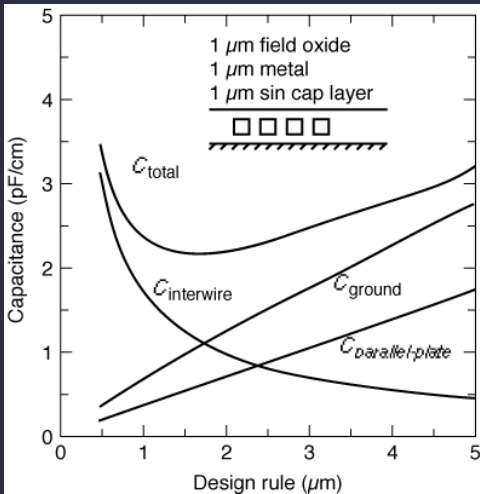


Plot of  $C_{total}$  for different gap ratios.

## Inter-wire capacitance



## Impact of inter-wire capacitance



## Wire resistance

- $R = \frac{\rho L}{HW}$ .
- Consider fixed-height, fixed- $\rho$  square material, i.e.,  $L \propto W$ .
- $R = k \frac{1}{W}$ , where  $k$  is a constant.

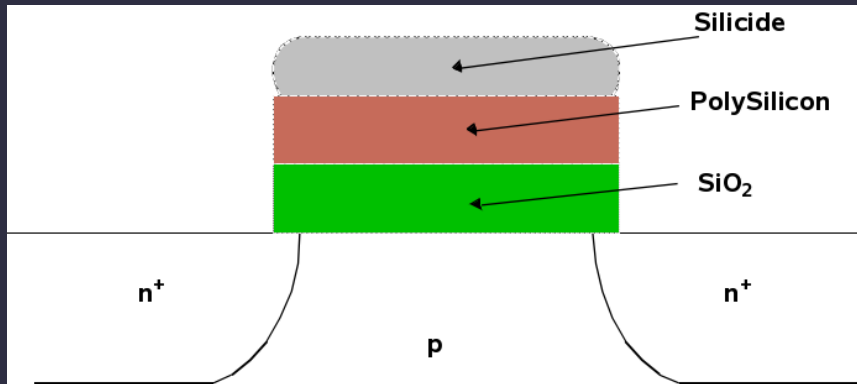
## Interconnect resistance

Material	$\rho$ ( $\Omega$ m) $\times 10^{-8}$
Silver	1.6
Copper	1.7
Gold	2.2
Aluminum	2.7
Tungsten	5.5

# Reducing resistance

- Higher interconnect aspect ratios
- Material selection
  - Copper
  - Silicides
  - Carbon nanotubes
- Structural changes
  - More interconnect layers
  - 3-D integration

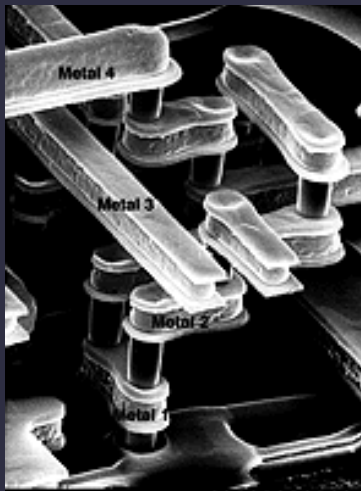
# Silicides



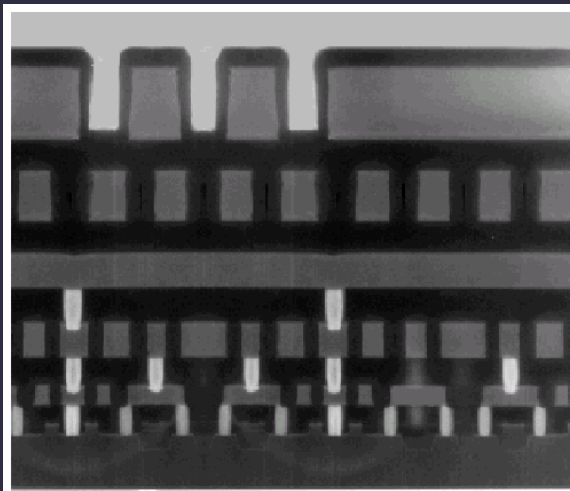
# Resistances

Material	Sheet resistance ( $\Omega/\square$ )
n- or p-well diffusion	1,000–1,500
n <sup>+</sup> or p <sup>+</sup> diffusion	50–150
silicided n <sup>+</sup> or p <sup>+</sup> diffusion	3–5
doped polysilicon	150–200
doped silicides polysilicon	4–5
Aluminum	0.05–0.1

## Multi-layer interconnect



## Side view of interconnect



## Interconnect summary

- It is important to know which interconnect model to use in which situation.
  - Ideal.
  - $C$ .
  - $RC$ .
  - $RLC$ .
- $dl/dt$  effects are particularly important in power delivery networks.
- Capacitive coupling complicates design.
- Cu and silicides can be used to reduce resistance.

# Lecture plan

1. Interconnect: Rent's rule and coupling capacitance
2. Elmore delay modeling
3. Logic design
4. Homework

# Delay modeling

- Single-node lumped model inaccurate.
- Full detailed accurate model intractable for manual analysis and slow for automated analysis.
- Elmore delay model permits rapid analysis with often adequate accuracy.

# Elmore delay

## Problem definition

- Goal: Determine  $\tau$  for RC path.
- Note: Source node is implicit.
- $C_i$ : Self-capacitance of node  $i$ .
- $R_{ij}$ : Path resistance from source to node  $i$ .
- $R_{ik}$ : Shared resistance from source to both nodes  $i$  and  $k$ .

$$\tau_i = \sum_{k=1}^N C_k R_{ik}$$

Derive and explain.

## Special case: RC chains

- Consider  $\pi$  network.
- $\tau_n = \sum_{i=1}^n C_i \sum_{j=1}^i R_j$ .
- Use homogeneous discretization.
- $\forall_{i=2}^N C_i = C_1$

$$\begin{aligned}\tau &= \sum_{k=1}^N CR_{nk} \\ &= \frac{L}{N} C \frac{L}{N} r \frac{N(N+1)}{2} \\ &= rcL^2 \frac{N+1}{2N}\end{aligned}$$

What if  $N \rightarrow \infty$ ?  $\tau \rightarrow rcL^2/2$ .

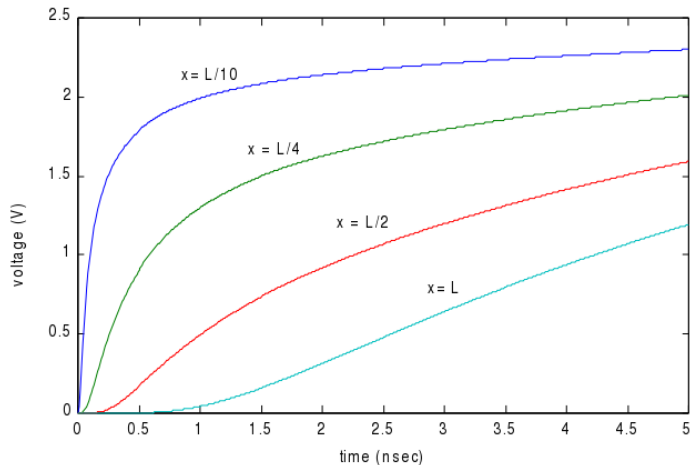
## Underlying continuous physical model

$$cr \frac{\delta V}{\delta t} = \frac{\delta^2 V}{\delta x^2}$$

## Power delivery network considerations

- IR drop.
- $di/dt$  effects.
- Location of parasitic inductance.
- Methods to correct power delivery network non-idealities.

## Response to step function over time and space



## Simplifying assumptions

- Ignore wire RC delay when wire delay does not much exceed that of the driving gate, i.e.,

$$L_{crit} \gg \sqrt{\frac{t_{p,gate}}{0.38rc}}$$

- Ignore wire RC when rise time greater than RC delay.
- Ignore for high-resistance wires:  $R > 0.2C$ .
- Ignore when time of flight is large compared to rise or fall time:  
 $t_{rise,fall} < 2.5t_{flight}$ .

## Elmore delay summary

- Pick simplest model for intended purpose:  $C$ ,  $RC$ , or  $RLC$ .
- Capacitive coupling complicates timing analysis.
- Transition direction impacts  $C$  magnitude in simplified ground-cap model.
- Learn Elmore delay. It is a good first-order approximation of network delay.

# Lecture plan

1. Interconnect: Rent's rule and coupling capacitance
2. Elmore delay modeling
3. Logic design
4. Homework

# Static CMOS design styles and components

- Logic gates
- Switch-based design
- MUX
- DEMUX
- Encoder
- Decoder

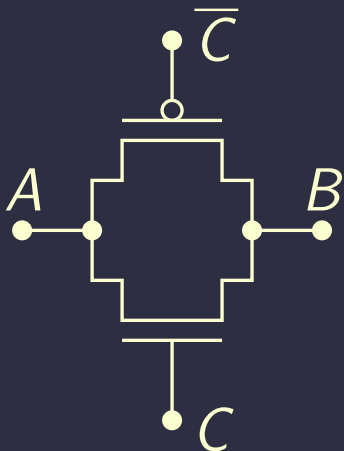
# Transistor sizing review

- Goal: equal  $\tau$  for worst-case pull-up and pull-down paths.
- Observations
  - Adding duplicate parallel path halves resistance.
  - Adding duplicate series path doubles resistance.
  - Doubling width halves resistance.
- Consider logic gate examples.

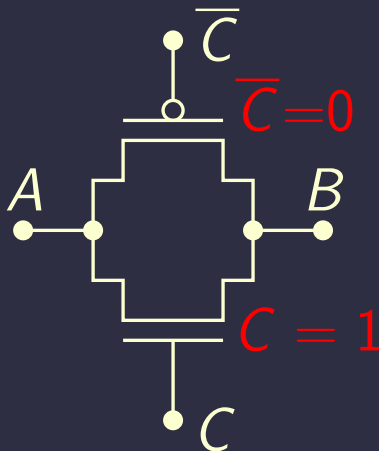
## Section outline

1. Introduction
2. Interconnect
3. Logic design
  - Switch-based design

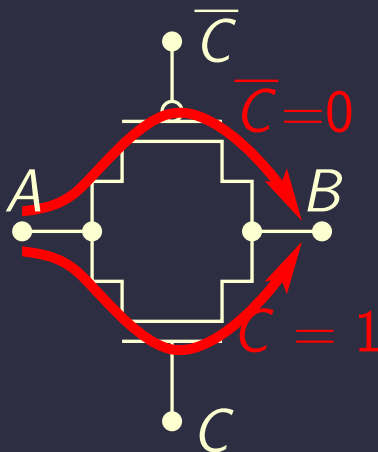
## CMOS transmission gate (TG)



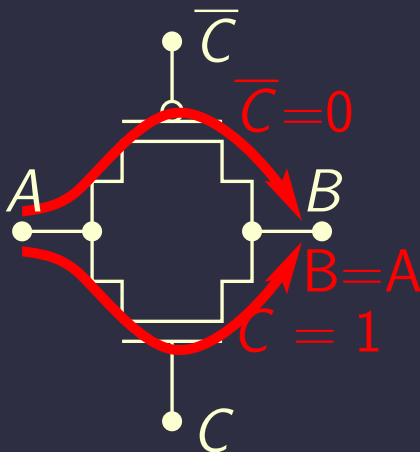
## CMOS transmission gate (TG)



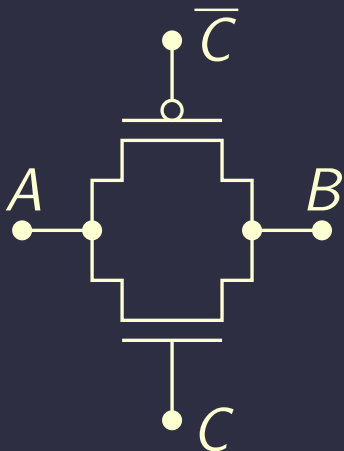
## CMOS transmission gate (TG)



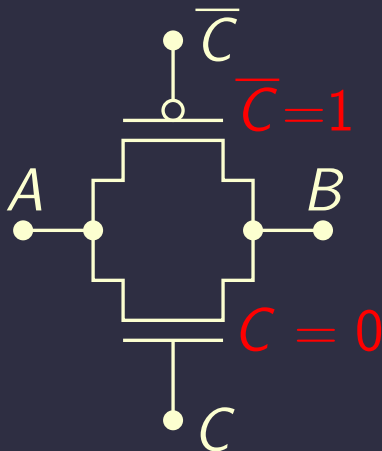
# CMOS transmission gate (TG)



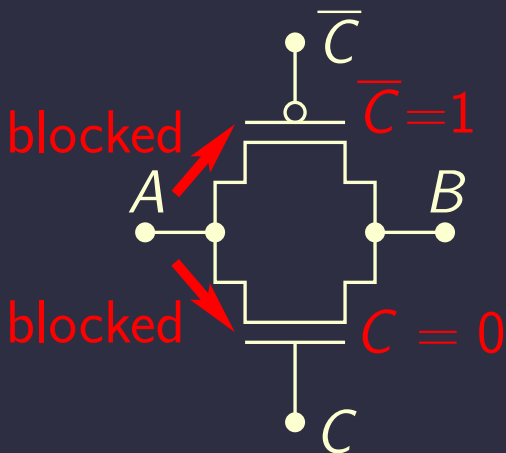
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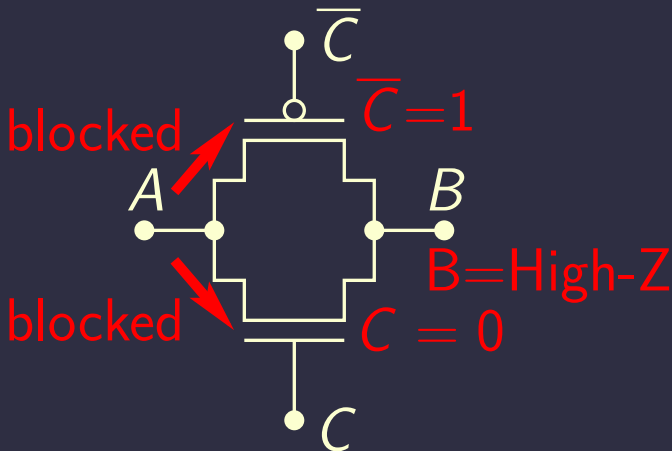
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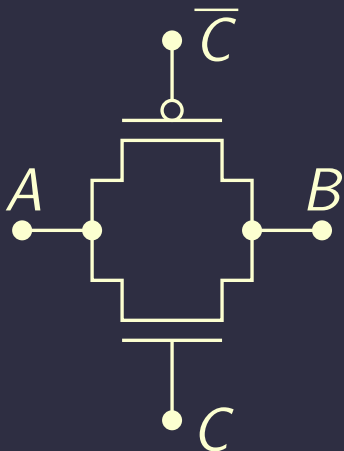
## CMOS transmission gate (TG)



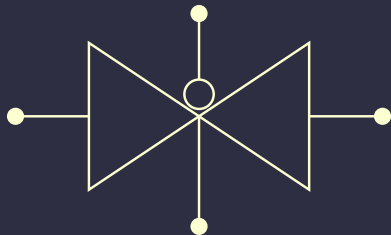
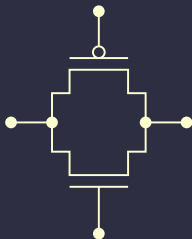
# CMOS transmission gate (TG)



## CMOS transmission gate (TG)



## Other TG diagram



# Multiplexer (MUX) definitions

- Also called *selectors*
- $2^n$  inputs
- $n$  control lines
- One output

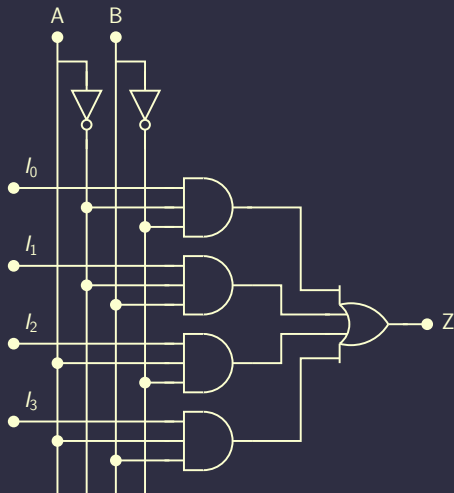
# MUX functional table

C	Z
0	$I_0$
1	$I_1$

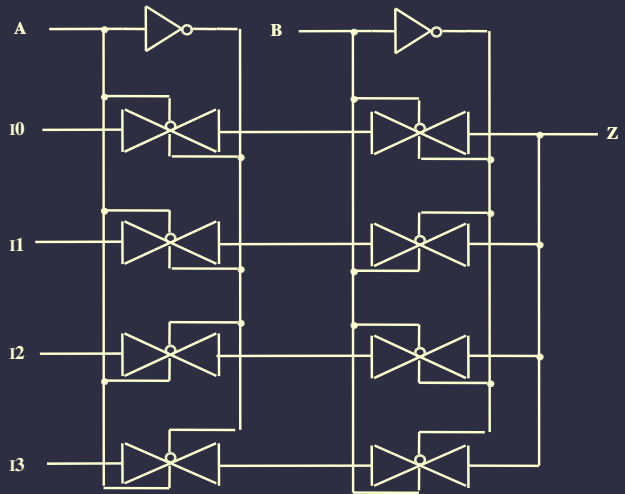
# MUX truth table

$I_1$	$I_0$	$C$	$Z$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

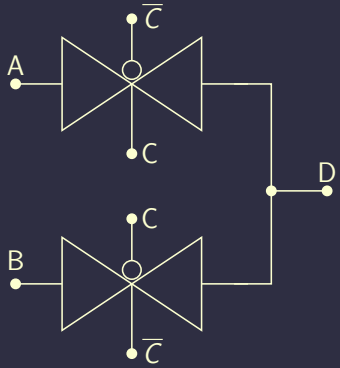
# MUX using logic gates



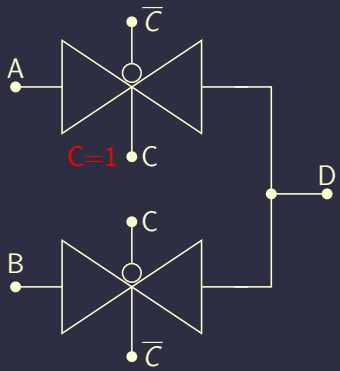
# MUX using TGs



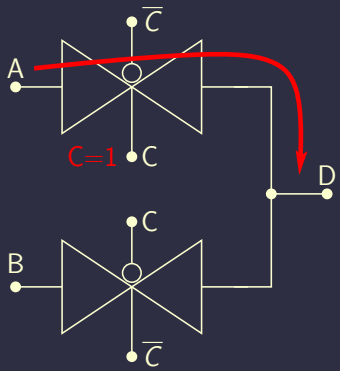
# MUX



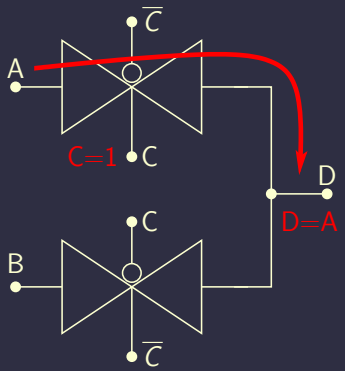
# MUX



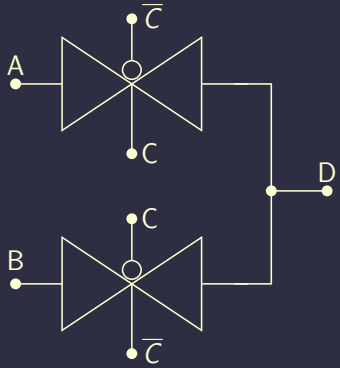
# MUX



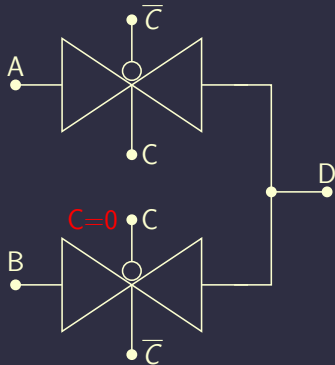
# MUX



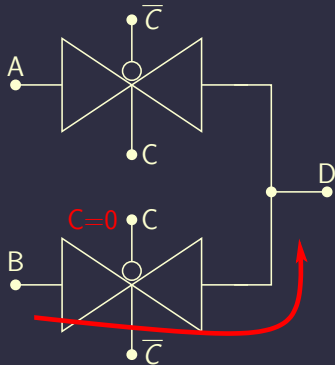
# MUX



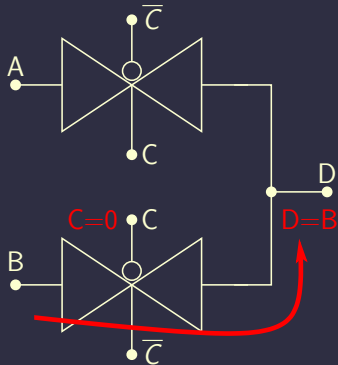
# MUX



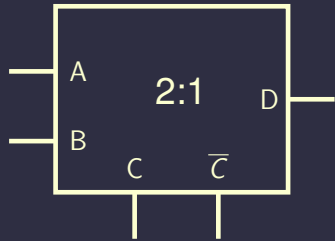
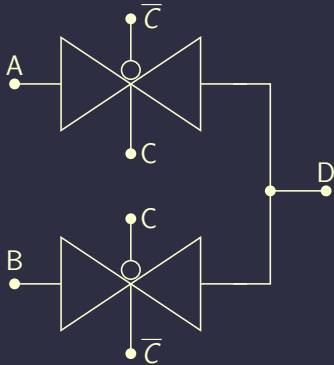
# MUX



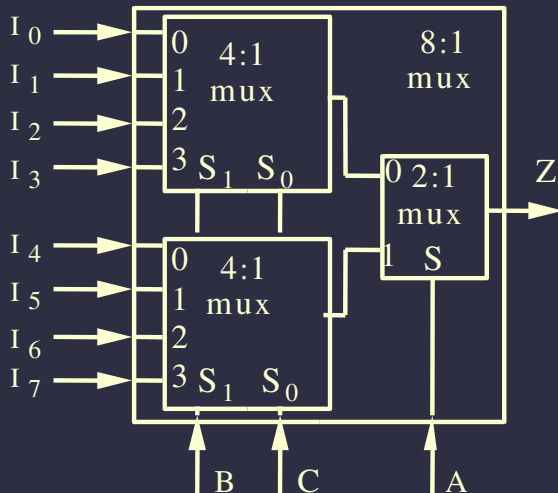
# MUX



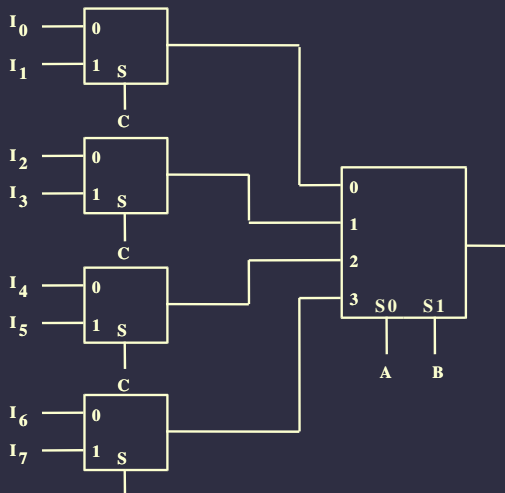
# MUX



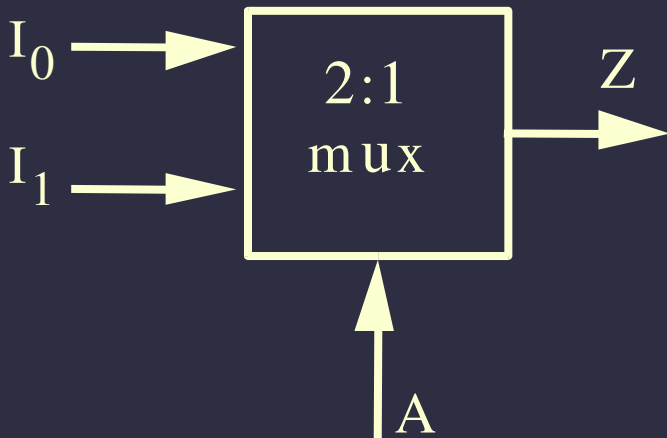
# Hierarchical MUX implementation



# Alternative hierarchical MUX implementation

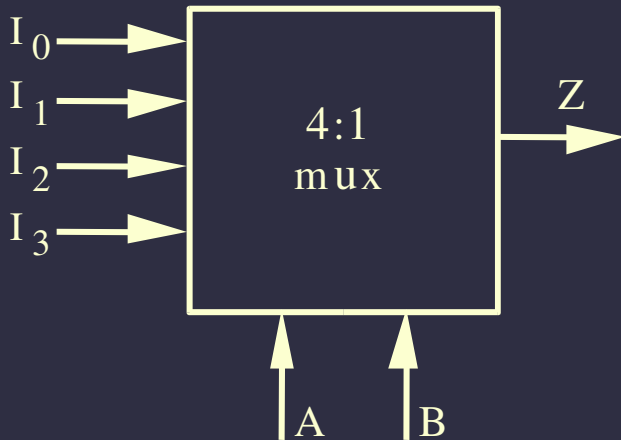


## MUX examples



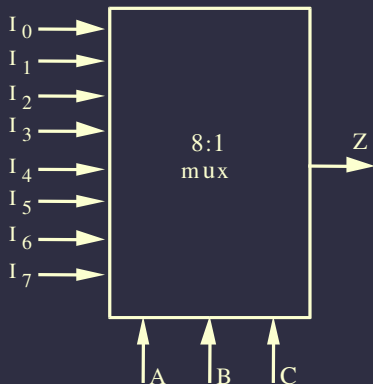
$$Z = \bar{A}I_0 + AI_1$$

## MUX examples



$$Z = \bar{A}\bar{B}I_0 + \bar{A}BI_1 + A\bar{B}I_2 + ABI_3$$

## MUX examples



$$Z = \bar{A}\bar{B}\bar{C}I_0 + \bar{A}\bar{B}CI_1 + \bar{A}B\bar{C}I_2 + \bar{A}BCI_3 + \\ AB\bar{C}I_4 + AB\bar{C}I_5 + ABC\bar{C}I_6 + ABCI_7$$

## MUX properties

- A  $2^n : 1$  MUX can implement any function of  $n$  variables
- A  $2^{n-1} : 1$  can also be used
  - Use remaining variable as an input to the MUX

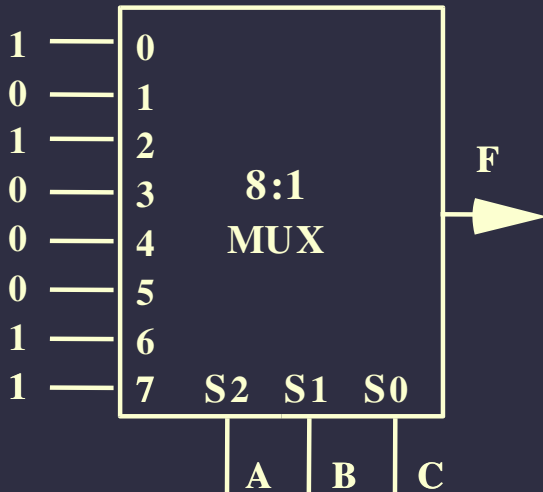
## MUX example

$$\begin{aligned} F(A, B, C) &= \sum(0, 2, 6, 7) \\ &= \overline{A}\overline{B}\overline{C} + \overline{A}B\overline{C} + AB\overline{C} + ABC \end{aligned}$$

# Truth table

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

## Lookup table implementation



## MUX example

$$\begin{aligned} F(A, B, C) &= \sum(0, 2, 6, 7) \\ &= \overline{A}\overline{B}\overline{C} + \overline{A}B\overline{C} + AB\overline{C} + ABC \end{aligned}$$

Therefore,

$$\overline{A}\overline{B} \rightarrow F = \overline{C}$$

$$\overline{A}B \rightarrow F = \overline{C}$$

$$A\overline{B} \rightarrow F = 0$$

$$AB \rightarrow F = 1$$

# Truth table

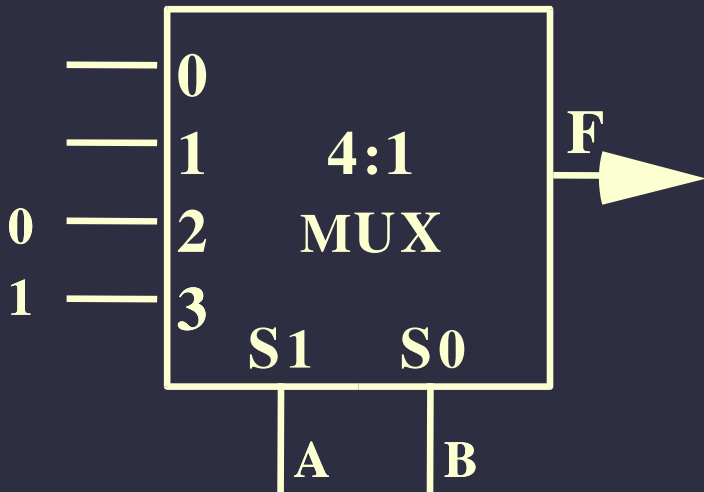
A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

# Truth table

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

$$F = \overline{C}$$

## Lookup table implementation



## Logic design summary

- Logic gate, transmission gate, and pass transistor design each have applications.
- MUX-based design provides a good starting point for transmission gate and pass transistor based design.

## Examples

Instead of flying through a bunch of slides, let's try examples.

- $f(a) = a$ .
- $f(a) = \bar{a}$
- $f(a, b) = a\bar{b}$
- $f(a, b) = ab$  (Check Figure 6-33 in J. Rabaey, A. Chandrakasan, and B. Nikolic. *Digital Integrated Circuits: A Design Perspective*. Prentice-Hall, second edition, 2003!)
- $f(a, b, c) = ab + \bar{b}c$  (try both ways).

Derive and explain.

## Upcoming topics

- Alternative logic design styles.
- Latches and flip-flops.
- Memories.

# Lecture plan

1. Interconnect: Rent's rule and coupling capacitance
2. Elmore delay modeling
3. Logic design
4. Homework

## Homework assignment

- 9 November, Tuesday: Read Section 6.3 in J. Rabaey, A. Chandrakasan, and B. Nikolic. *Digital Integrated Circuits: A Design Perspective*. Prentice-Hall, second edition, 2003.
- 11 November, Thursday: Homework 3.

# Special topic: Atomic layer deposition

Katherine Dropiewski, Matt Jansen, and Olga Rouditchenko