Pass-Transistor Logic and Dynamic Logic

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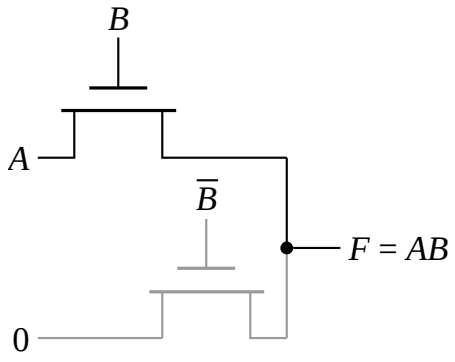
PTL AND Gate



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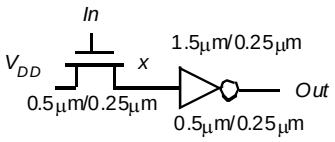
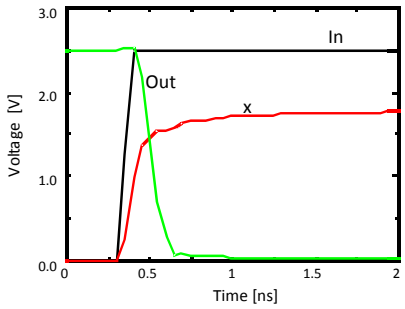
NMOS-Only Logic





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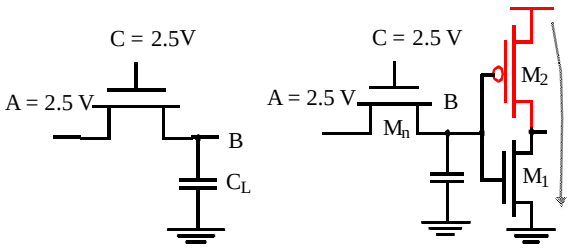
NMOS-only Switch



V_B does not pull up to 2.5V, but 2.5V - V_T

Threshold voltage loss causes static power consumption

NMOS has higher threshold than PMOS (body effect)

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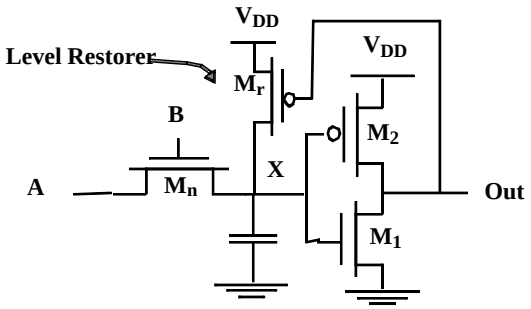
NMOS Only Logic: Level Restoring Transistor



- Advantage: Full Swing
- Restorer adds capacitance, takes away pull down current at X
- Ratio problem

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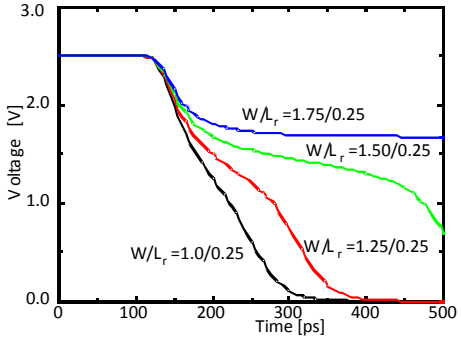
Restorer Sizing



- Upper limit on restorer size
- Pass-transistor pull-down can have several transistors in stack

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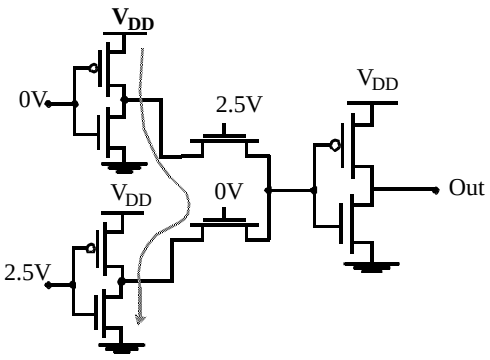
Solution 2: Single Transistor Pass Gate with V_T=0



WATCH OUT FOR LEAKAGE CURRENTS

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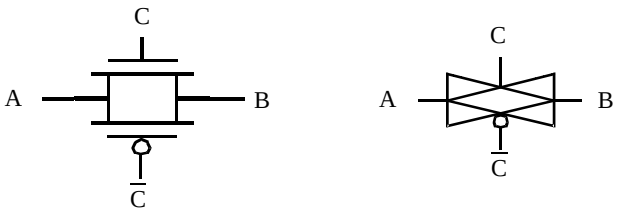
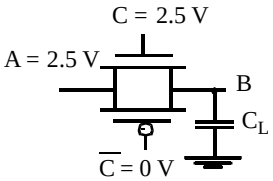
Solution 3: Transmission Gate





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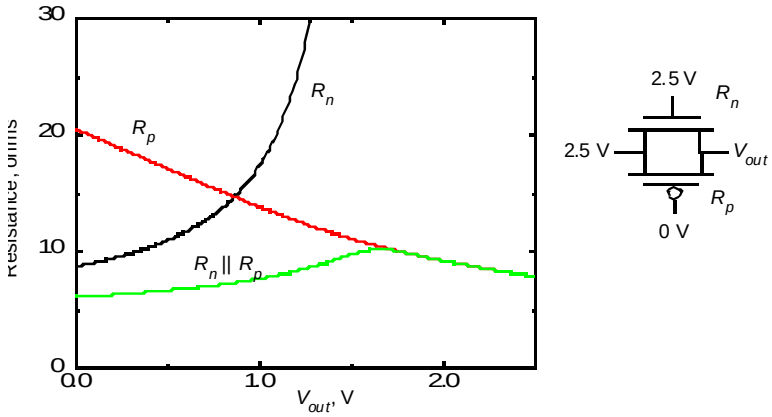
Resistance of Transmission Gate



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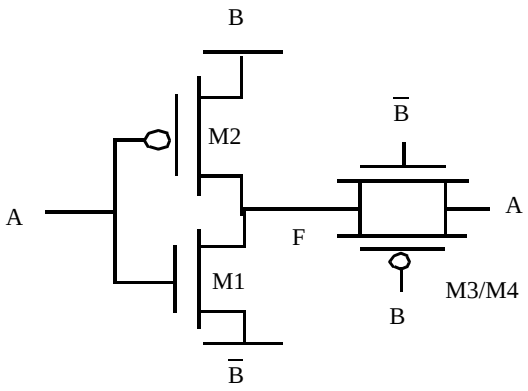
Transmission Gate XOR



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Dynamic CMOS

- In static circuits at every point in time (except when switching) the output is connected to either GND or V_{DD} via a low resistance path.
  - fan-in of *n* requires 2*n* (*n* N-type + *n* P-type) devices
- Dynamic circuits rely on the temporary storage of signal values on the capacitance of high impedance nodes.
  - requires on *n* + 2 (*n*+1 N-type + 1 P-type) transistors

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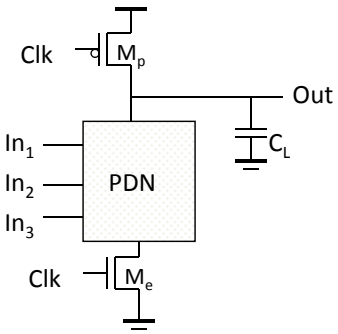
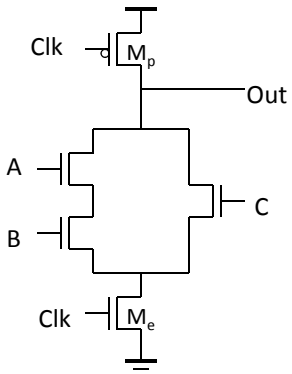
Dynamic Gate





Two phase operation
Precharge (CLK = 0)
Evaluate (CLK = 1)

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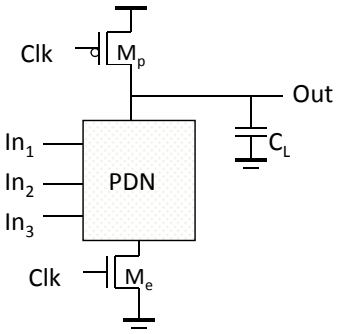
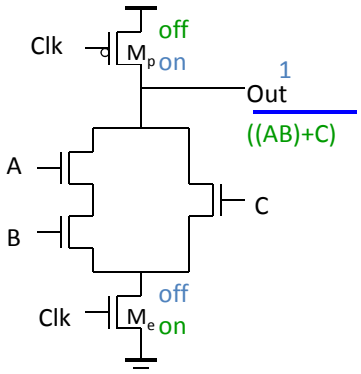
Dynamic Gate



Two phase operation

Precharge (Clk = 0)

Evaluate (Clk = 1)



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Conditions on Output

- Once the output of a dynamic gate is discharged, it cannot be charged again until the next precharge operation.
- Inputs to the gate can make at most one transition during evaluation.
- Output can be in the high impedance state during and after evaluation (PDN off), state is stored on C_L

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Properties of Dynamic Gates

- Logic function is implemented by the PDN only
  - number of transistors is N + 2 (versus 2N for static complementary CMOS)
- Full swing outputs (V_{OL} = GND and V_{OH} = V_{DD})
- Non-ratioed - sizing of the devices does not affect the logic levels
- Faster switching speeds
  - reduced load capacitance due to lower input capacitance (C_{in})
  - reduced load capacitance due to smaller output loading (Cout)
  - no I_{sc}, so all the current provided by PDN goes into discharging C_L

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Properties of Dynamic Gates

- Overall power dissipation usually higher than static CMOS
  - no static current path ever exists between V_{DD} and GND (including P_{sc})
  - no glitching
  - higher transition probabilities
  - extra load on Clk
- PDN starts to work as soon as the input signals exceed V_{Tn}, so V_M, V_{IH} and V_{IL} equal to V_{Tn}
  - low noise margin (NM_L)
- Needs a precharge/evaluate clock

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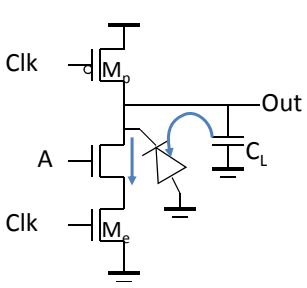
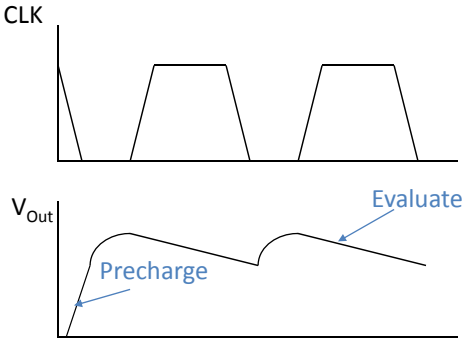
Issues in Dynamic Design 1: Charge Leakage



Leakage sources



Dominant component is subthreshold current

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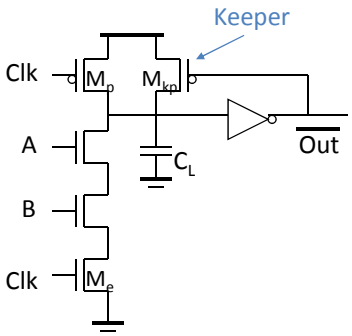
Solution to Charge Leakage



Same approach as level restorer for pass-transistor logic

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