Enabling Technology Development Through Modeling

Lei Jiang

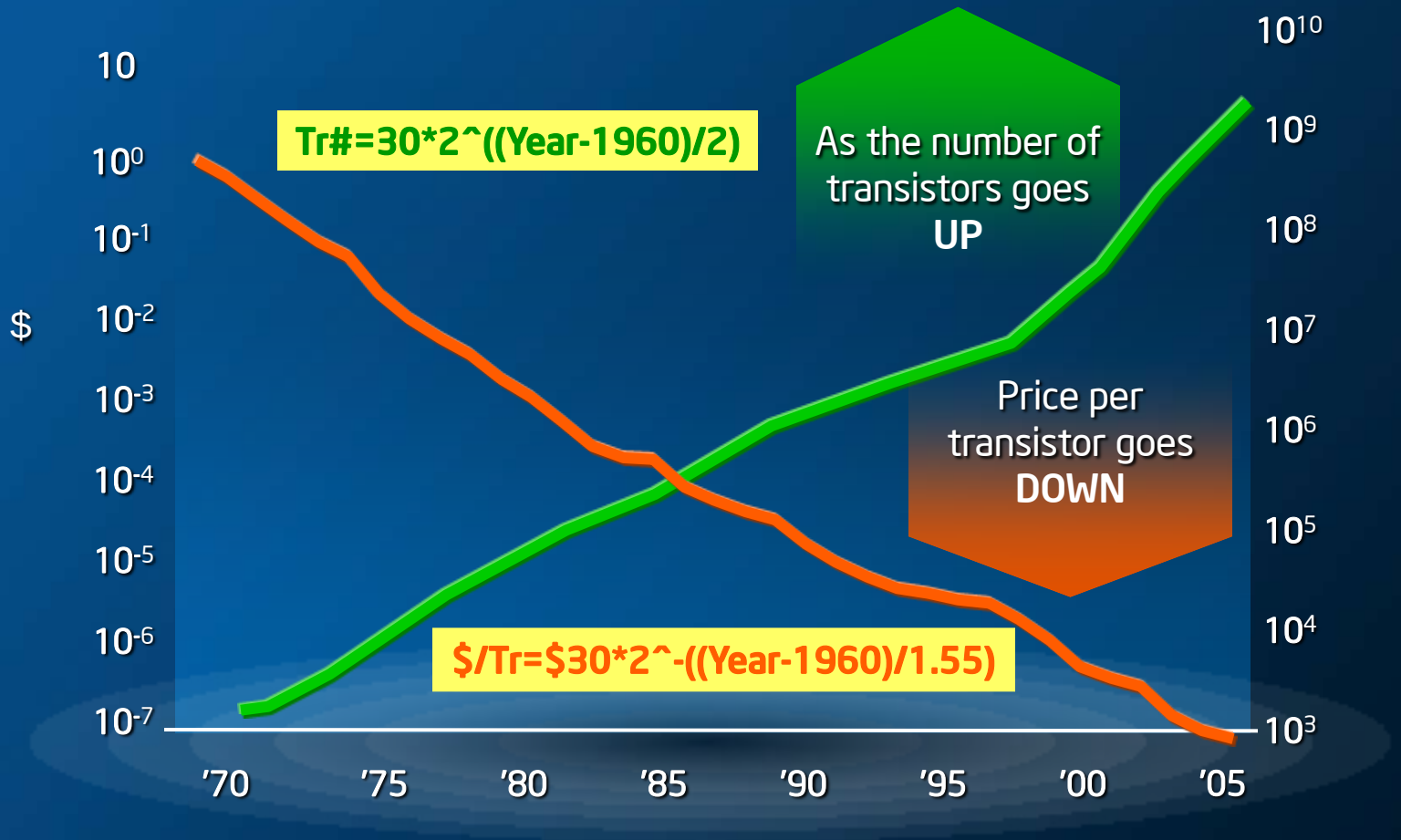
Sr. Staff Engineer

Thermo Mechanical Modeling Group
Technology Manufacturing Group
Intel Corporation

Outline

- Technology Scaling
  - Moore's law
  - Intel Process and Product
- Technology modeling
  - Material research
  - Lithography
  - Process Variation
  - Thermal, mechanical, reliability

The Cost Reduction Engine that Drives the Industry Growth

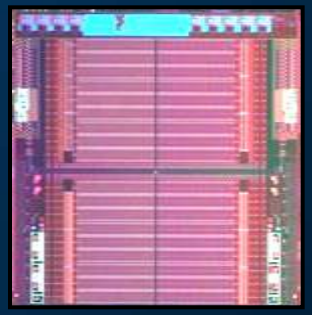


Source: WSTS/Dataquest/Intel

intel

Technology Scaling: 2 Year Cycles

90 nm	65 nm	45 nm	32 nm	22 nm
2003	2005	2007	2009	2011

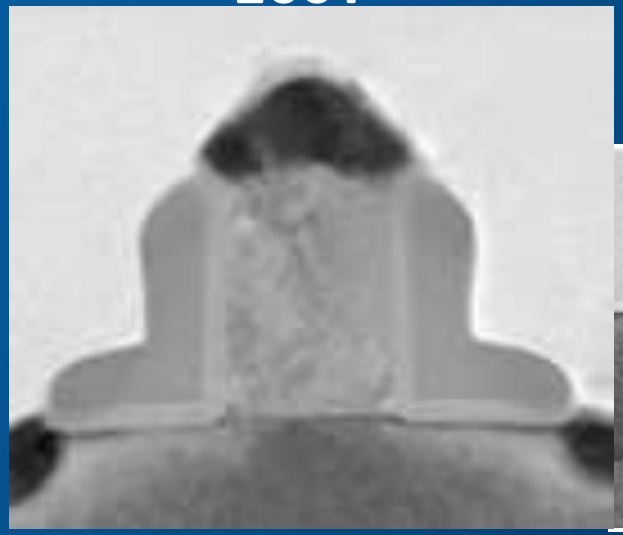


In development

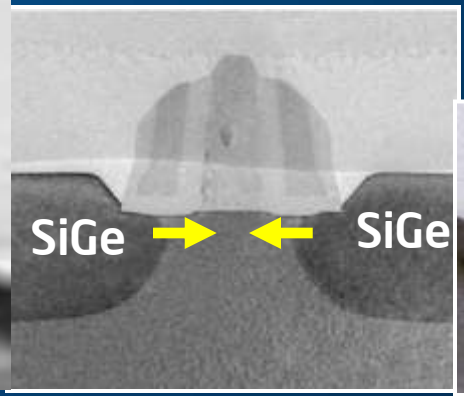
Source: V. Singh CSTIC 2010

The Ever-Shrinking Devices

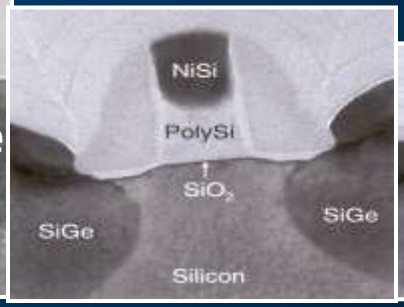
130nm
2001



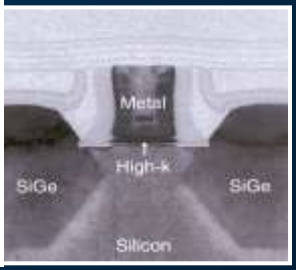
90nm
2003



65nm
2005



45nm
2007



32nm
2009

SiGe => Channel strain

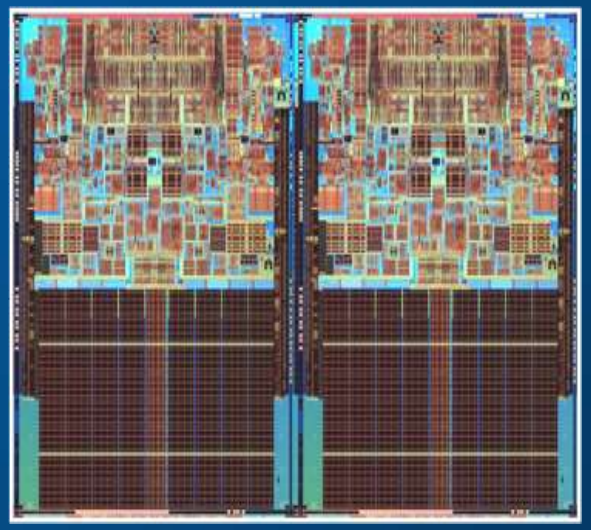
Hf-based dielectric
Metal gate electrode

With advances in materials and lithography, transistors continue to shrink in size

Ack: Rios April 2010

Moore's Law in Action

Intel® Xeon® 5300 Processor
(Clovertown)
65 nm

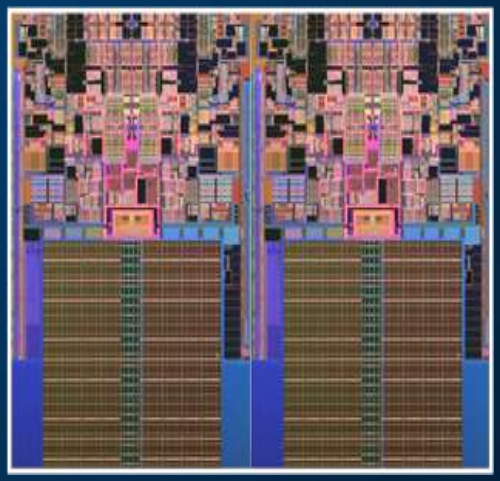


143 mm^2

582M Transistors
8 MB Cache

1.9x
transistors/mm^2

Intel® Xeon® 5400 Processor
(Harpertown)
45 nm Hi-k



107 mm^2

820M Transistors
12 MB Cache

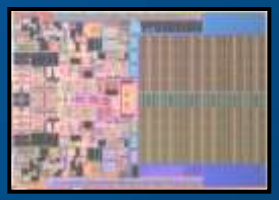
Ack: Rios April 2010

Source: Intel

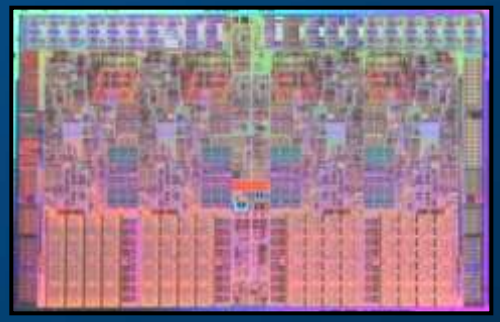
A Family of 45nm Microprocessor Products

Atom

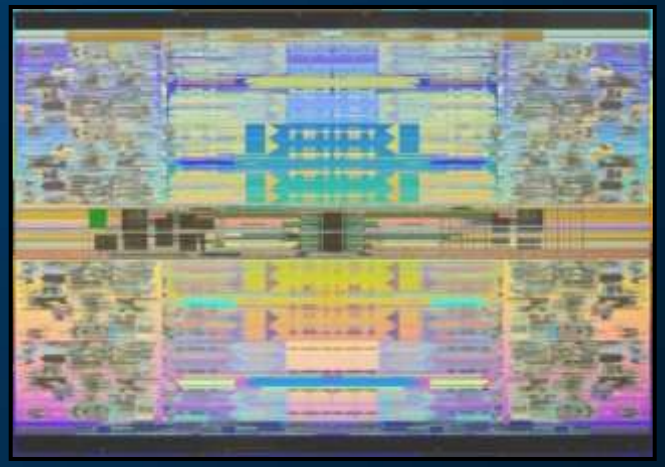
Core 2 Duo



Core i7



Xeron server

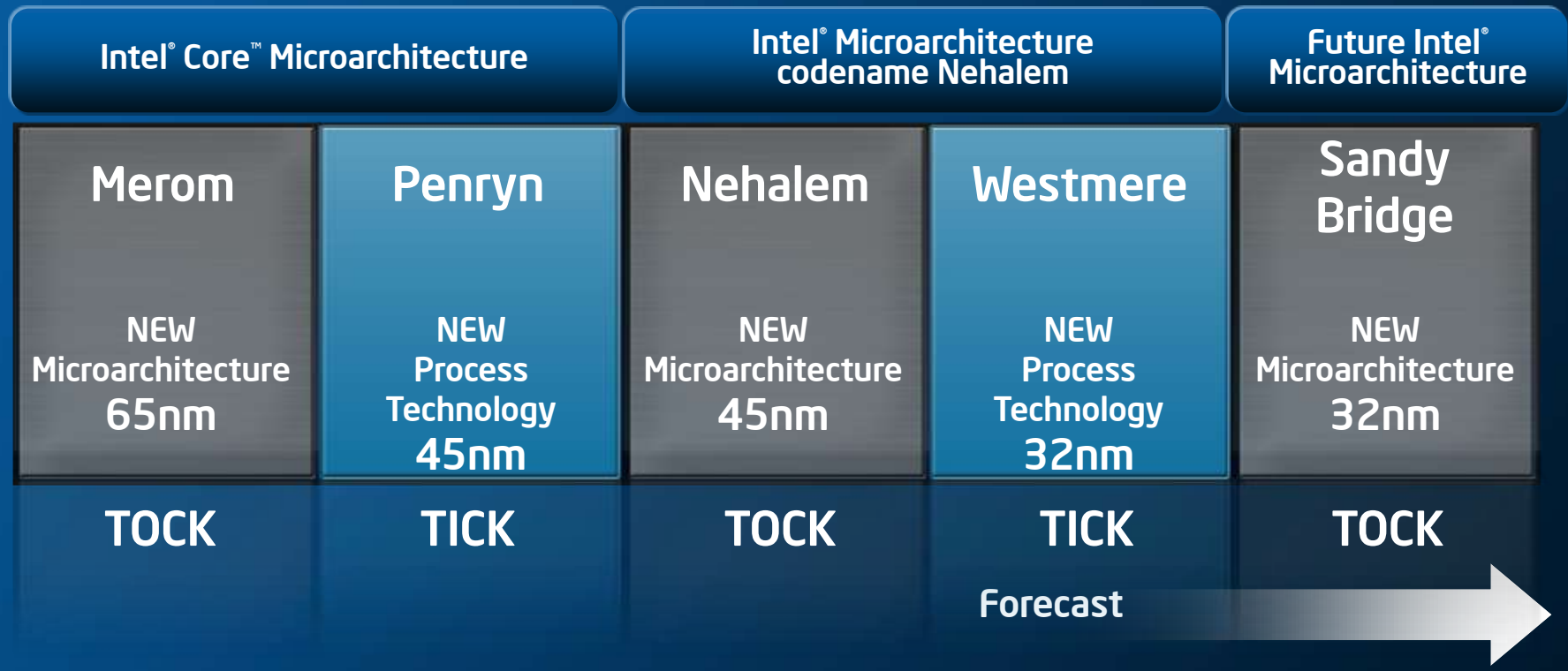


One technology, different market and design complexity

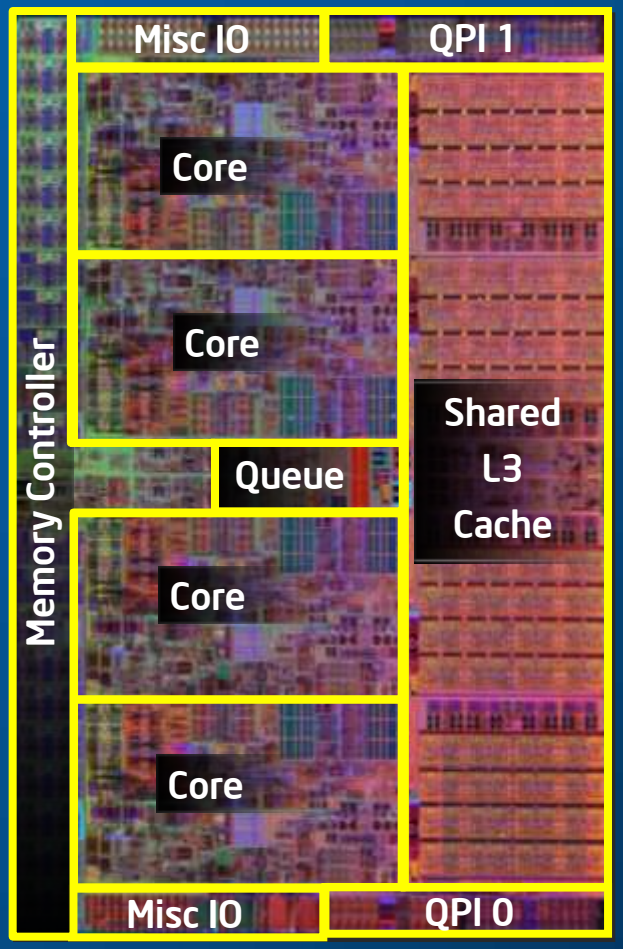
Ack: Rios April 2010

Microprocessor Development

Tick-Tock Development Model:
Sustained Microprocessor Leadership



Intel® Core™ i7 Microarchitecture

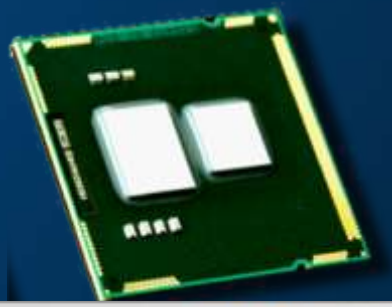


QPI: Intel® QuickPath Interconnect (Intel® QPI)

- **Core microarchitecture (Nehalem)**
  - Increased parallelism
    - e.g. 33% larger out of order window, handle more cache misses simultaneously
  - Enhanced algorithms
    - e.g. faster "unaligned" cache accesses, faster sync primitives, loop streaming detector, macro-fusion
  - Better branch prediction
    - e.g. 2nd level branch predictor, renamed RSB
  - New Instructions (SSE4)
  - Intel® Hyper-Threading Technology
- **Uncore microarchitecture and connectivity**
  - Scalable multi-core fabric
  - Shared last level Cache
  - Integrated memory controller
  - Intel® QuickPath Interconnect
- **Power management technologies**
  - PCU Microcontroller
  - Intel® Turbo Boost Technology
  - Integrated power gates

Ack: Stephan Jourdan, Intel Developer Forum 2009

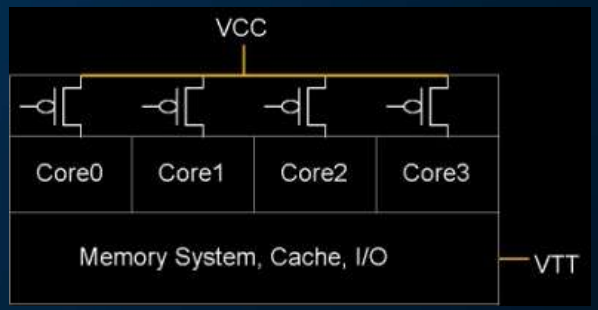
Clarkdale / Arrandale (Core i3/i5/i7)



- 32nm 2nd generation High-K metal gate processor
- 45nm process High-K metal gate integrated graphics

Key Features:

- 32nm Intel Microarchitecture codenamed 'Westmere'
- Intel® Hyper-Threading technology for 4 threads delivers a great multi-media experience
- Intel® Turbo Boost Technology for dynamic frequency scaling
- Up to 4MB of Intel® Smart Cache
- Integrated graphics or discrete/switchable graphics
- Advanced Encryption Standard (AES) acceleration



Dynamically Scaled Performance Boost

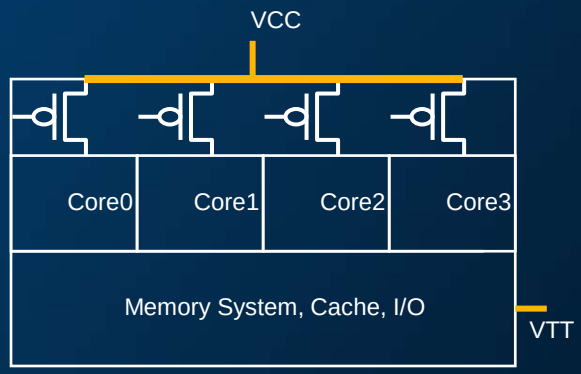
Major Innovations in Energy Efficiency

World First 32nm Based Processor

Ack: Stephan Jourdan, Intel Developer Forum 2009

Integrated Power Gates

- Integrated Power Gates (switches) are critical for integration, turning individual component blocks on/off
  - Zero leakage power, low latency to wake block
  - Key benefits in both idle and active power
- Nehalem turns individual cores on/off
  - Transparent to OS
  - Reduces latency to wake a core
  - Modular/Scalable Clocking
    - Cores, Memory System, I/O can run at independent voltage/frequency



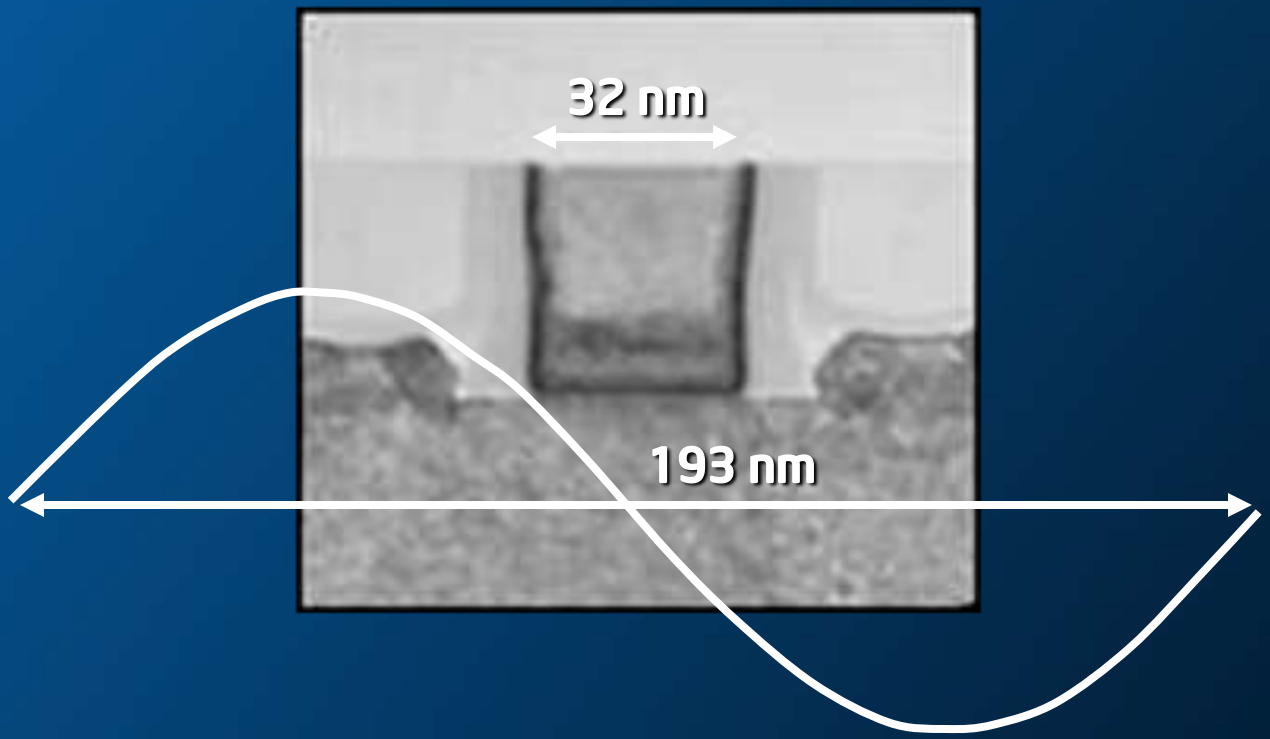
- Extended in 2009 platforms as Integrated Power Gates: in shared cache and I/O logic to dynamically power down when inactive

Integrated Power Gates enable Energy Efficient Integration

Ack: Stephan Jourdan, Intel Developer Forum 2009

Lithography: Driver to Enable Scaling

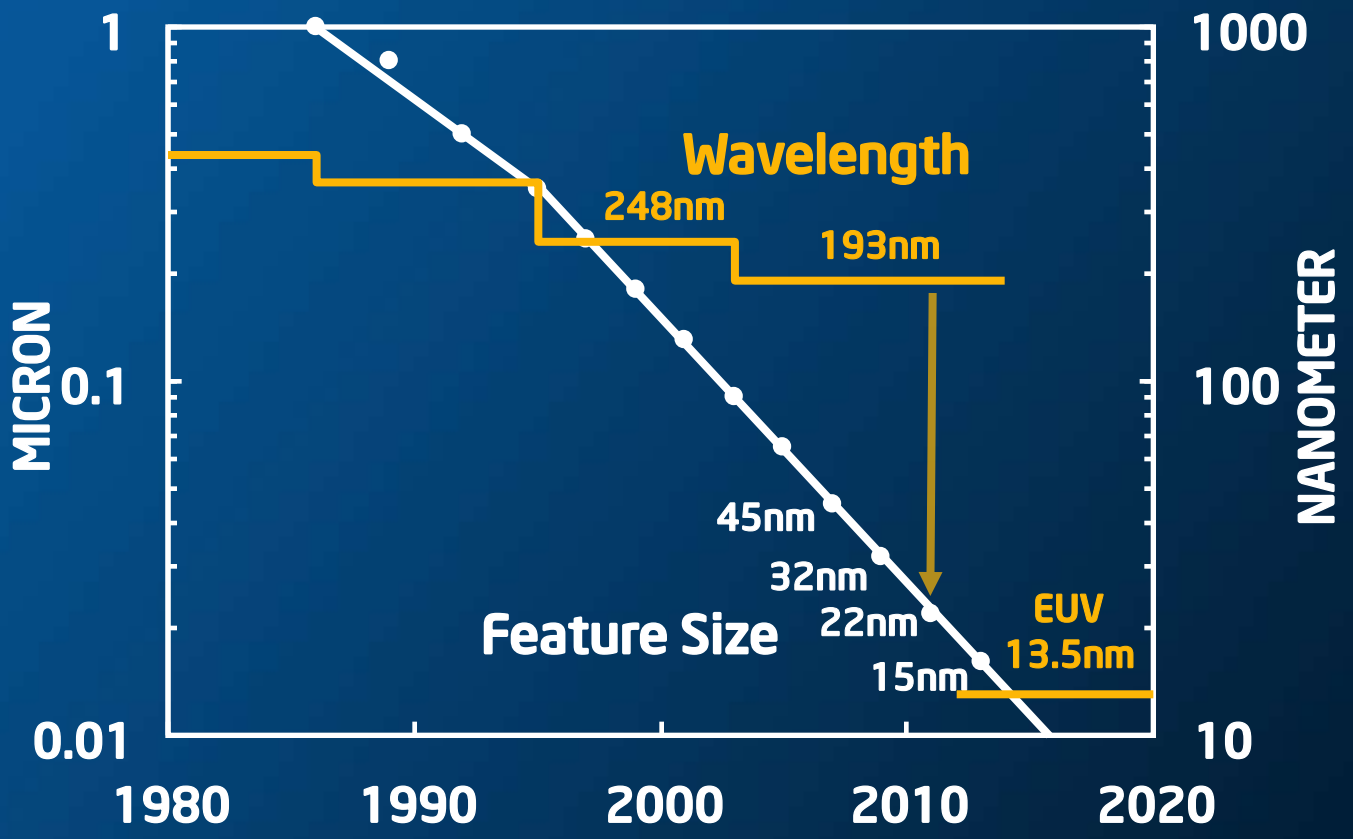
The Lithography Challenge



Litho continues to use 193nm wavelengths to define features many times smaller

Source: Rios April 2010

Lithography Pipeline



Extend 193nm Optical Lithography as far as possible
Deploy EUV Lithography when available/affordable

Source: Singh, CSTIC, 2010

Multiple Lithography Innovations

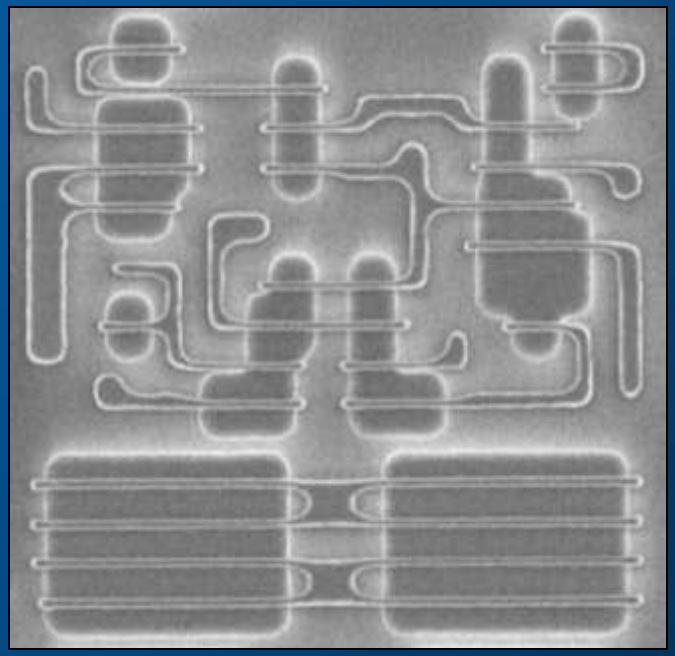
- Optical proximity correction
  - Phase shift masks
  - Double patterning
  - Immersion optics
  - Pixelated masks
- Computational lithography

Enhancements have extended 193nm lithography to the 22nm generation

Source: Singh, CSTIC, 2010

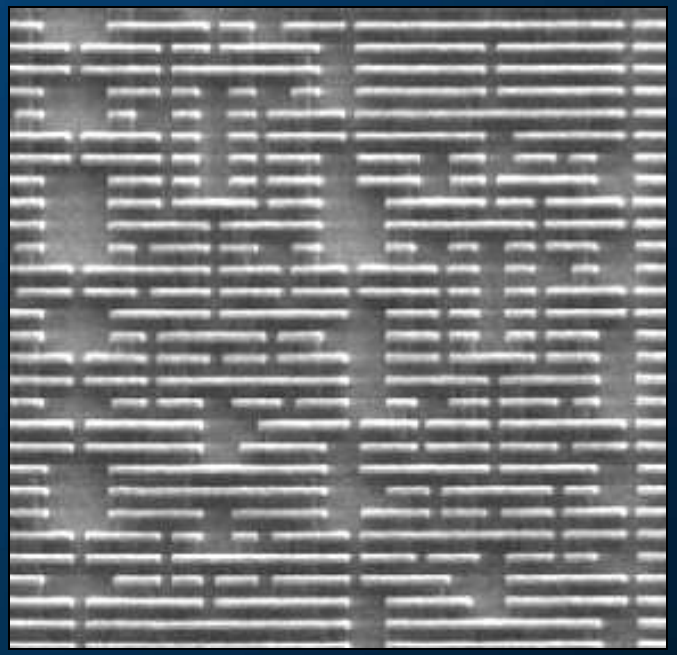
Layout adapted to litho constraints

65 nm Layout Style



- Bi-directional features
- Varied gate dimensions
- Varied pitches

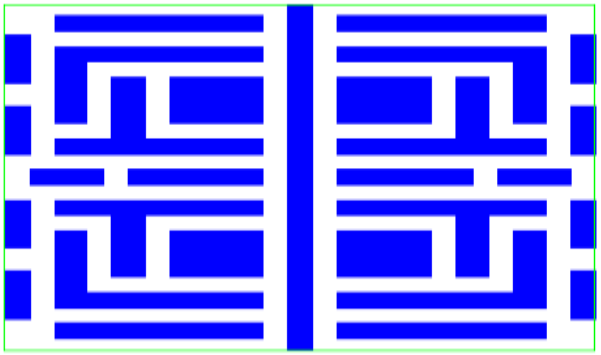
32 nm Layout Style



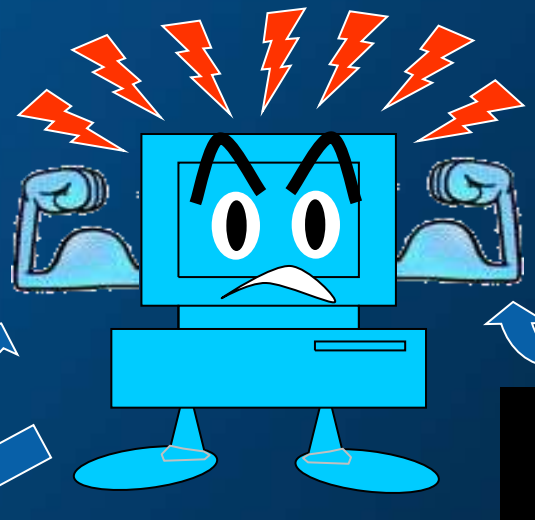
- Uni-directional features
- Uniform gate dimension
- Gridded layout

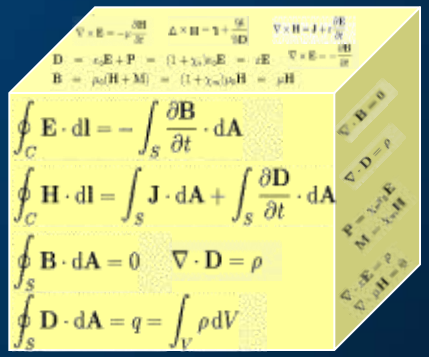
Source: M. Bohr, ISCC, 2009

Computational Lithography and Pixelated Masks

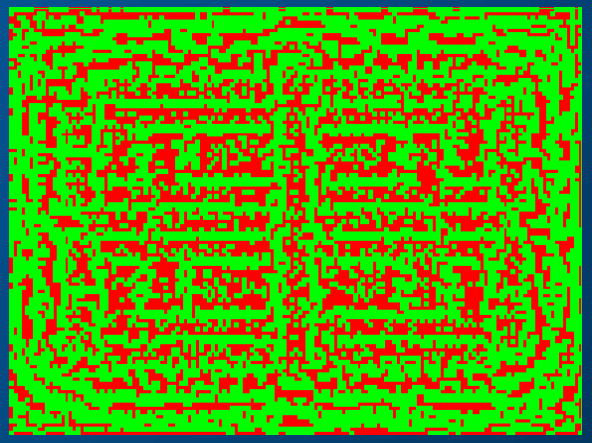


Design Pattern

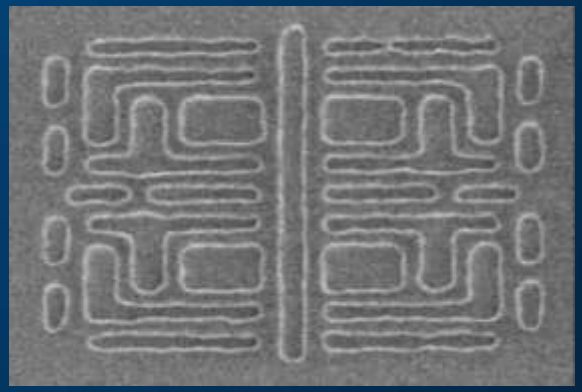




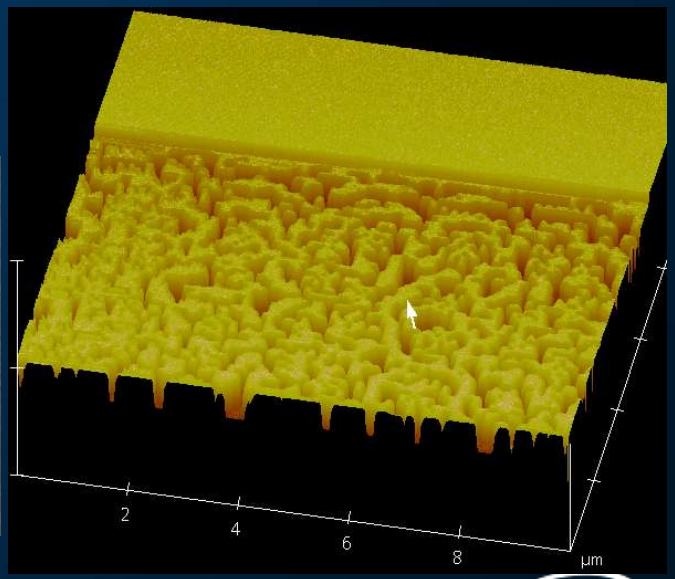
Model black-box



Pixelated mask



SEM image of wafer

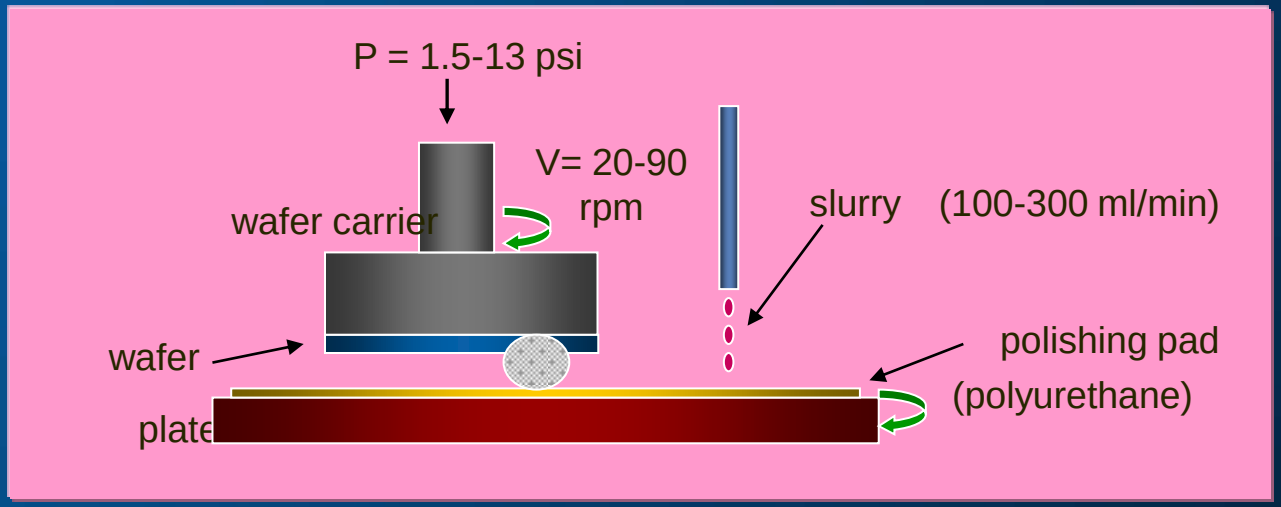


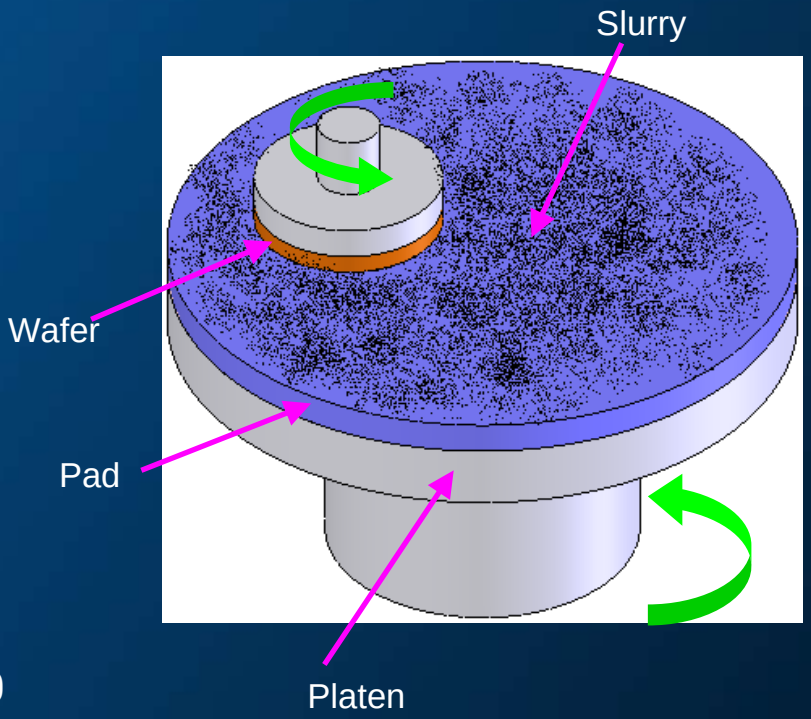
Atomic Force Microscope
Picture of mask

Source: Singh, CSTIC, 2010

Process Modeling: Integrating material science, chemistry, mechanics …

Typical CMP Platform





Ack. M. Buehler, 2010

Intel CMP Technologies

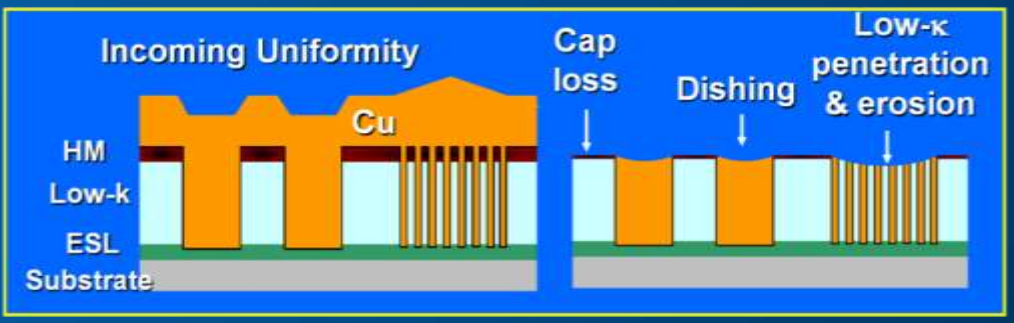
Node	Year	Module	Goals
0.8um	1990	ILD	Multi-level metallization
0.35um	1995	STI PSP W	Compact isolation Poly Si patterning Yield/defect red.
0.18um	1999	SiOF ILD	RC scaling
0.13um	2001	Cu	RC scaling
90nm	2003	SiOC ILD	RC scaling Cost Reduction
65nm	2005	--	Cost Reduction
45nm	2007	Poly Opening Metal Gate	High-k Transistor Cost Reduction
32nm	2009	Poly Opening Metal Gate Trench Contact	High-k Transistor Cost Reduction

- Many new CMP processes were introduced during the 1990s
- Cost reduction was a focus for most of the 2000s
- Recently, we introduced new CMP modules for the high-k transistor

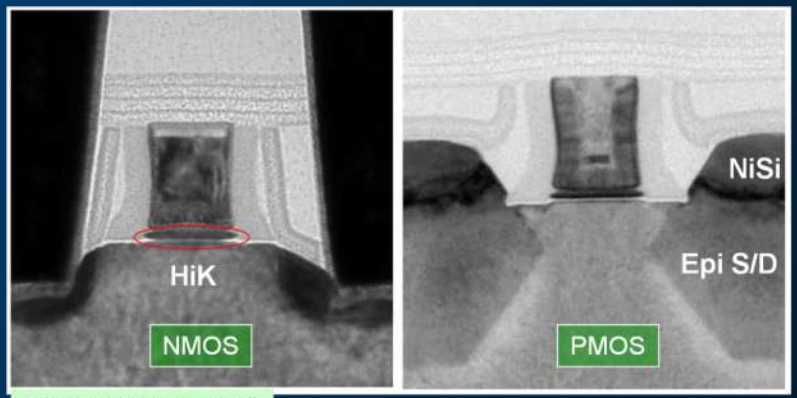
Ack. M. Buehler, 2010

Chemical Mechanical Planarization

• Interconnect



• Device



C.Auth et al. VLSI Symp. (2008)

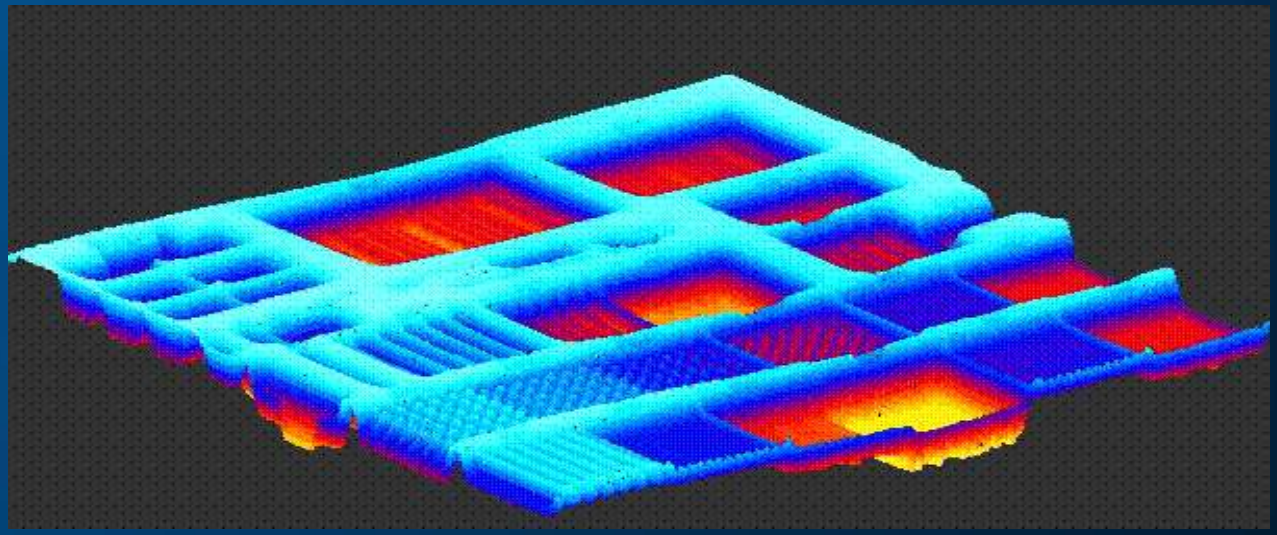
- ❑ Challenges
  - ➢ Mechanical Integrity Issues
  - ➢ Corrosion & Defectivity Concerns
  - ➢ Topography control

- Gate height control critical to proper transistor function
- Dimensions on 10nm scale; tolerance (1 nm)
- PMOS/NMOS differences complicate CMP

Ack. M. Buehler, 2010

Nanomechanics – Modeling Solutions

- Flow dynamics on nanometer scales
- Dynamic particle contact and fracture actions
  - Contact mechanics (nm – mm) – pad with asperity layer: deformation is function of topography
- Integrate stress with kinetics, flow and particle dynamics
- More advantageous than empirical modeling



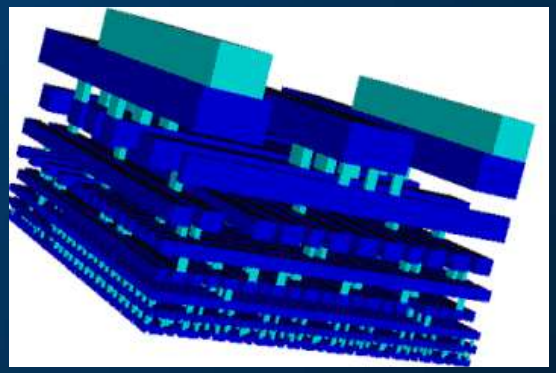
L Jiang et al. CMP-MIP 2004

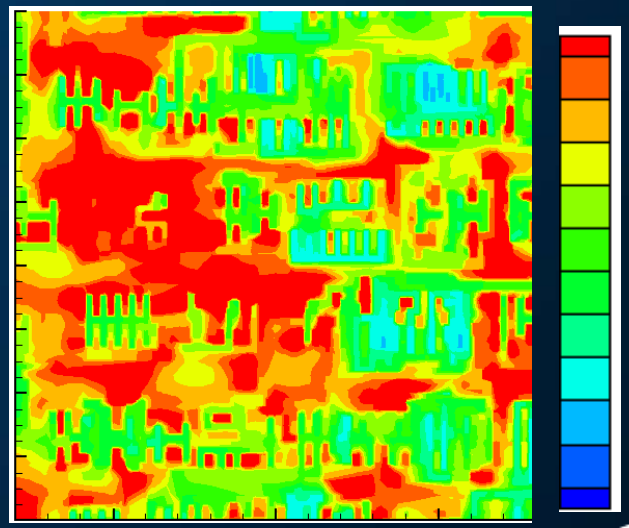
Reliability: Thermal Phenomena

Nano-micro scale: self-heating

Device and interconnect self heat becomes more critical

- More restrictive with scaling
- Impact reliability (e.g. electromigration)
- Circuit performance

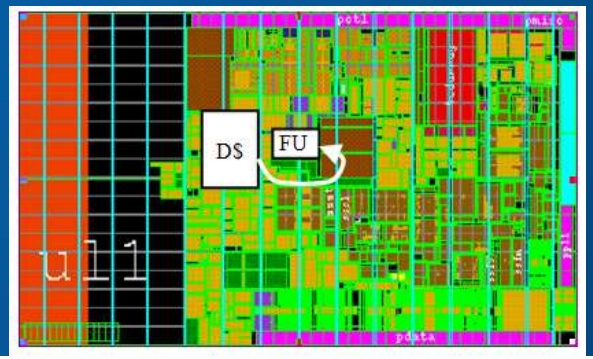


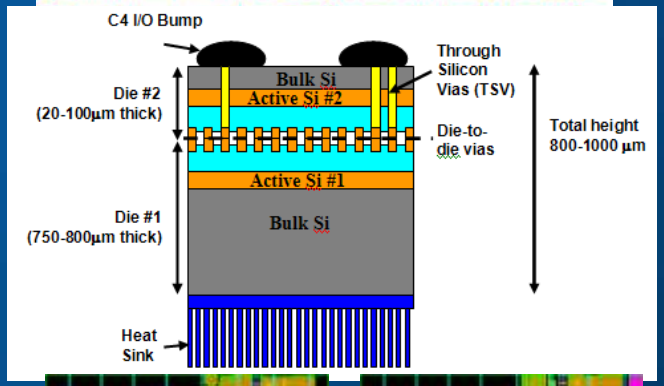


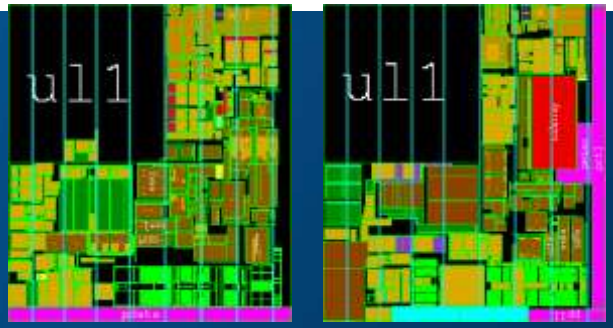
Source: Oregonian 2008

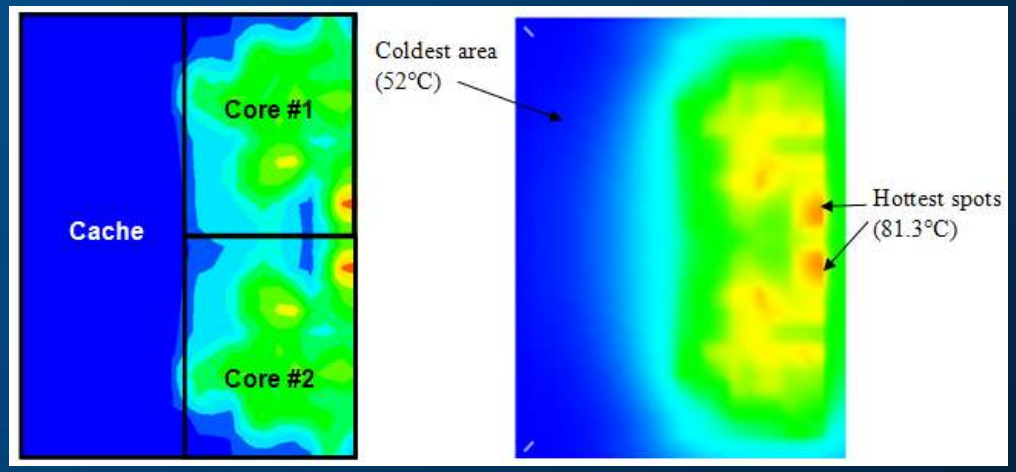
L. Jiang et al. IEEE IRPS 2009

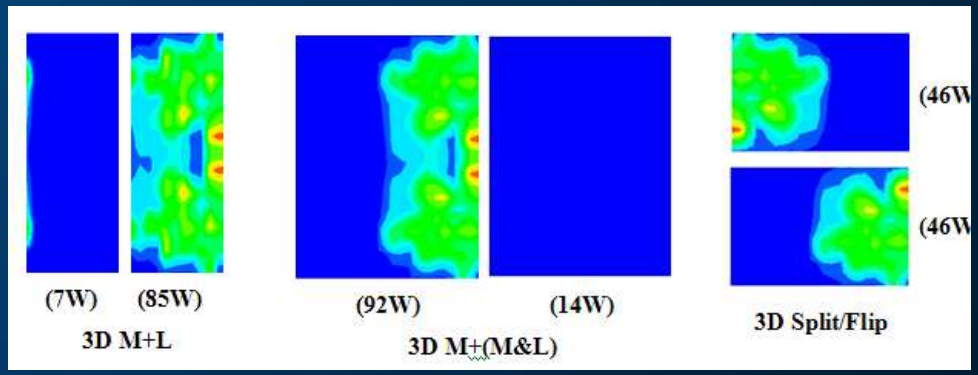
Three-Dimensional Die Stacking











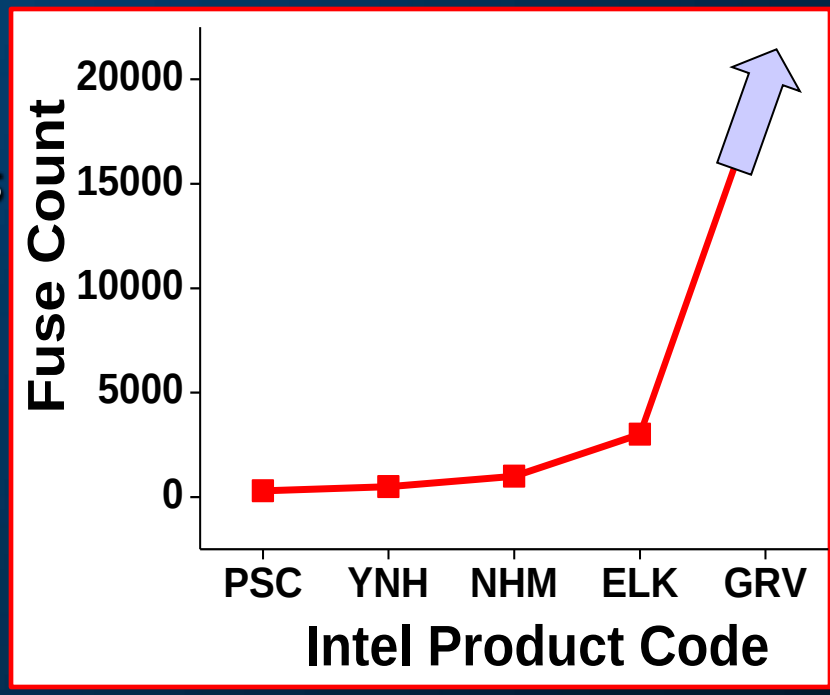
Double transistor density; impact power/latency

Heterogeneous technologies and system integration

B. Black et al. MICRO 2006

Fuse Design: Background

- On-chip Fuse critical functionalities
- Novel product features = rapid increase in on-chip fuse content
  - Security applications, e.g. HDCP keys
  - Microcode storage

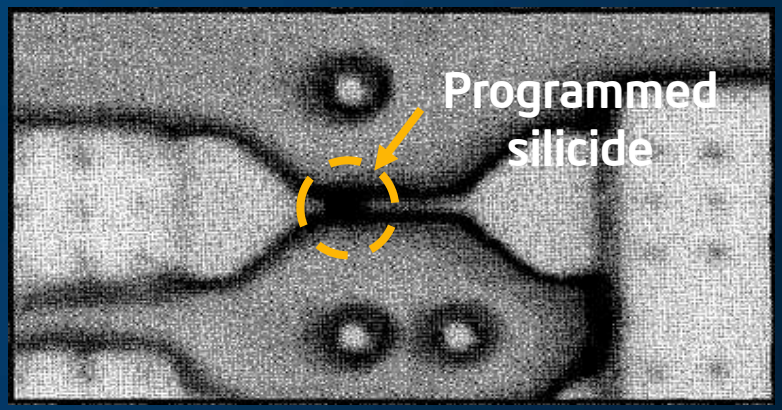


- Challenges
  - Small bitcell footprint
  - High-density array design
  - Reliable high-voltage programming
  - Low program pulse duration

Kulkarni et al. VLSI 2009, JOURNAL OF SOLID-STATE CIRCUITS, 2010

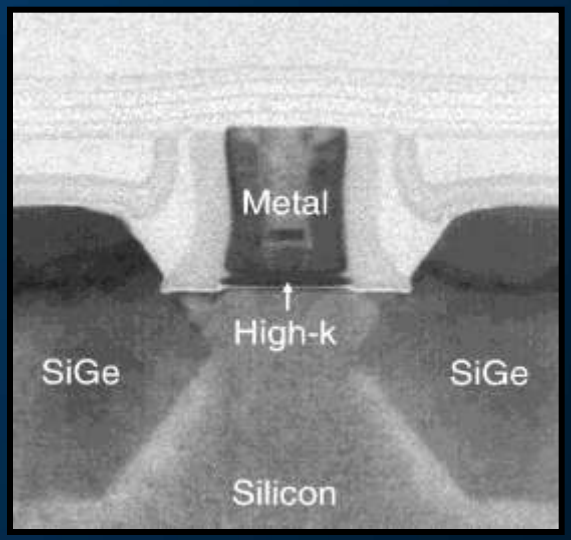
New Design: Using Thermal Physics

- Silicided polysilicon has traditionally served as the fuse element
  - Alavi, IEDM 1997
  - Chung, VLSI 2007
  - Uhlmann, ISSCC 2008



Source: M Alavi, IEDM 1997

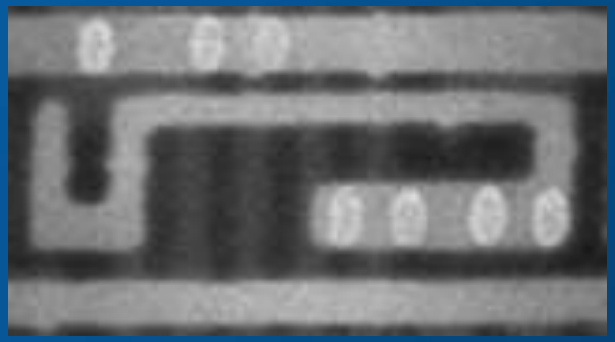
- Modern Metal-Gate technology integration necessitates a significant shift in fuse design
  - Intel 45nm: Mistry, IEDM 2007
  - Intel 32nm: Natarajan, IEDM 2008



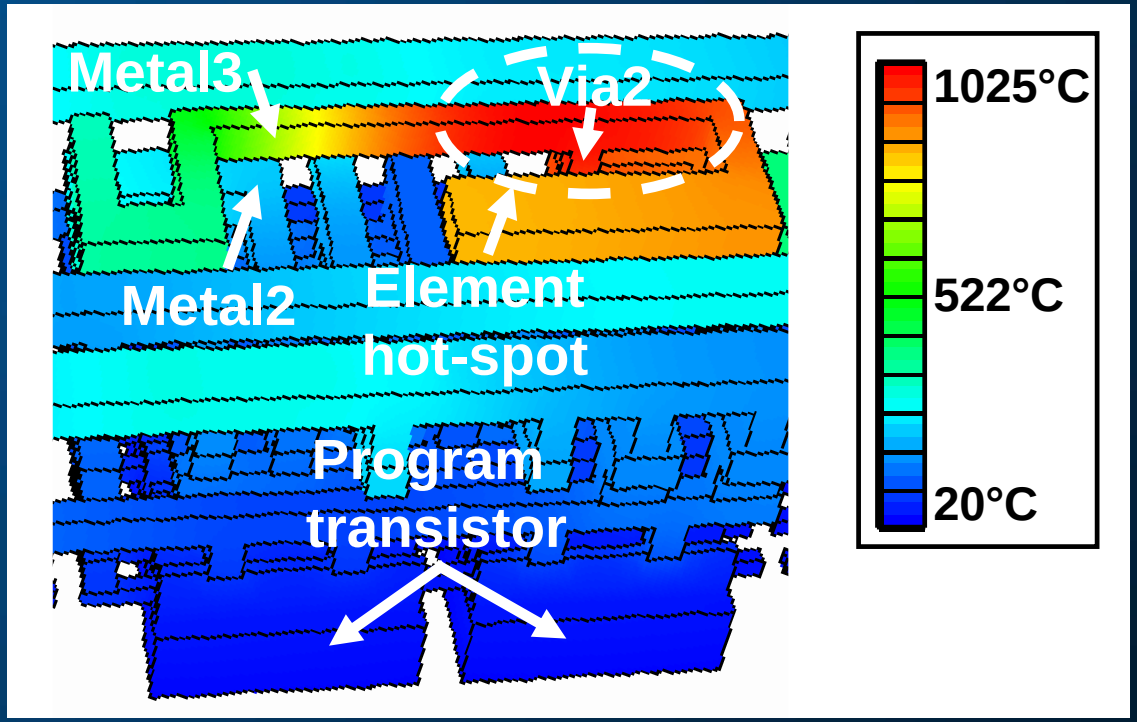
Source: K Mistry, IEDM 2007

Kulkarni et al. VLSI 2009, JOURNAL OF SOLID-STATE CIRCUITS, 2010

Electrothermal Analysis of Programming



1.37μm² SEM



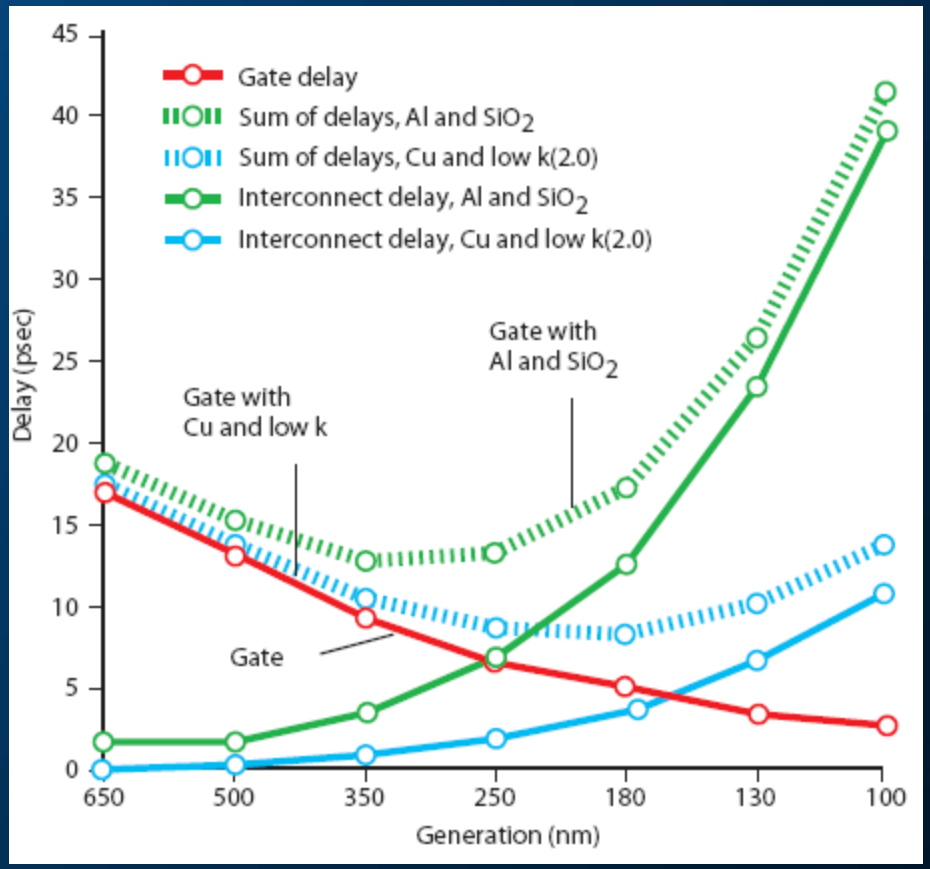
- Programming is based on metal electromigration
  - Momentary high current injection generates hot-spot
  - Void formation at via enables product security applications
- Localized peak temperature meets all reliability requirements

Kulkarni et al. VLSI 2009, JOURNAL OF SOLID-STATE CIRCUITS, 2010

Interconnect Reliability: Drivers for Thermo-Mechanical failures

Interconnect Performance Trends – Need for low-k dielectrics

- Beyond 100 nm node keeping ILD k < 2.0 is required to maintain delay within acceptable limits

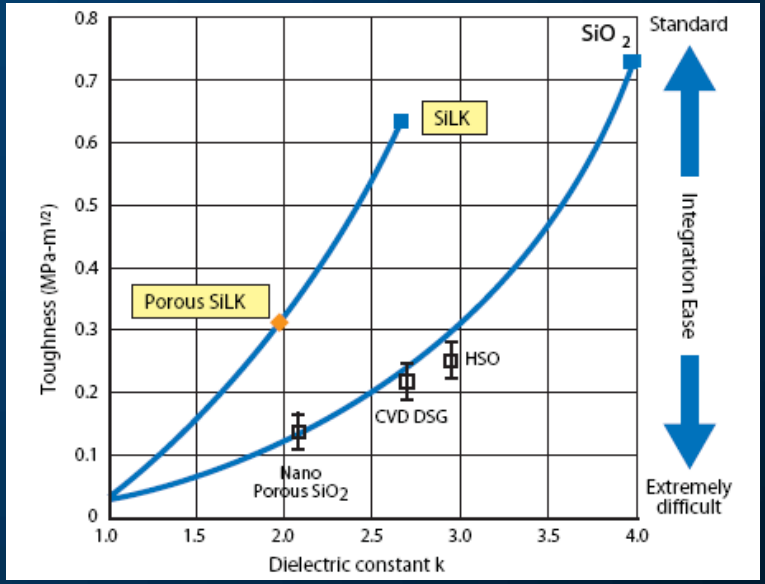


Ack: Pantuso, Purdue, July 2009

Thermo-Mechanical Reliability Concerns

- Lower-k materials are mechanically weaker
- Thermo-mechanical reliability is a concern
  - Two main sources of stresses in Si interconnect thin films
    1. Temperature variations due to wafer processing
    2. Die/package interactions due to the difference in coefficient of thermal expansion between the Si and package material

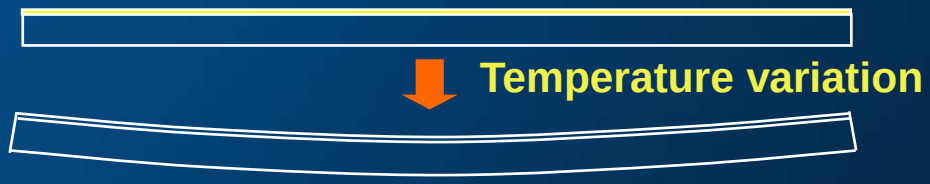
Ref: B. Chandran, et.al – Future Fab International – 17 (2004)



Ack: Pantuso, Purdue, July 2009

Interconnect Thin film stress

- Two main sources of stress in Si interconnect thin films
  - Temperature variations due to wafer processing
    - Leading mainly to large in-plane stresses in the film causing delamination or cohesive cracks in ILD, metal voiding



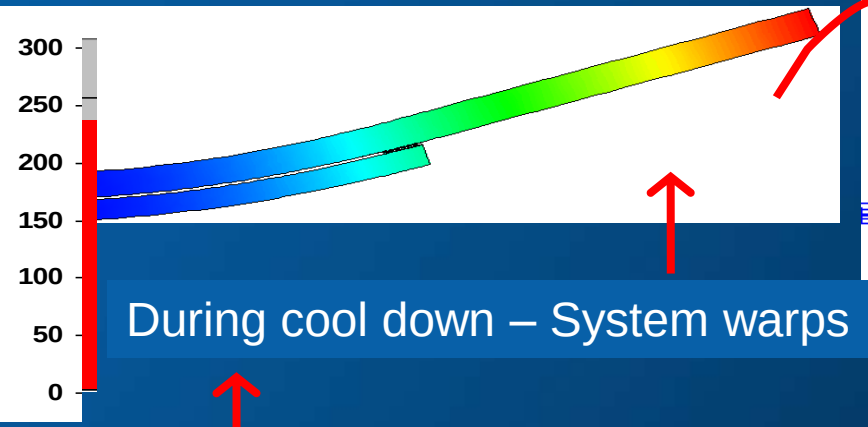
Thin film
0.1 - 10 um thick

Silicon substrate
0.7 mm thick – 300 mm diameter

  - Die/package interactions due to the difference in coefficient of thermal expansion between the Si and package material
    - Si CTE ~ 2.3 x10-6, Package CTE = 16.0 x10-6
    - Leading mainly to large out-plane stresses in film; causing cohesize cracking, delaminations, large stress at the solder joint (EM issues)

Ack: Pantuso, Purdue, July 2009

Mechanics of stress transfer to the Si due to die/package interaction

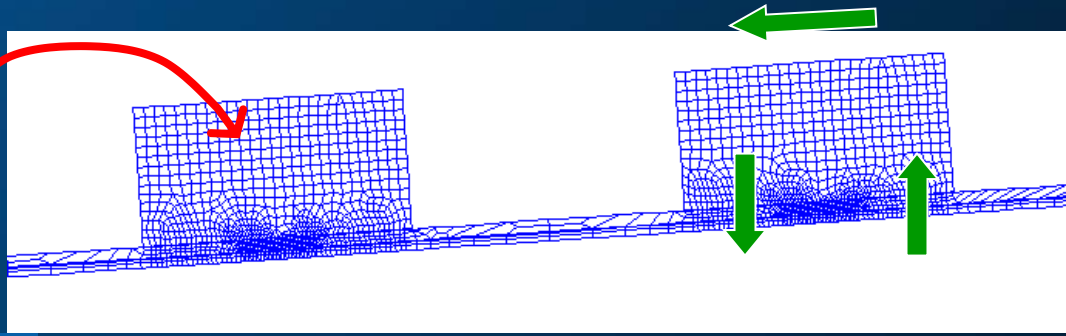


During cool down – System warps

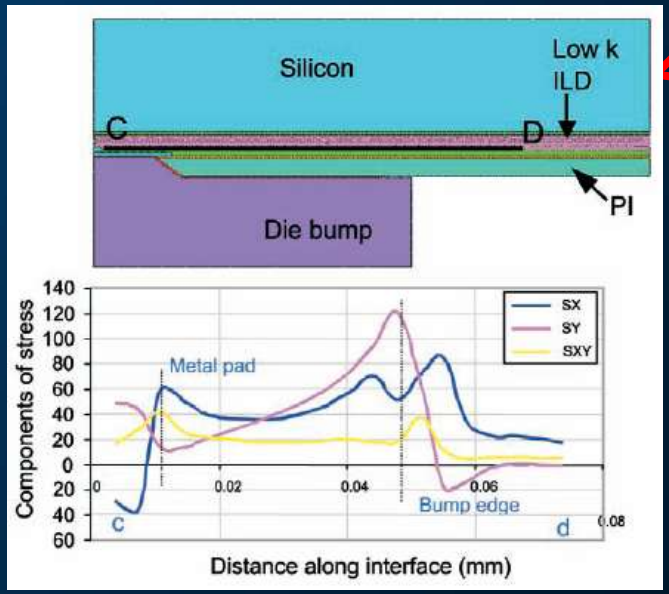
Package substrate is attached to Si

Process Temperature

Bump/solder shear/rotation results in tensile stress on the bump side closer to the die edge



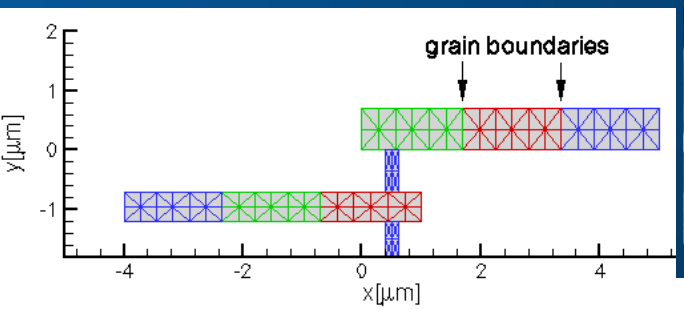
Die/package warpage results in Cu bump shear and rotation → Mechanism for stress transfer to the Si die

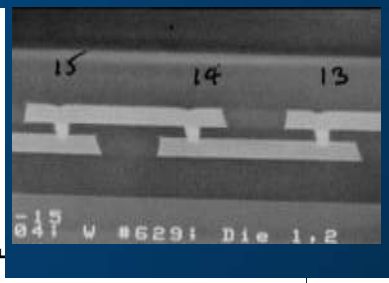


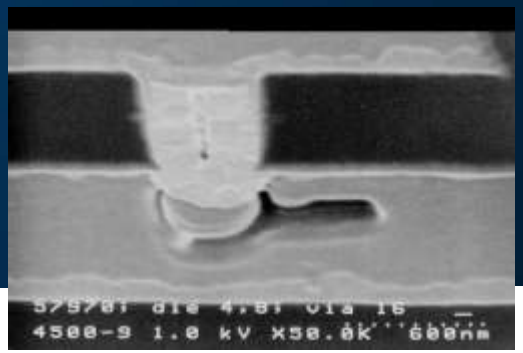
Ack: Pantuso, Purdue, July 2009

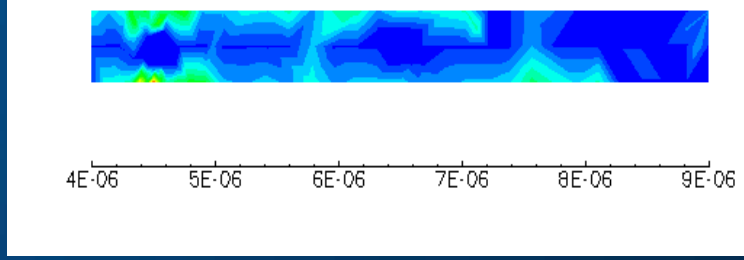
Interconnect stress voiding

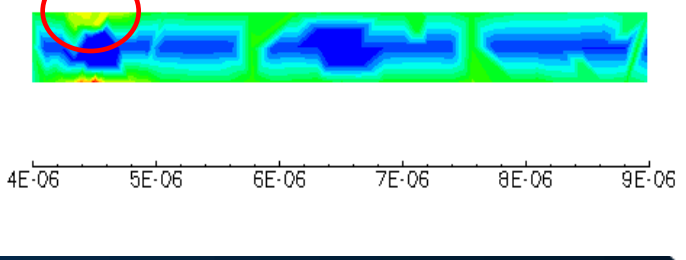
- Void growth by vacancy diffusion along preferential paths such as grain boundaries and interfaces
  - When the vacancy concentration due to plastic deformation is larger than the equilibrium concentration near the free surface of the void → vacancies moves towards the surface

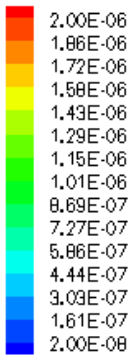












Ref: Cuitiño et.al. MRS 2003

Ack: Pantuso, Purdue, July 2009

Summary

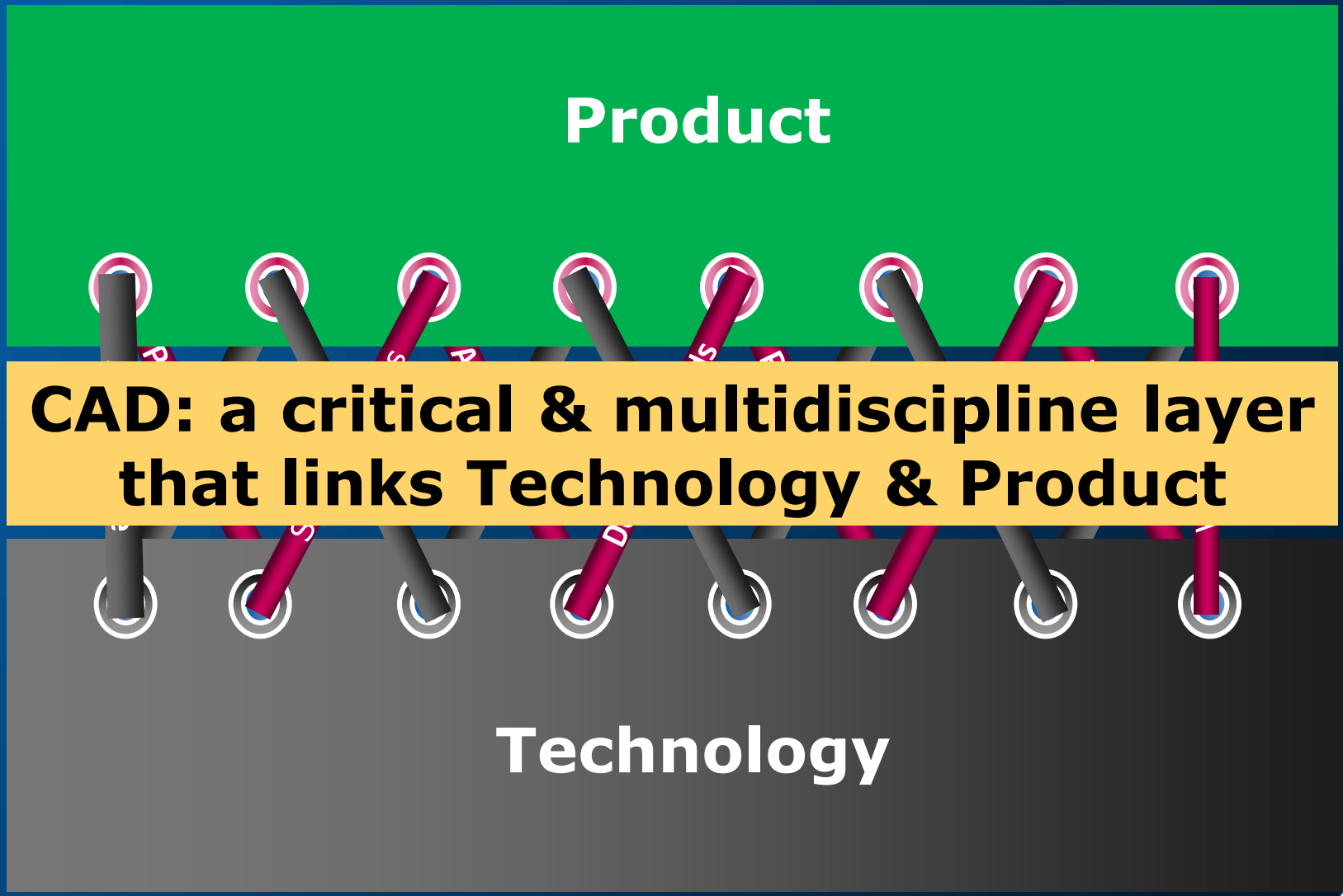
- Intel continues relentless pursuit of scaling
- CAD continutes to be play key role to lithography, device, and process integration
- Reliability and variation simply become more challenging at leading edge technology
  - Modeling helps set direction for disruptive technology and design of new circuit

Source: Garcia July 2010

Technology Leadership Through Close Multi-group Collaboration

Source: Shankar, Tech. Lec. Series, 2007

CAD Bridges Technology & Product



Source: Dai, 2009

Design & Technology Solutions

Validation, power, & design efficiency	Deliver process leadership to Design	Maximize test & debug efficiency

Integrate design & validation across boundaries

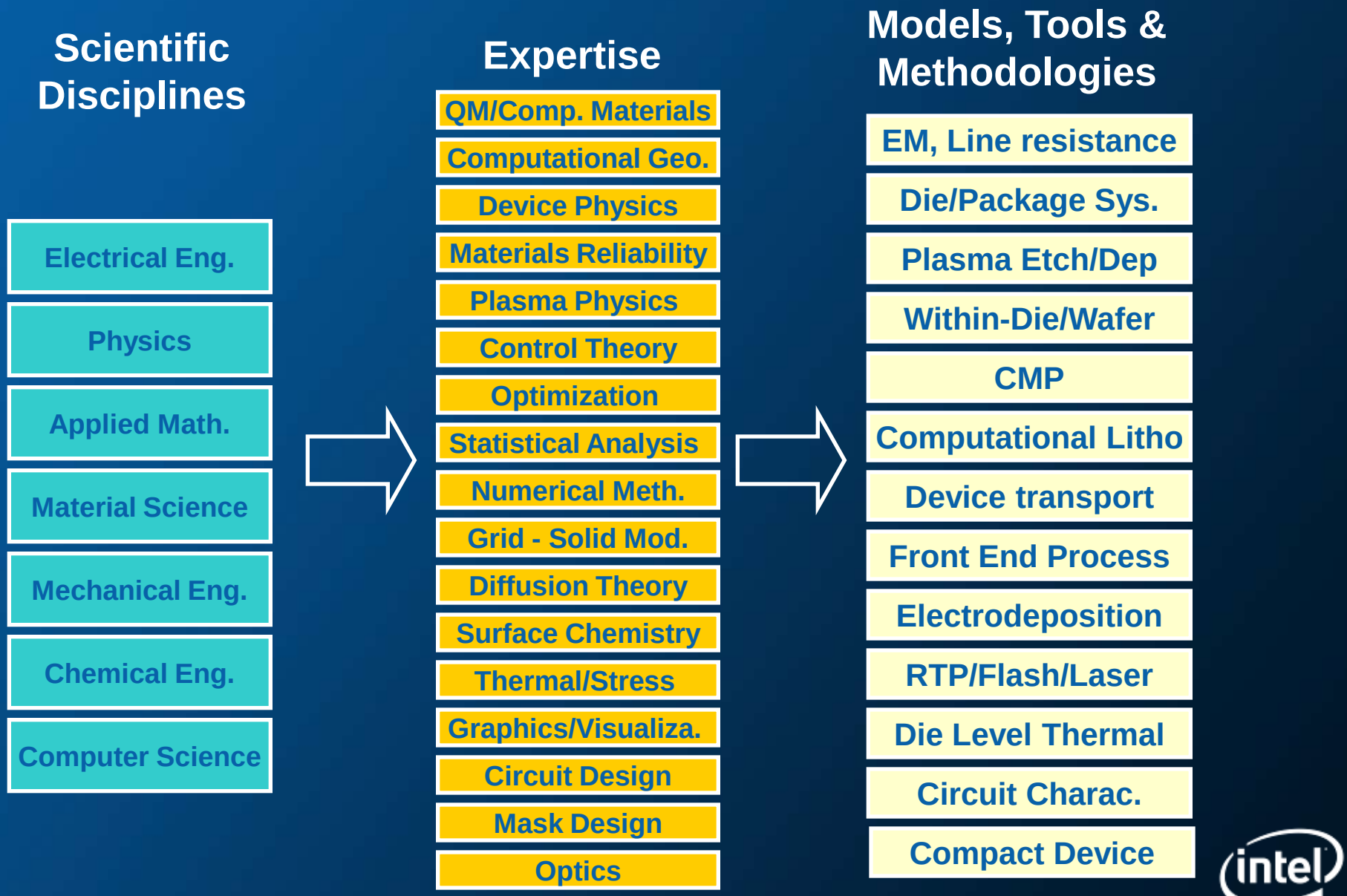
Enable modular design

Solutions for developing leading process technology

Address the entire platform

Source: Dai, 2009

Process and Technology Modeling : Core Expertises



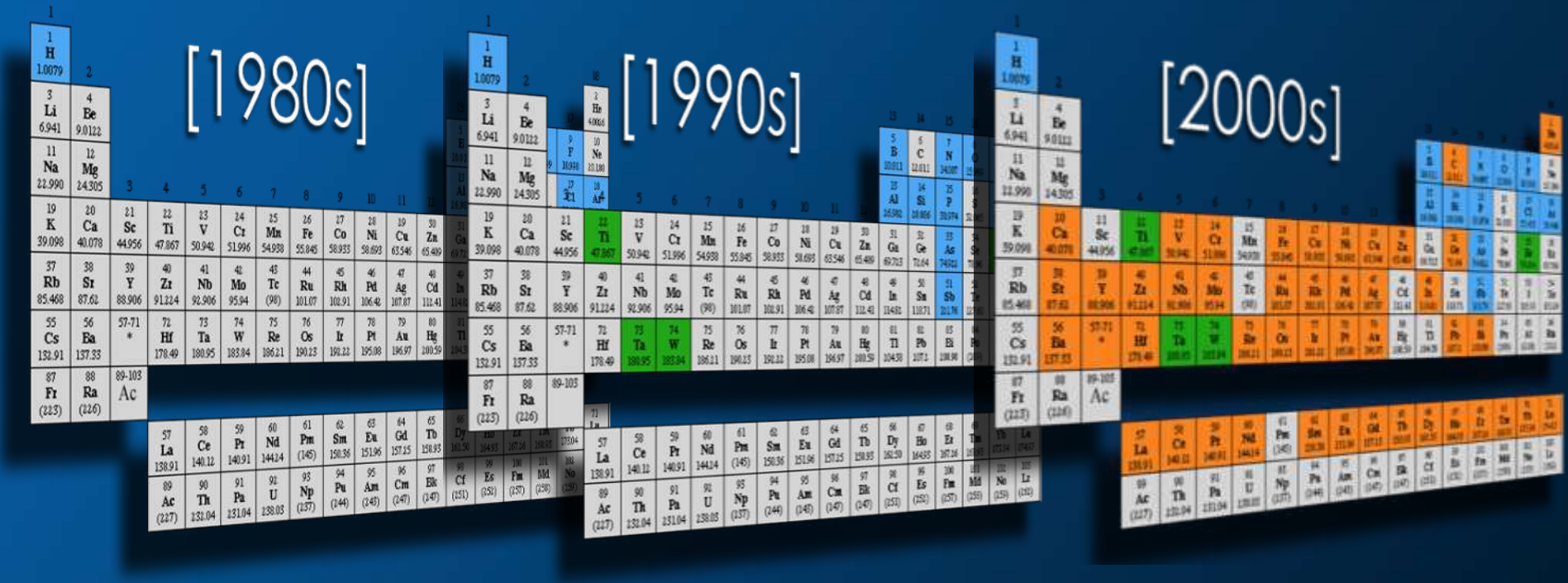
Source: J. Garcia July 2010

Process and Technology Modeling Challenges

- Computational Materials Design
- Device Modeling in Quantum Regime
- Support process to design information transfer for development
- Full-Chip Layout Processing
- Large Scale Computing

Source: Garcia July 2010

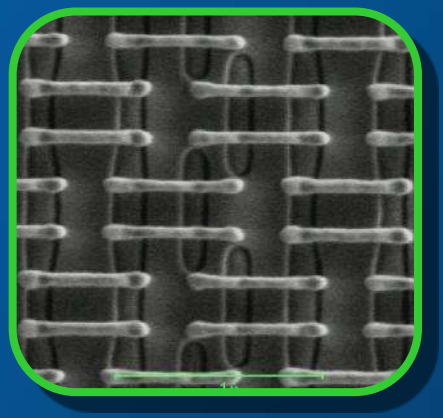
Silicon Technology: Complexity Increasing Exponentially



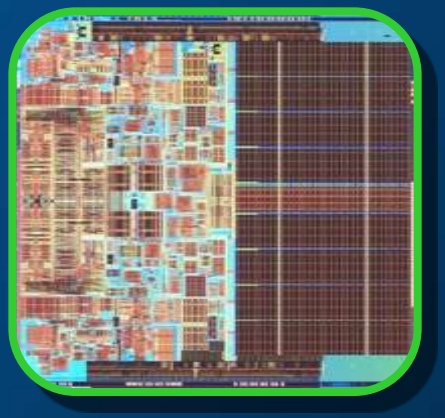
- Number of materials increasing due to highly demanding integration
- Pure materials being replaced by alloys, compounds,& polymers
  - In general, electrical performance drives selection of materials, resulting in weaker mechanical integrity

Source: Shankar, Tech. Lec. Series, 2007

Intel offers the unique opportunity to see them all and work on them all together!

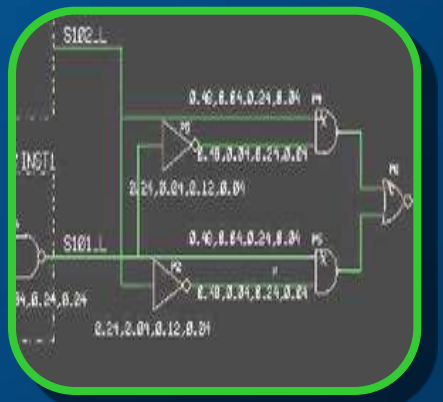


Process

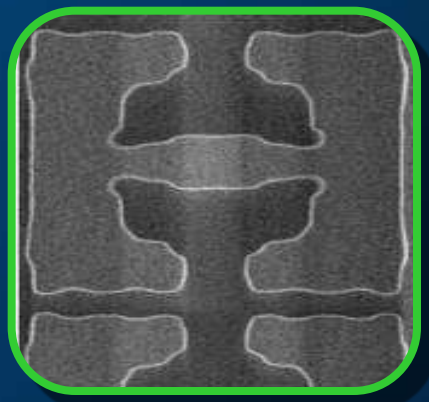


Product

Leading-edge Capacity



Design Tools



Masks

Packaging

intel

Words of Wisdom to Follow

"No exponential is forever … but we can delay 'forever'."

Gordon Moore
ISSCC
2003