EECS 312 Discussion 8

10/29/10

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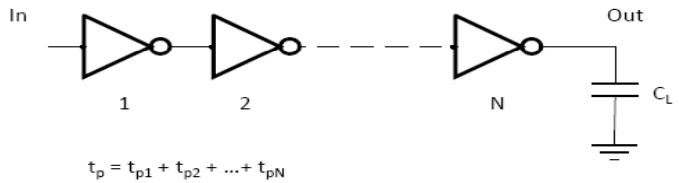
Overview

- Reminder
  - Second section of Lab 3: Due 2 Nov (Tue.)
- Lab 3 Part 2 Help
- Optimal Buffering
- Exercise

Lab 3 Part 2

- Input to the system: a' and b' (ideal step transitions)
  - Your design take a and b as inputs
- $E_{SUPPLY} = \int P(t)dt = V_{DD} \int_{t1}^{t2} I_{SUPPLY}(t)dt$
  - t1, t2: from 10% input transition to 90% output transition (crossing over 0.25V or 2.25V)
  - I_{SUPPLY} can be measured at your VDC
  - Use "Intel" function in the Waveform Calculator
  - Identify the highest energy consumption input transition

Optimal Buffering



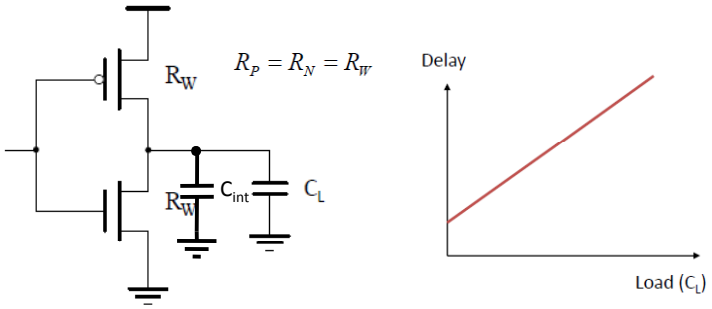
- Objective : Sizing for Performance
- Constraint: Self-loading and Intrinsic Delay

- If C_L is given:
  - How many stages are needed to minimize the delay?
  - How to size the inverters for a given number of stages?

Inverter Intrinsic Delay

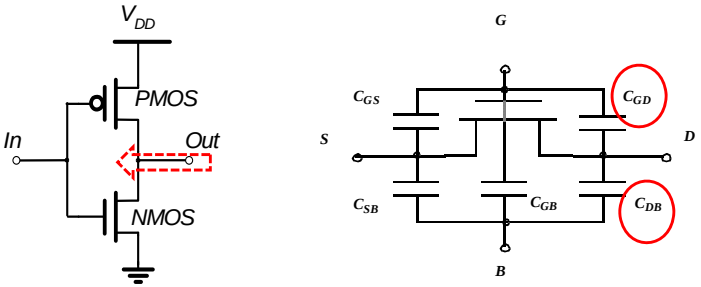
- Assume that for $W_P = 2W_N = 2W_{unit}$
  - same pull-up and pull-down currents
  - approx. equal resistances $R_N = R_P$
  - approx. equal rise t_{pLH} and fall t_{pHL} delays

$t_{pHL} = (\ln 2)\, R_N C_L$ $\quad$ $t_{pLH} = (\ln 2)\, R_P C_L$



Delay = $0.69R_W(C_{int} + C_L) = 0.69R_W C_{int} + 0.69R_W C_L$
= Delay (Internal) + Delay (Load)

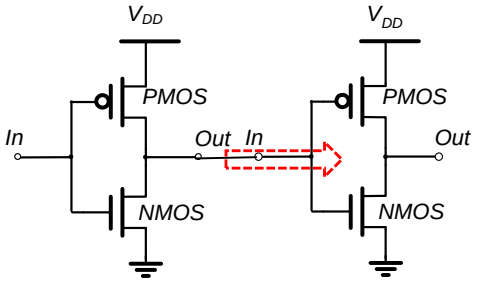
Inverter Intrinsic Capacitances



$C_{GD} = C_{GCD} + C_{GD\text{-}Overlap} = C_{GD\text{-}Overlap}$
but with Miller Effect (will be covered)-> $2C_{GD}$
$C_{DB} = K_{eq} * (C_J L_D W + C_{JW}(2L_D + W))$

Details will be covered in class soon

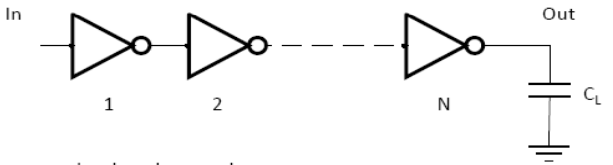
Inverter Gate Load Capacitances



$C_G = C_{GC} + C_{GD\text{-}Overlap} + C_{GS\text{-}Overlap}$
$= C_{ox}L_{eff}W + C_{GDO}W + C_{GSO}W$

Optimal Tapering for Given N

- Stage Delay=$(\ln 2)\cdot R_W (C_{int}+C_L)=(\ln 2)\cdot R_W C_{int}(1+C_L/C_{int})=t_{p0}(1+f/\Upsilon)$
  - $f=C_L/C_g$ – effective fan out, $C_{int}=\Upsilon C_g$



$t_p = t_{p1} + t_{p2} + \ldots + t_{pN}$

$$t_{pj} = t_{p0}\left(1 + \frac{C_{g,j+1}}{\gamma C_{g,j}}\right)$$

$$t_p = \sum_{j=1}^{N} t_{p,j} = t_{p0}\sum_{i=1}^{N}\left(1 + \frac{C_{g,j+1}}{\gamma C_{g,j}}\right),\quad C_{g,N+1} = C_L$$

Optimal Tapering for Given N

- Tapering factor between stages f= $F^{1/N}$
  - F=overall effective fan out = C_L / C_{g1}
  - Each stage has the same effective fanout

    $C_{g,j+1}/C_{g,j} = C_{g,j}/C_{g,j-1} \rightarrow f_j = f_{j-1}$
  - Size of each stage is the geometric mean of two neighbors

    $C_{g,j} = \sqrt{C_{g,j-1}C_{g,j+1}}$
- Minimum path delay
  - t_p=N * t_{p0}(1+f/ϒ)
  - Each stage has the same delay

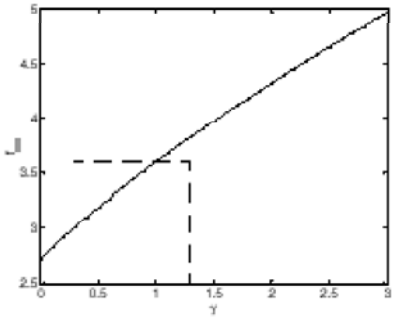
Optimum Number of Stages for a Given F

- Minimum Path Delay: t_p=N * t_{p0}(1+ $F^{1/N}$/ ϒ)
- Optimum Number of Stages:

  N is solution of $\gamma + \sqrt[N]{F} - \frac{\sqrt[N]{F}\ln F}{N} = 0$

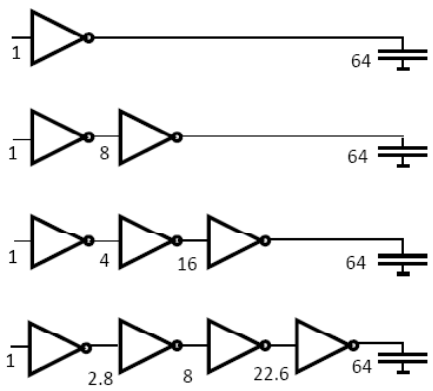
  or N=lnF/lnf where f is given by

  $f = \exp(1+\gamma/f)$



f_{opt} = 3.6 for γ=1

Buffer design example



N	f	t_p
1	64	$65tp_0$
2	8	$18tp_0$
3	4	$15tp_0$
4	2.8	$15.3tp_0$

Exercise

- A 2λ wide inverter with input capacitance C_m must drive a load of $50C_m$. ϒ =0.5. The output signal may be inverted. Derive the optimum delay, # of stages, and sizing.