EECS 312 Discussion 4

10/01/10

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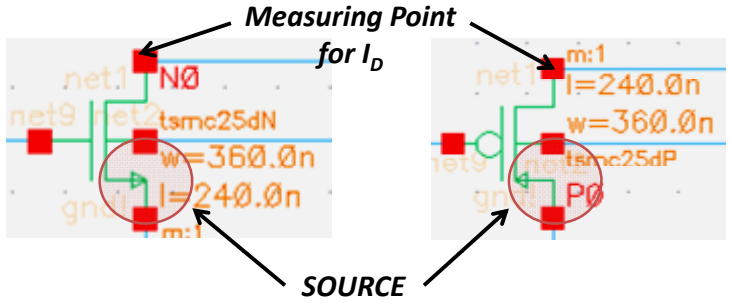
Overview

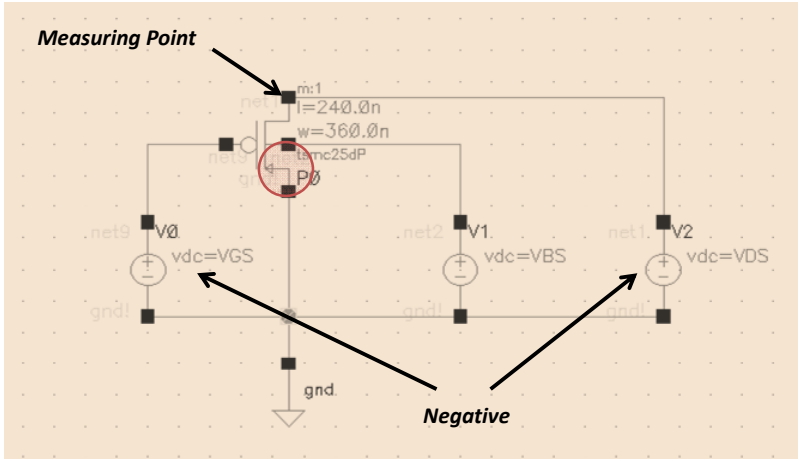
- Reminder
  - Lab Project 2: Due Monday (Oct 4)
  - Office hour: Monday 3:30-5:00pm (CAEN Lab)`
  - In-out box: Outside EECS 2417-G
- Lab Project 2 Help
- CMOS Fabrication

MOSFET Symbol

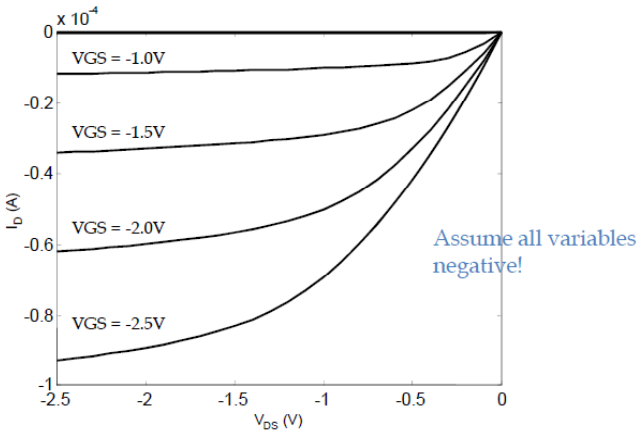
- For both PMOSFETs and NMOSFETs, the arrow is on the source side of the gate, and points in the direction of current
- In the NMOSFET symbol, the arrow points away from the gate
- In the PMOSFET symbol, the arrow points toward the gate



Lab 2 Part2 – PMOS characterization



Lab 2 Part2 – PMOS characterization



Assume all variables negative!

(From lecture slide)

Lab 2 Part 3 – Body Bias

$$I_D = k'\frac{W}{L}\left(V_{GT}V_{min} - \frac{V_{min}^2}{2}\right)(1+\lambda V_{DS}) \text{ for } V_{GT} \geq 0$$

with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$,

$V_{GT} = V_{GS} - V_T$,

and $V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$

- We already have found k', V_{T0}, and λ
- We can obtain I_D from simulation
- Two unknowns – ϒ, ϕ_F
  - $2\phi_F$ is negative in NMOS and positive in PMOS
  - ϒ is positive in NMOS and negative in PMOS
  - If V_{SB}=0, simply V_T=V_{T0}

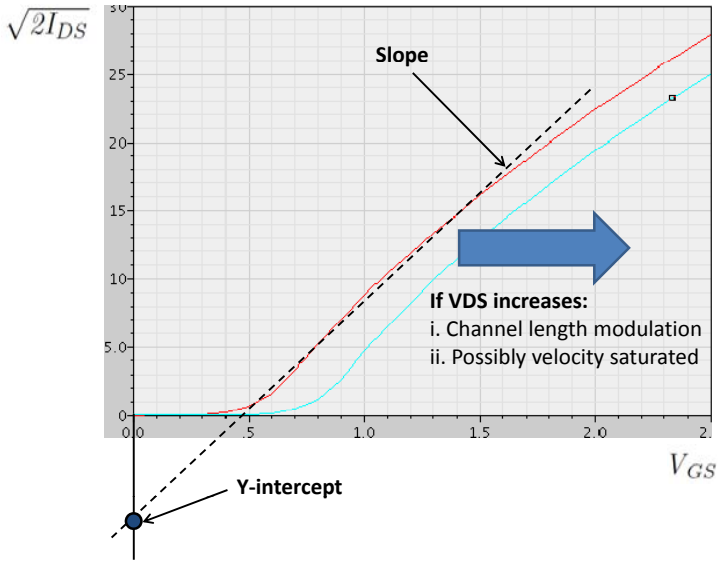
Lab 2 Part 5 – Alternate Method

- Determine V_T and k based on

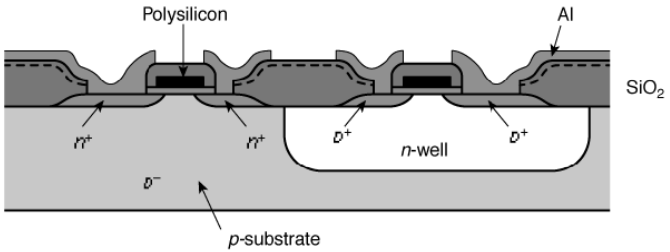
$$I_D = \frac{k'}{2}\frac{W}{L}(V_{GS} - V_T)^2 \quad \text{,so} \quad V_{GS} \propto \sqrt{2I_{DS}}$$

- Drain and gate are shorted forcing V_{DS} = V_{GS} and therefore V_{DS} > V_{GS}-V_{T0} for all V_{GS}, keeping it in saturation but ideally not velocity saturation

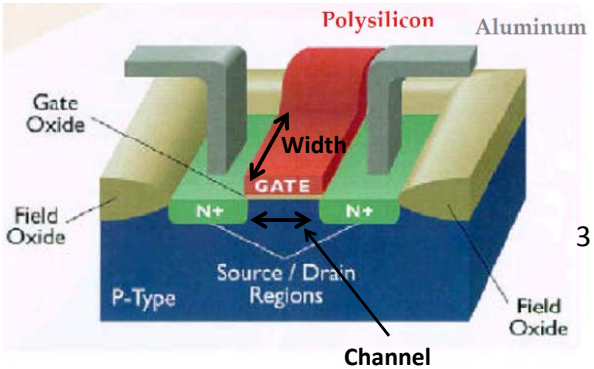
- Take five points along the most linear portion of the curve and use linear regression software to fit a line to them with minimal error.



CMOS Process

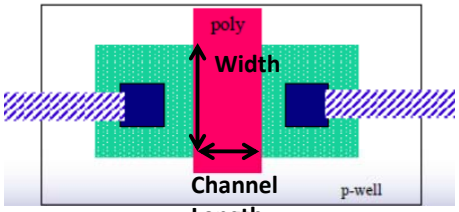


Cross-Sectional View

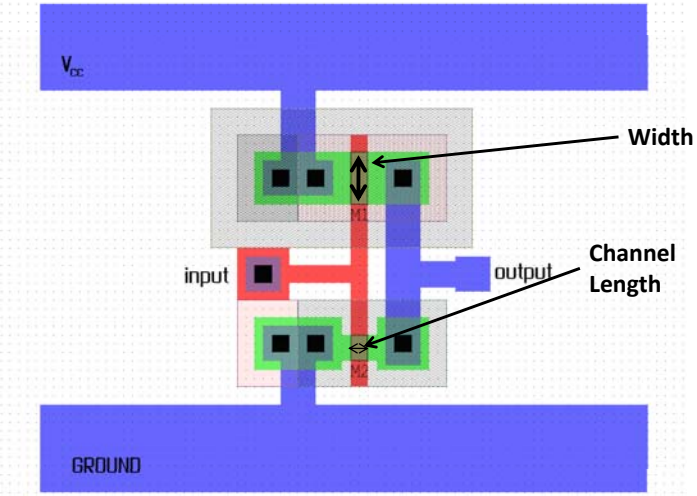


3 Dimensional View

Layout View

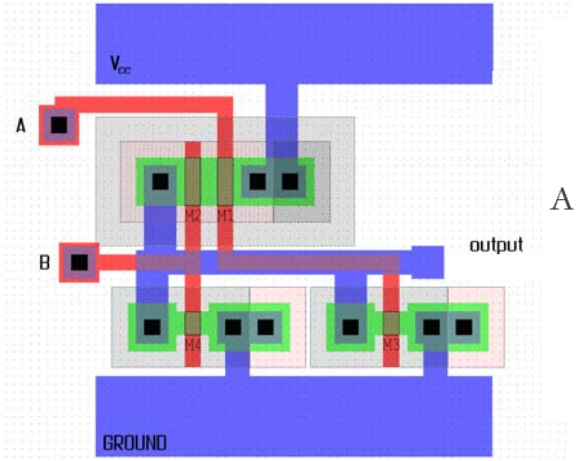


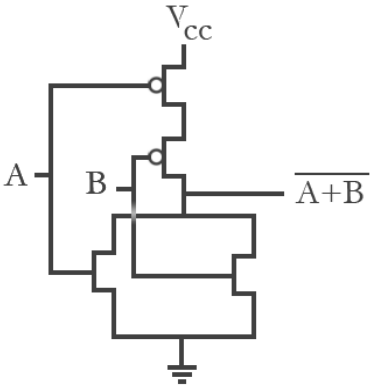
Inverter Layout



Exercise 1

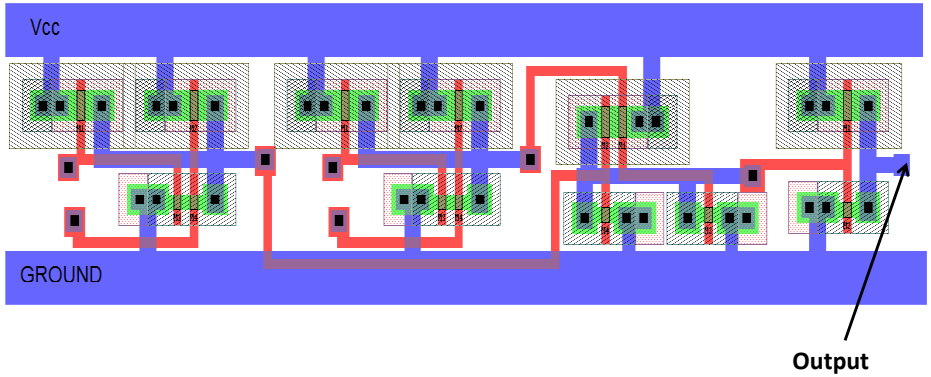
What is this gate?

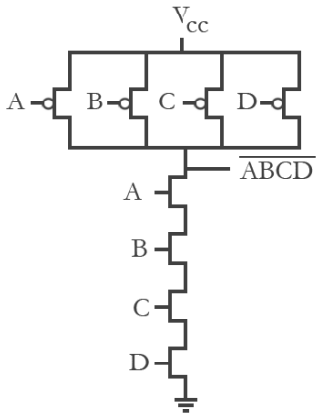


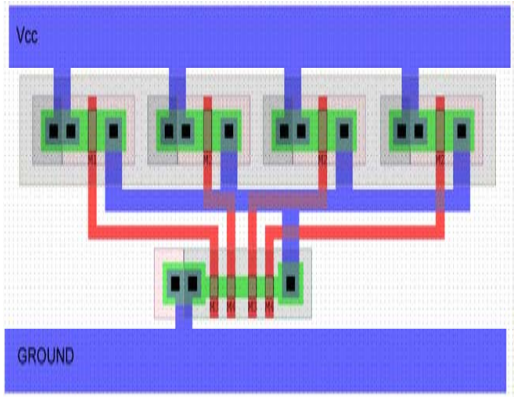


Exercise 2

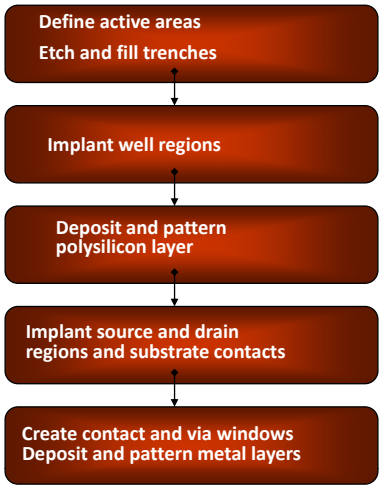
1. **Draw gate-level schematic for the layout**
2. **Decide the functionality**

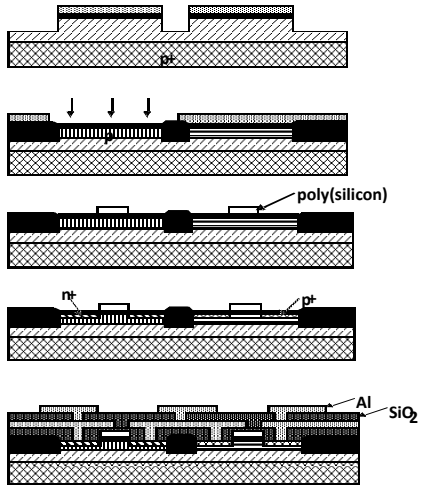






CMOS Process at a Glance





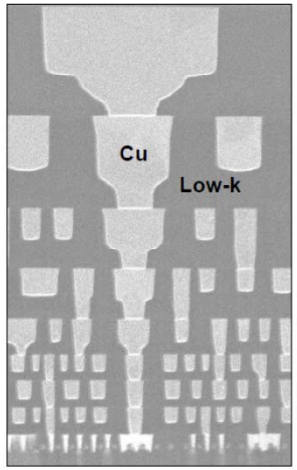
Intel 45nm Interconnects (Cross Section View)

Loose pitch + thick metal on upper layers

- High speed global wires
- Low resistance power grid

Tight pitch on lower layers

- Maximum density for local interconnects



	Pitch (nm)
M8	810
M7	560
M6	360
M5	280
M4	240
M3	160
M2	160
M1	160