EECS 312 Discussion 11

11/15

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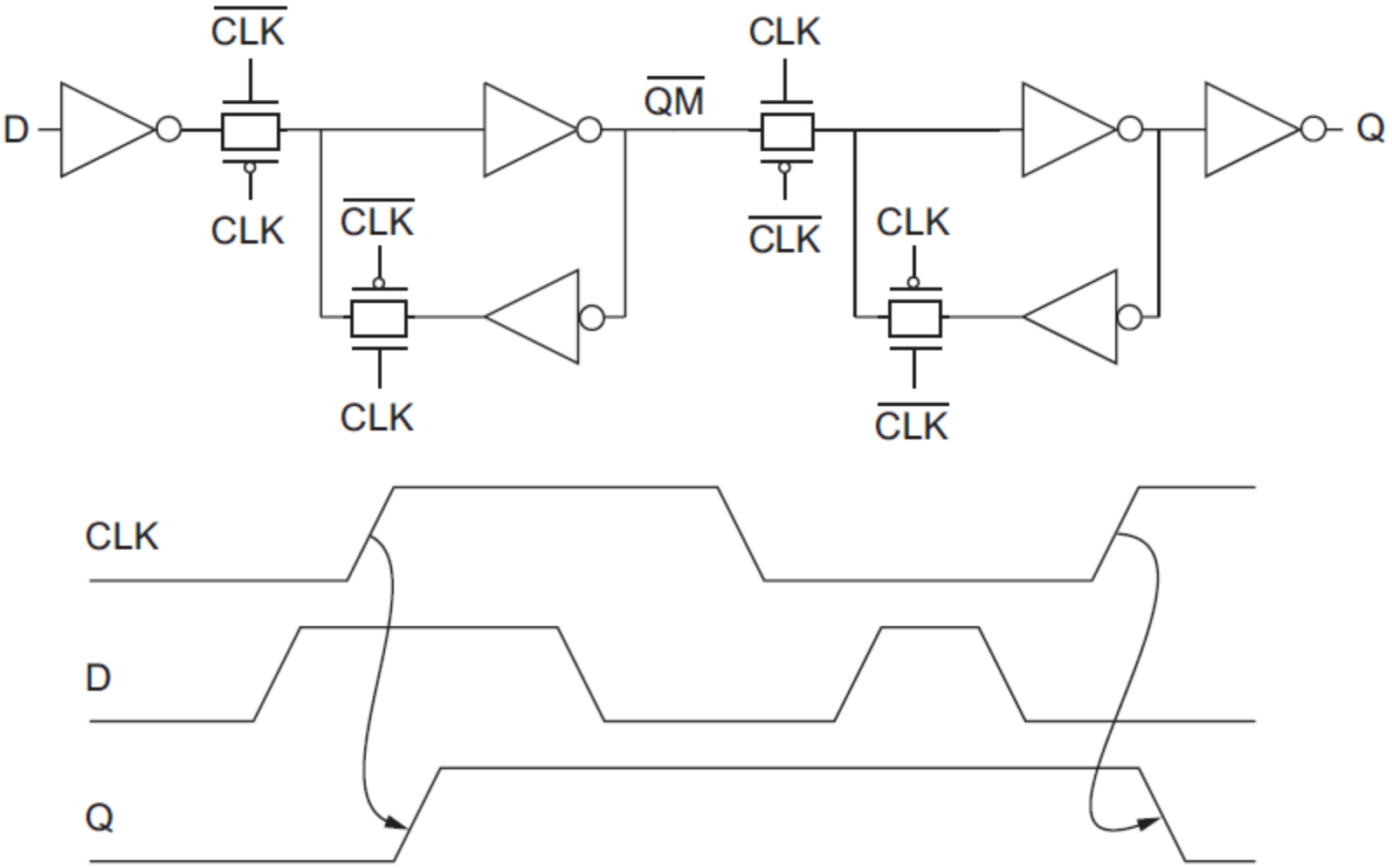
Overview

- Reminder
  - Hw 4: Due Nov 20

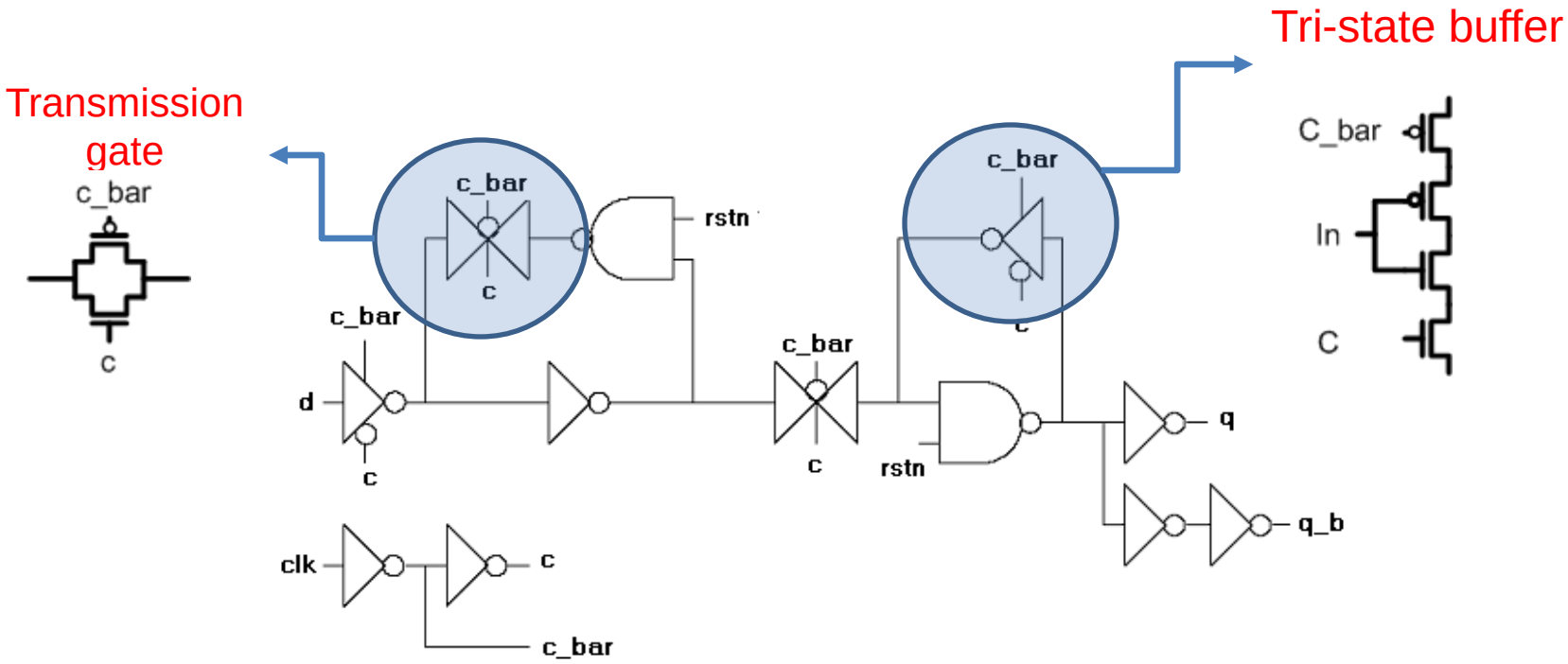
- Sequential Logic

Sequential Logic

Flip-flop (Basics)



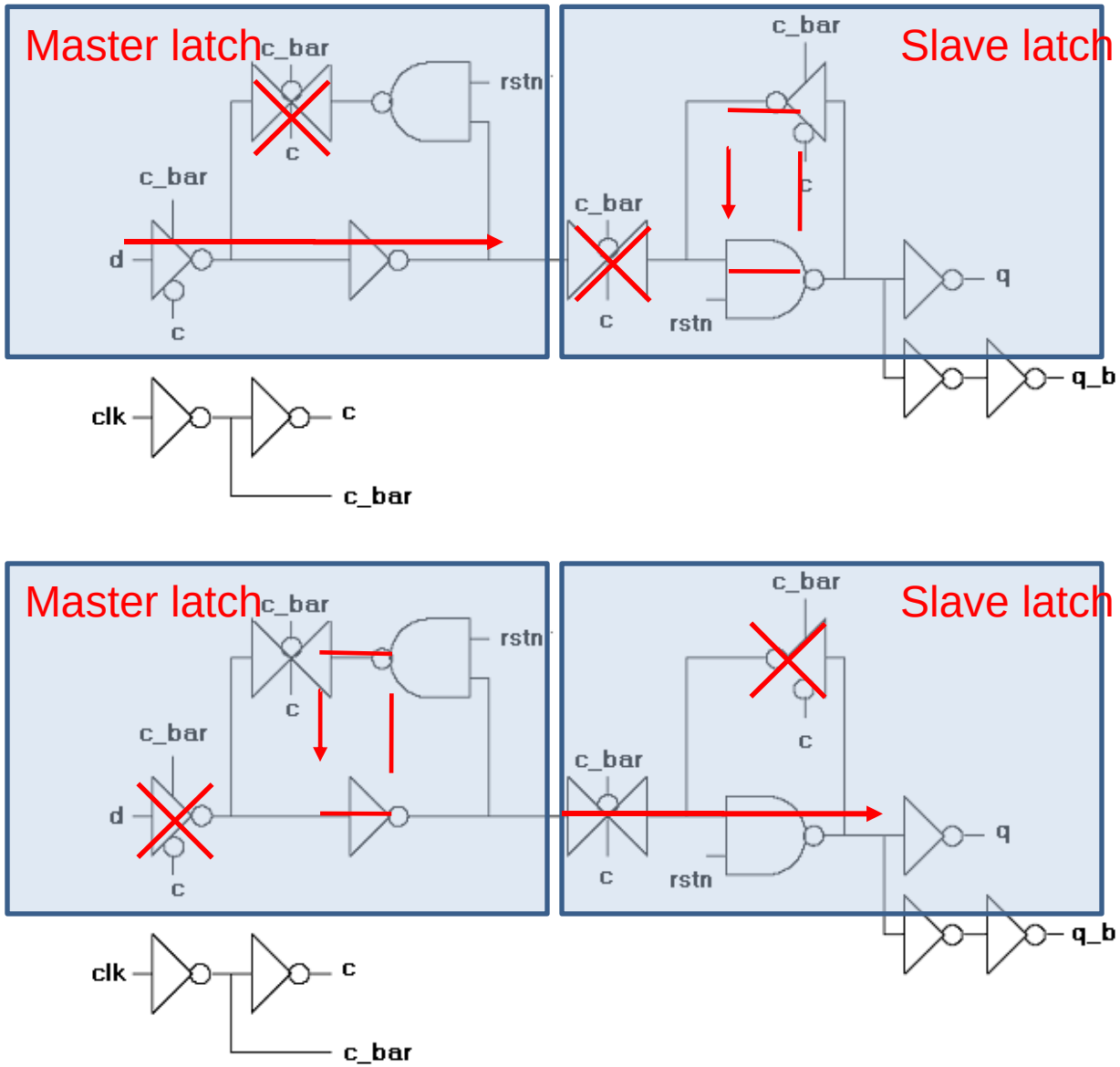
Flip-flop



- Flip Flop with Asynchronous Reset

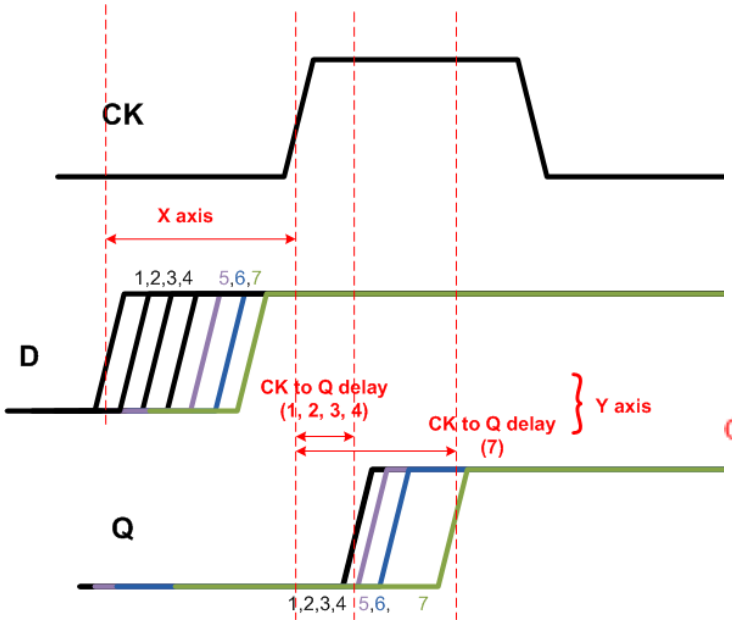
Flip-flop

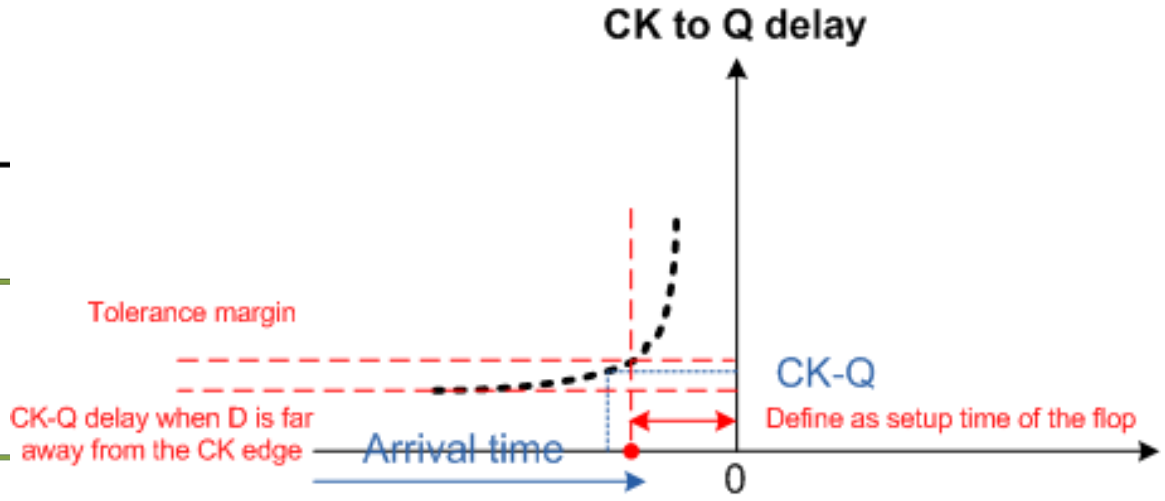
- How it works
  - Divided flip flop into 2 latches (master and slave)
  - When master is transparent, slave holds.
  - When master holds, slave is transparent
  - Capture data at the rising edge of clock



Flip-flop (continued)

- Setup Time
  - As D approaches to CK edge, C-Q delay goes up



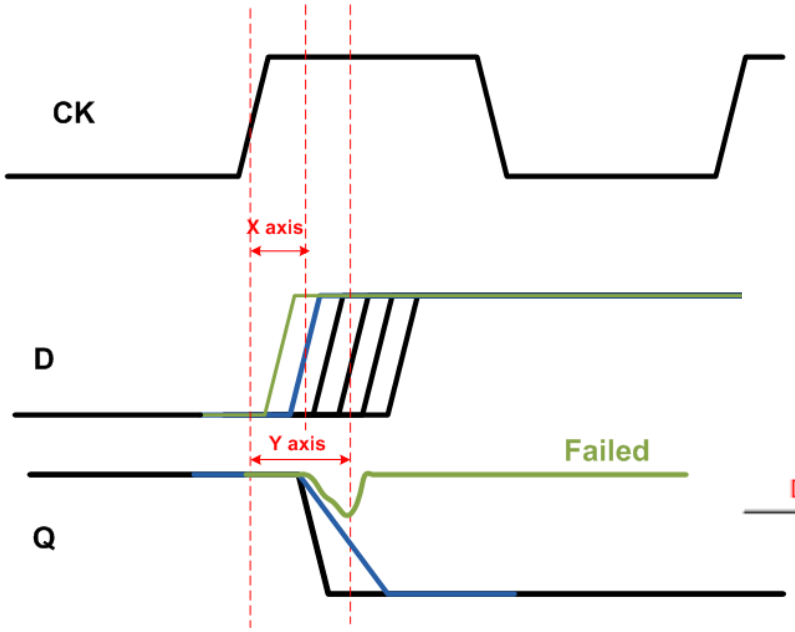


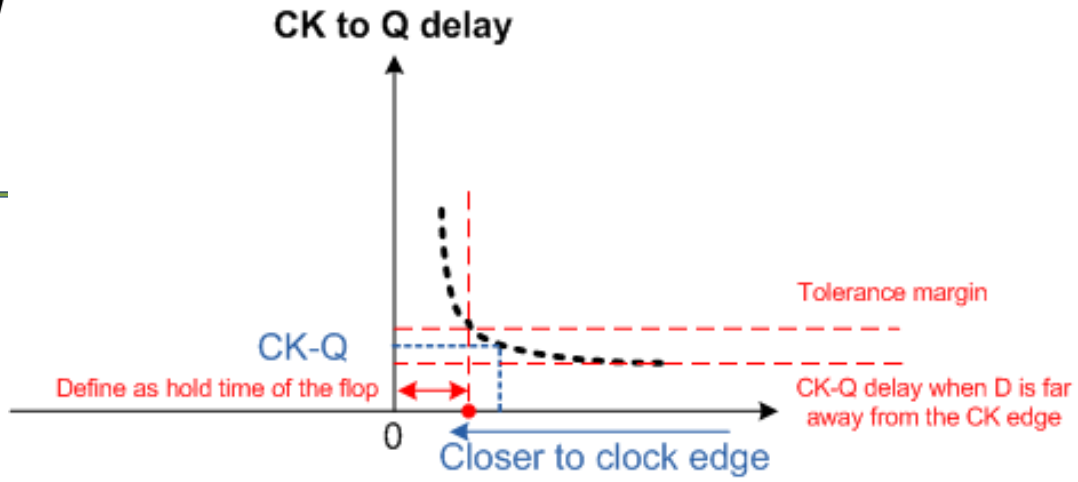
When D arrives after the setup time point, we call it setup time violation

Setup-Time : Point at which CLK-Q delay rises 5% beyond nominal

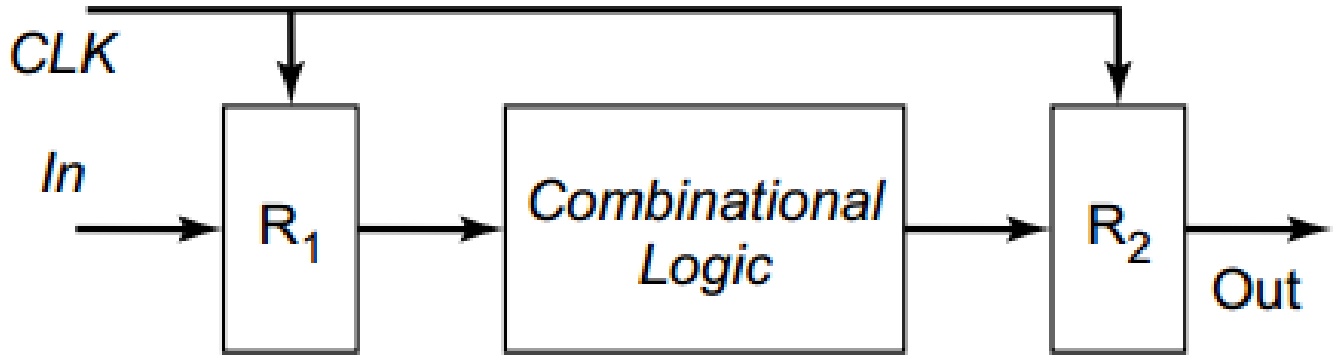
Flip-flop (continued)

- Hold Time
  - Input should be stable for a period of time after the clk edge

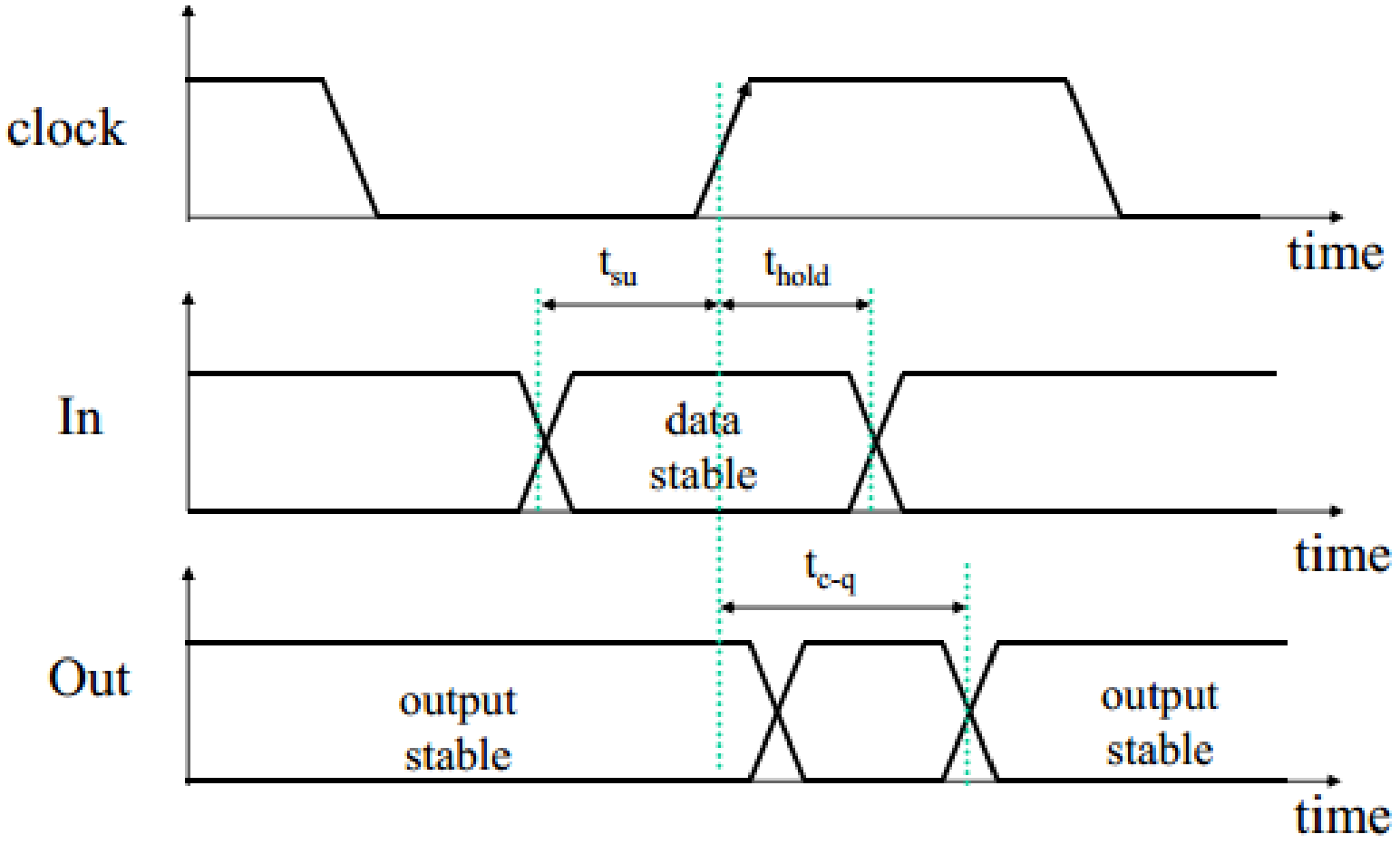




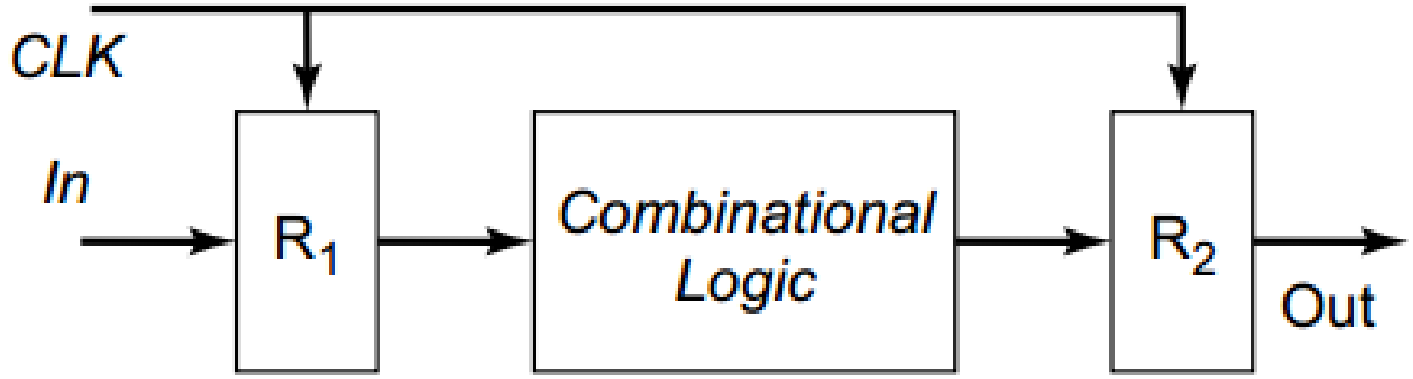
Synchronous Timing



Timing Metrics



Synchronous Timing



$$T_{c\text{-}q} + t_{plogic,min} \geq t_{hold}$$

$$T \geq t_{c\text{-}q} + t_{plogic,max} + t_{su}$$