EECS 312: Digital Integrated Circuits
Final lab project

Teacher:	Robert Dick
Assigned:	14 November
Due:	10 December

1 Assignment

Design a three-bit rising edge-triggered decreasing binary counter with asynchronous preset to 111. After reaching 000, the counter should wrap around to 111. The outputs should be loaded with 300 fF capacitors. The raw asynchronous preset and clock inputs should be inverted. They should be passed through inverters with a NMOSFET widths of 360 nm and PMOSFET widths of 720 nm. Minimize the energy–delay product for the entire system. Determine delay based on the worst-case state transition. Determining energy consumption is more complex. You should use the average energy consumption over all normal counting state transitions; you needn't consider asynchronous preset energy consumption. In order to simplify computing this value, you may assume that the energy consumed when changing multiple bit states is the sum of the energy consumptions for each individual bit state change. This assumption will permit you to simulate a subset of transitions and compute the average energy, instead of simulating all transitions. You may use any design style you prefer. You may also choose any V_{DD}, but may use only one V_{DD} value for the entire system. You needn't consider changes in the preset input when analyzing energy consumption or delay. This counter should be designed for general purpose use. If you would like to use an optimization technique that limits generality, e.g., requires a high clocking frequency to be used for correct operation, please explain your idea and its limitations to me before proceeding.

2 Hints

1. Start by determining the flip-flop circuit structure that will be used for each of the three stages.
2. Although the optimization goal is based on average energy consumption, a design that minimizes worst-case energy consumption will provide a good starting point.

3 Deliverables

1. An indication of the maximum clock frequency for your design and the clock-to-output transition delay.
2. A timing diagram showing the input and all output for a worst-case state transition. When producing timing diagrams, probe the proper post-inverter, not raw, inputs.
3. Schematic.
4. Explanation of the design decisions you made, and justification for them.
5. The product of average energy consumption and worst-case delay for your design.
6. In your report, please indicate which analysis techniques you used. Did results in Cadence agree with those your analysis predicted? If not, what causes could explain the differences?