Q1:
Plasma Etching is more selective (directional etching, anisotropic) compared to wet etching (isotropic) however wet etching can be performed in batch mode (processing many wafers all at once).

Q3:
By using the high k dielectric and keeping all the other parameters constant we can increase transconductance compared to the case with a low k dielectric material. I \sim C_{ox} and C_{ox} = E_{ox}/t_{ox}. By changing silicon dioxide (SiO2) with a high K dielectric material, let’s say y we have I \sim C_y = E_y/T_y and E_y > E_{ox}. Therefore we have more current.

Q4:
A double-gate transistor on an SOI substrate in which the gate is wrapped around the channel.

Q5:
In the question it says: V_{DD}=V\_t; conclusion: this devices is either in cut off or linear region.

a) C_{gcs}, C_{gcd} and C_{gcb} contribute to C_r.

b) V_{gs} < V_t: Cut-off: C_r = C_{gcb} = WLC_{ox}
V_{gs}-V_t < V_{ds}: Saturation: C_r = C_{gcs} = 2/3WLC_{ox}
V_{gs}-V_t > V_{ds}: Linear: C_r = C_{gcs} + C_{gcd} = 1/2WLC_{ox} + 1/2WLC_{ox} = WLC_{ox}

c) t = t_1 + t_2 = C_1 \Delta V_1/l_{in} + C_2 \Delta V_2/l_{in} = WLC_{ox} \cdot V_2/l_{in} + 2/3 \cdot WLC_{ox} \cdot (2V_t-V_t)/l_{in} + WLC_{ox} \cdot (3V_t-2V_t)/l_{in}
   = 8/3 \cdot WLC_{ox} \cdot V_2/l_{in}
Q6:

(a) \( V_{in}=0V \); this implies B is off
No current flows through A, but is on since \( V_{GS}=0 > -0.4V \)
The mode of operation of A is linear as \( V_{GS-V_t} > V_{DS} = 0V \)
(\( V_{out}=2.5V \) as it pulled to VDD)

(b) \( V_{in}=2.5V \) and B is on

(i) First assume both A and B is in linear region:

\[
I_D = k_n' \frac{W}{L} \left[ (V_{GS} - V_t) \right]
\]

Setting two current in two devices equal:

\[
k_n' \frac{W}{L} \left[ (V_{GS_B} - V_t_B) \right] = k_n' \frac{W}{L} \left[ (V_{GS_A} - V_t_A) \right]
\]

(2.5-0.4)\( V_{out}^2/2 = 0.4(2.5-V_{out}) - (2.5-V_{out})^2/2 \)

Doesn’t solve

(ii) Assume B is in saturation while A is in linear:

\[
\frac{1}{2} k_n' \frac{W}{L} (V_{GS_B} - V_t_B)^2 = k_n' \frac{W}{L} \left[ (V_{GS_A} - V_t_A) \right]
\]

(2.5-0.4)\( V_{out}^2/2 = 0.4(2.5-V_{out}) - (2.5-V_{out})^2/2 \)

\( V_{out} = 2.1 \pm 2.062i \), \( 2.1 \pm 2.062i \) → Complex, Not good.

(iii) Assume B is in linear while A is in saturation:

\[
k_n' \frac{W}{L} \left[ (V_{GS_B} - V_t_B) \right] = \frac{1}{2} k_n' \frac{W}{L} (V_{GS_A} - V_t_A)^2
\]

(2.5-0.4)\( V_{out}^2/2 = \frac{1}{2} (0.4)^2 \)

\( V_{out} = 0.038V, 4.16V (>V_{DD}) \)

Check B is in linear: \( 2.5-0.038 > V_t \) → o.k.

Check A is in saturation: \( 0-(2.5-0.038) < V_t \) → o.k.

(c) \( P_{avg} = 2.5V \cdot I_D \cdot 0.7 \ (V_{in}=2.5V) + 2.5V \cdot 0 \cdot 0.3 \ (V_{in}=0V) \)

\[= 2.5V \cdot ( \frac{1}{2} k_n' \frac{W}{L} (0.4)^2 ) \cdot 0.7 = 0.14 \cdot k_n' \frac{W}{L} \text{ Watt} \]

Q7:

(a) \( P_{dynamic} = CV^2 f_{0,>1} \)
\( P_{clock} = 10000 \cdot 40fF \cdot 2.5V^2 \cdot 1GHz = 2.5W \)
\( P_{comb} = 50000000 \cdot 6fF \cdot 2.5V^2 \cdot (0.1 \cdot 1GHz \cdot 0.5) = 9.375W \rightarrow f_{0,>1} = 0.5 \cdot 1GHz \cdot 0.5 \)
\( P_{\text{dynamic}} = P_{\text{clock}} + P_{\text{comb}} = 11.875 \text{W} \)

\( \text{Time}_{\text{depletion}} = \frac{E_{\text{battery}}}{P_{\text{dynamic}}} = \frac{39 \text{W} \cdot \text{hr}}{11.875 \text{W}} = 3.28 \text{ hours} \)

(b) \( I_{\text{off}} (I_{\text{DS}}@V_{\text{GS}}=0) \) is given as \( 10^{-10} \text{A} \) for \( V_t=0.5 \text{V} \)

Determine \( I_{\text{off}} \) when \( V_t=0.25 \text{V} \)

Note that \( V_t \) shift corresponds with a shift of \( I_{\text{DS}} \) vs. \( V_{\text{GS}} \) graph

Slope of sub-threshold region is 90 mV/dec and shifting the sub-threshold line left by 250mV will increase the off current by \( 250 \text{mV}/90 \text{mV}=2.78 \text{dec} \)

Therefore \( I_{\text{off}} @ V_t=0.25 \text{V} \)

\[ I_{\text{off}} = 10^{-10} \cdot 10^{2.78} = 6.026 \cdot 10^{-8} \text{A} \]

\( P_{\text{static}} = I_{\text{static}} \cdot V = 5010000 \cdot 6.026 \cdot 10^{-8} \cdot 2.5 \text{V} = 0.391 \text{W} \)

\( P_{\text{total}} = P_{\text{dynamic}} + P_{\text{static}} = 2.00 \text{W} \)

\( \text{Time}_{\text{depletion}} = \frac{E_{\text{battery}}}{P_{\text{total}}} = \frac{39 \text{W} \cdot \text{hr}}{2 \text{W}} = 19.5 \text{ hours} \)

% reduction = \( (3.28-3.09)/3.28 = 5.79\% \)

(C) From Fig. 5-17 @ \( V_{\text{DD}}=1.3 \) normalized \( t_p \) is \( \sim 2 \). That is, propagation delay has doubled so peak frequency has to be halved. The operating clock frequency = \( 0.5 \cdot 1 \text{GHz} = 500 \text{mHz} \)

\( P_{\text{dynamic}} = P_{\text{clock}} + P_{\text{comb}} = 100000 \cdot 40 \text{fF} \cdot 1.3 \text{V}^2 \cdot 500 \text{mHz} = 1.61 \text{W} \)

\( P_{\text{static}} = 5010000 \cdot 6.026 \cdot 10^{-8} \text{A} \cdot 1.3 \text{V} = 0.391 \text{W} \)

\( P_{\text{total}} = P_{\text{dynamic}} + P_{\text{static}} = 2.00 \text{W} \)

\( \text{Time}_{\text{depletion}} = \frac{E_{\text{battery}}}{P_{\text{total}}} = \frac{39 \text{W} \cdot \text{hr}}{2 \text{W}} = 19.5 \text{ hours} \)

(d) \( P_{\text{dynamic}} = P_{\text{clock}} + P_{\text{comb}} = 100000 \cdot 40 \text{fF} \cdot 2.5 \text{V}^2 \cdot 500 \text{mHz} + 5000000 \cdot 6 \text{fF} \cdot 2.5 \text{V}^2 \cdot 0.10 \cdot 500 \text{mHz} = 5.94 \text{W} \)

\( P_{\text{static}} = 5010000 \cdot 6.026 \cdot 10^{-8} \text{A} \cdot 2.5 \text{V} = 0.75 \text{W} \)

\( P_{\text{total}} = P_{\text{dynamic}} + P_{\text{static}} = 6.69 \text{W} \)

\( \text{Time}_{\text{depletion}} = \frac{E_{\text{battery}}}{P_{\text{total}}} = \frac{39 \text{W} \cdot \text{hr}}{6.69 \text{W}} = 5.83 \text{ hours} \)

Q10:

\( V_{\text{instantaneous}} = V_{\text{final}} + (V_{\text{initial}} - V_{\text{final}}) \cdot e^{-t/RC} \)

(a) By replacing the PMOSFET with 3.8kΩ,

\( V_{\text{DD}}/2 = 0 - (V_{\text{DD}} - 0) \cdot e^{-t/3.8 \text{k}\Omega \cdot 73.2 \text{fF}} \)

\( t = \ln(2 \cdot 3.8 \text{k}\Omega \cdot 73.2 \text{fF}) = 0.693 \cdot 2.782 \cdot 10^{-10} = 192.81 \text{ps} \)
(b) PMOSFET will be cut-off when $V_{GS} > V_t$ and for a PMOSFET, the terminal with the higher voltage is source between source and drain terminals. In this problem, the terminal connected to $C_l$ will have the higher voltage, so it works as a source terminal.

The PMOSFET will continue to discharge the $C_l$, but if $C_l$ is discharged to $|V_{TP}| = 0.5V$, the PMOSFET will be cut-off since $V_{GS} = 0$ - $V_S = -V_{CL} > V_t = -0.5V$
Therefore the final voltage of the capacitor is $|V_{TP}| = 0.5V$

(c) Since we assumed resistor-switch model, the final voltage is still 0. In this equation, we assume there is a sudden change in resistance to infinity when PMOS cuts-off.
$$0.5 = 0 - (V_{DD} = 0) e^{-t/3.8k\Omega \cdot 73.2fF}$$
$$t = \ln 5 \cdot 3.8k\Omega \cdot 73.2fF = 0.693 \cdot 2.782 \cdot 10^{-10} = 447.68\text{ps}$$

(d) Resistor-switch model assumes a constant resistance (3.8KΩ) during a transition before cut-off and a step change in resistance to infinity as the PMOSFET becomes cut-off. However, with a real PMOSFET, on-resistance increases gradually with decreasing $|V_{gs}|$. Since $R$ is a function of time that is monotonically increasing, RC time constant and delay will increase over a transition. Therefore, the delay calculated with resistor-switch model may be optimistic. i.e., with a real PMOSFET, it takes more time to get to the final voltage due to long tailed transition.