# Homework Two

EECS 312: Digital Integrated Circuits
Fabrication and MOSFETs

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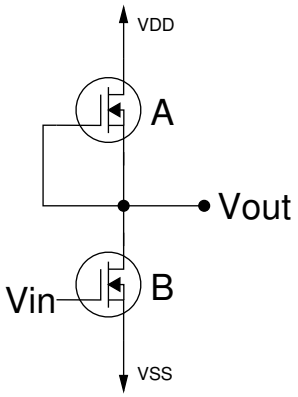
Due 10 October

You may discuss the assignment with your classmates. However, you need to understand and write the solutions independently. Please stop by in office hours, ask questions in class, and use the discussion list for clarification and help. Don't be shy about asking for more information or help.

1. **(5 pts.)** What advantage does plasma etching have over wet etching? Use at most one sentence.
2. **(5 pts.)** What are the advantages of using high-$\kappa$ dielectric material is deep-submicron process technologies, and where is it used (at most two short sentences)?
3. **(5 pts.)** What are the advantages of using low-$\kappa$ dielectric material is deep-submicron process technologies, and where is it used (at most two short sentences)?
4. **(5 pts.)** Use one sentence to define "FinFET".
5. **(20 pts.)** Consider a CMOS process with the following capacitive parameters for the NMOS transistor: $C_{GSO}$, $C_{GDO}$, $C_{OX}$, $C_J$, $m_j$, $C_{jsw}$, $m_{jsw}$, $C_O$, and $\phi_b$, with the lateral diffusion equal to $L_D$. The MOS transistor M1 is characterized by the following parameters: $W$, $L$, $A_D$ (drain area), $P_D$ (drain perimeter), $A_S$ (source area), $P_S$ (source perimeter). $V_{DD}$ is equal to $V_t$ (the threshold voltage of the transistor). Assume that the initial value of $V_{GS}$ is 0 V and that $V_{DS} = V_{DD}$. A current of $I_{in}$ flows into the gate, starting at time 0 s.
   (a) Assume all the capacitance at the gate node can be lumped into a single, grounded, linear capacitance $C_T$. Among $C_{db}$, $C_{sb}$, $C_{gcs}$, $C_{gcd}$, and $C_{gcb}$, which contribute to $C_T$?
   (b) For those that contribute to $C_T$, give the expression that determines the value of the contribution. Use only the parameters given above. If the transistor goes through different operation regions and this impacts the value of the capacitor, determine the expression of the contribution for each region (and indicate the region).
   (c) Assuming that all the capacitance at the gate node can be lumped into a single grounded linear capacitance $C_T$, derive an expression for the time it will take for $V_{GS}$ to reach 3 $V_t$. Hint: the transistor goes through two operating regions as $V_{GS}$ charges from 0 V to 3 $V_t$.
6. **(10 pts.)** Consider the circuit below.




Device B is a standard NMOSFET. Device A has the same properties as B, except that its device threshold voltage, $V_T$ is -0.4 V (it is negative). Assume that all the current equations and inequality equations (to determine the mode of operation) for the depletion device A are the same as an enhancement-mode NMOSFET. $V_{DD} = 2.5\,\text{V}$.

(a) If $Vin = 0\,\text{V}$, what is $Vout$? In steady state, what is the mode of operation for device A?

(b) Compute the output voltage for $Vin = 2.5\,\text{V}$.

(c) If $Vin$ is 0 V 30% of the time and 2.5 V 70% of the time, what is the average static power dissipation of this circuit?

7. **(10 pts.)** Consider an IC designed for portable applications such as a laptop computer. The system is designed with a 39 Watt-hour battery and you may assume that the IC is the only device consuming any power from the battery. The IC contains a clocked network with 10,000 nodes (assume all inverters) with an average capacitive load (CL) of 40 fF, and another 5 million un-clocked nodes (assume all inverters) with capacitive loads of 6 fF and a switching activity $\alpha_{SW} = 0.10$. The IC has a $V_{DD}$ of 2.5 V and is clocked at a frequency of 1 GHz. Assume that the average device width is 4 µm. Use $V_T$ = 0.25 V and subthreshold swing, SS = 90 mV/decade. Please use $n$=1.5 (from page 99) and lambda from page 103. You may use an off current of $10^{-10}$ A at a threshold voltage of 0.5 V for the 4 µm wide devices in order to compute $I_S$ (at $V_T = 0.25\,\text{V}$). Use the default technology for any additional parameters needed.

(a) Considering only dynamic power consumption, calculate the power consumption of the IC and the amount of time before a fully charged battery is depleted.

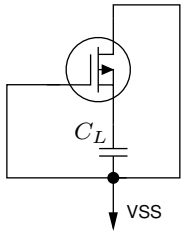
(b) To obtain a more accurate estimate of battery life, now consider the added impact of subthreshold current. Calculate the static power consumption of the IC, assuming all nodes are driven by inverters. Recalculate the amount of time required to discharge a fully charged battery. By what percentage is the battery life reduced compared to (a)?

(c) Calculate the power consumption (static and dynamic) when the supply voltage is reduced to 1.3 V. You may assume that there is no timing slack at 1 GHz and that the frequency must, therefore, be reduced along with the voltage. You may use Figure 5–17 from the textbook to determine the resulting change in frequency, assuming that the delays of all combinational paths

scale in proportion to the delay of an individual inverter. How long does a battery charge last with reduced voltage and frequency?

(d) Calculate the power consumption (static and dynamic) when the frequency of the IC is reduced by the same amount implied by the previous question but $V_{DD}$ remains 2.5 V. How long does the battery last with reduced frequency?

8. In the following circuit the capacitance of $C_L$ is 73.2 fF. $C_L$ is initially charged to 2.5 V. At time zero, its gate is attached ground, as shown in the figure. $V_{TP}$ = -0.5 V. You may ignore the effects of leakage.




(a) **(3 pts.)** If we replace the PMOSFET channel with a 3.8 kΩ resistor, how long does it take for the capacitor to discharge to $V_{DD}/2$?

(b) **(3 pts.)** If we consider transistor cut-off, what is the final voltage of the capacitor?

(c) **(3 pts.)** Based on a resistor–switch model, how long does it take for the capacitor to get to this final voltage?

(d) **(3 pts.)** Using no more than three sentences, and/or a plot, indicate the main difference(s) between the voltage as a function of time curve for the resistor–switch model and a real PMOSFET.

9. **(0 pts.)** Review your work on Lab 2. I was considering asking you to essentially repeat derivation of MOSFET parameters for practice. However, you did this a lot in the lab assignment already. Make sure you have not forgotten how.