

EECS 312: Digital Integrated Circuits  
Midterm Exam

24 November 2009

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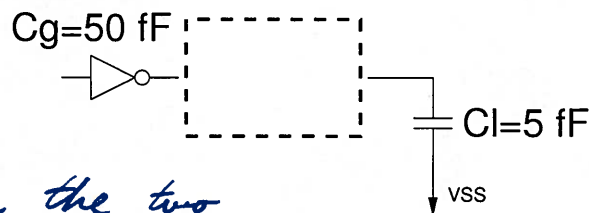
Show your work. Derivations are required for credit; end results are insufficient.  
Closed book. No electronic mental aids. One side of one 8.5×11 inch page of notes may be used during the exam. permitted.

Honor Pledge: I have neither given nor received aid in this exam.

Signature:

## 1 Qualitative questions

1. (10 pts.) What is the optimal number of inverter stages to use between the fixed-capacitance inverter and the load in the following circuit? Using no more than three sentences, explain your answer.



0. Consider the two cases. Adding an inverter w.  $C_g > 5 \text{ fF}$  will increase prop. delay. Adding an inverter w.  $C_g \leq 5 \text{ fF}$  will increase the delay of driving (i.e.

Or

$$\lceil \ln(5 \text{ fF} / 50 \text{ fF}) \rceil \leq 0.$$

2. (10 pts.) List two advantages of ratioed logic, and two disadvantages of ratioed logic.

advantages: (1) less area due to fewer transistors and (2) less driven capacitance.

disadvantages: (1) High static power consumption when output low and inability to produce 0V output.

3. (10 pts.) For each of the following types of load, indicate the scales (e.g., gate-level) at which the type of load will have a significant impact on circuit behavior:

(a) Resistive,

*All levels above gate level. Transistor R is important at all levels, but we are considering load*

(b) Capacitive, and *here.*

*all the way down to transistor level.*

(c) Inductive.

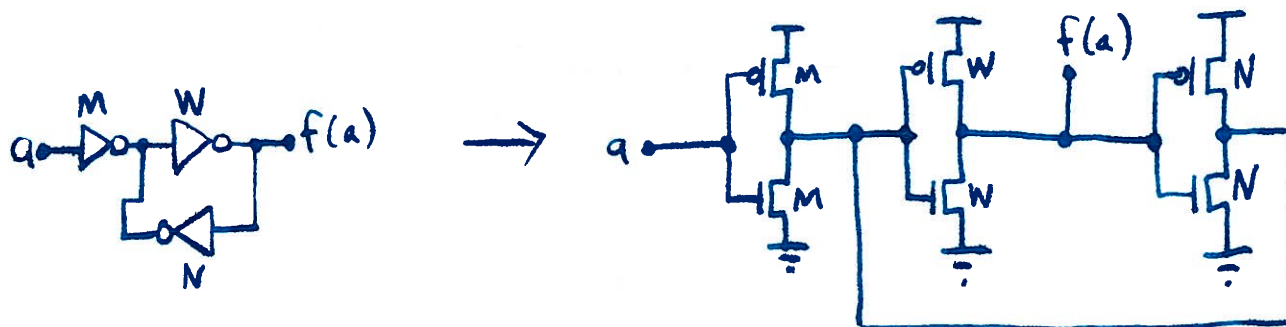
*Package - PCB level.  
maybe a problem for very long global interconnect*

4. (10 pts.) What trend has caused the importance of inter-wire coupling capacitance, relative to substrate coupling capacitance, to increase?

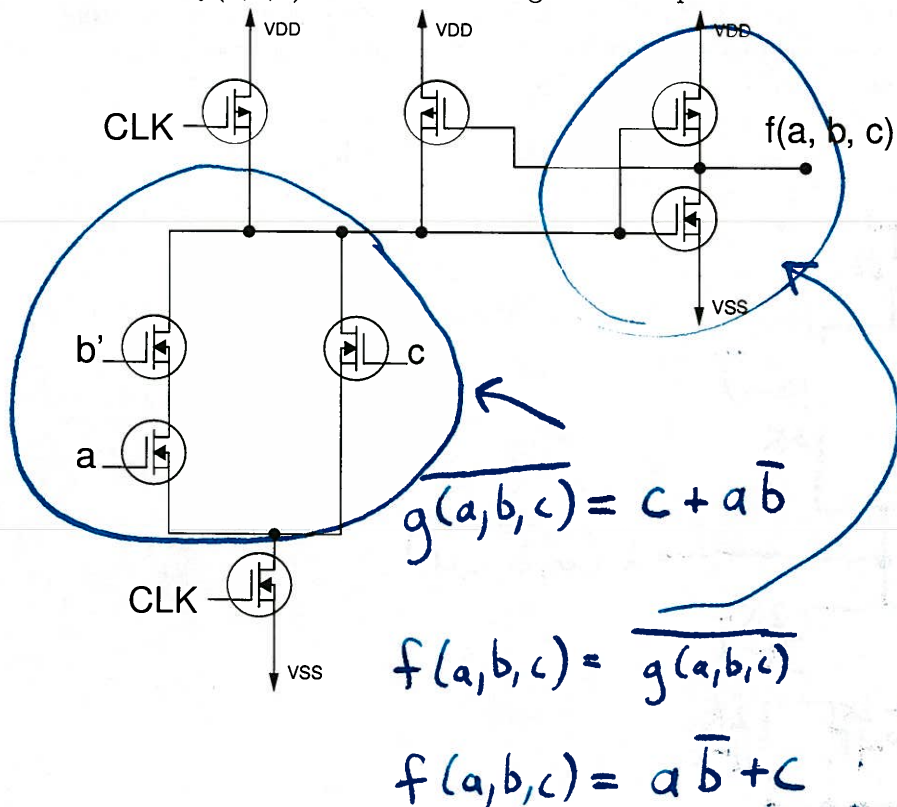
*Increasing interconnect aspect ratio.*

## 2 Quantitative questions

5. (10 pts.) Draw the schematic for a non-inverting Schmitt trigger buffer composed entirely of NMOSFETS and PMOSFETS, i.e., if you need a resistor, use a MOSFET instead. You needn't specify precise transistor sizes, but may specify that individual transistors are wide (use  $W$ ), medium (use  $M$ ), or narrow (use  $N$ ). It is understood that PMOSFETs will have twice the width of NMOSFETs with the same label. When the output of your design changes, this should have little impact on the previous gate, i.e., the gate driving your design, so be sure to have a high resistance at the input of your gate.



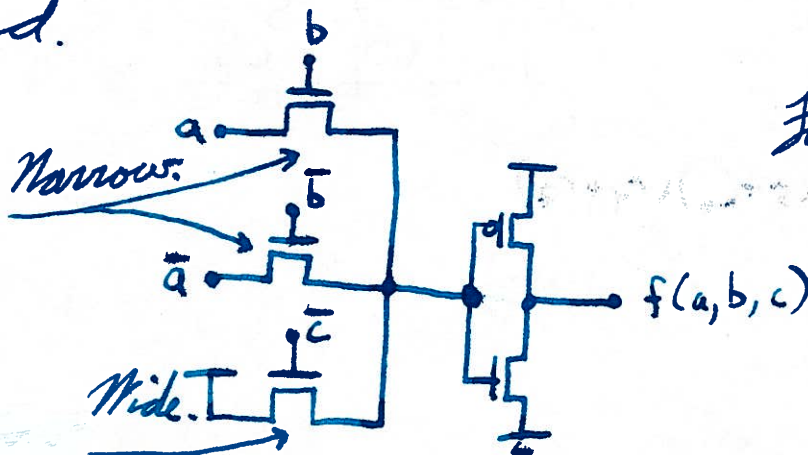
6. (10 pts.) What function  $f(a, b, c)$  does the following circuit implement?



7. (10 pts.) Implement the following function using the minimal number of transistors. The output of your implementation should have full output range, from  $V_{SS}$  to  $V_{DD}$ . However, it needn't be particularly fast. You may use literals as direct inputs.

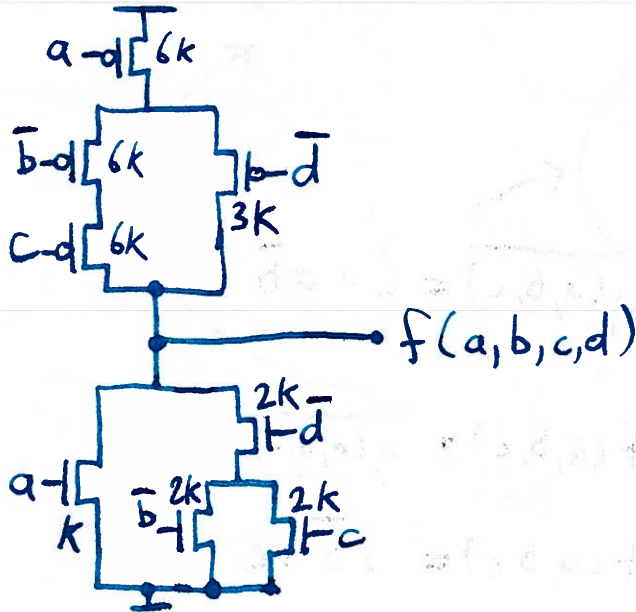
$$f(a, b, c) = (a\bar{b} + \bar{a}b)c$$

Most or full credit was given for same designs w.  $\leq 8$  transistors. However, I wanted to see how far this could be pushed.

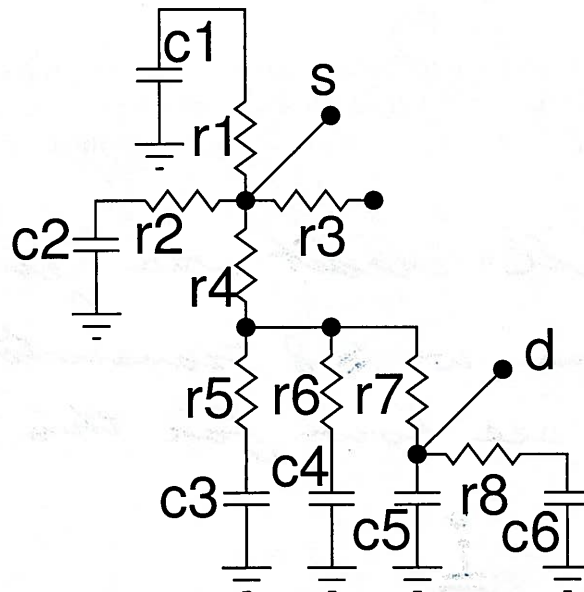


8. (10 pts.) Implement the following function as a single logic gate. Indicate the widths of all gates in terms of  $k$ , the minimal gate width. Size the transistors to achieve the same worst-case resistance as a balanced, minimal width inverter (i.e., an inverter with a  $k$ -wide NMOSFET and a  $2k$ -wide PMOSFET).

$$f(a, b, c, d) = \bar{a}(b\bar{c} + d)$$



9. (10 pts.) What is the Elmore delay time constant for the response at node  $d$  to a change at node  $s$  in the following circuit?



$$\begin{aligned} \tau &= C_3(r_4) + C_4(r_4) + \\ &C_5(r_4 + r_7) + \\ &C_6(r_4 + r_7) \end{aligned}$$

$$\tau = (C_3 + C_4)r_4 + (C_5 + C_6)(r_4 + r_7)$$