1 Knowledge

1. (5 pts.) What problem can the inductance in the PCB and package power delivery network cause? When does this problem occur? Use at most four sentences.

2. (10 pts.) Why was there a recent transition from using polysilicon gates to using metal gates? Use at most three sentences.
3. **(10 pts.)** Show the side view of the basic memory element used in an EPROM. Using at most two sentences, explain the process of programming it. Using at most two sentences, explain the process of erasing it.

4. **(10 pts.)** What does this layout show? What is its greatest performance irregularity or flaw? In other words, if you were to implement the same function, how would your solution differ? Use at most four sentences.
5. (10 pts.) List one problem caused by hot carriers and one profitable use of them. Use at most four sentences.

6. (5 pts.) What controls whether carbon nanotubes are metallic or semi-conducting? Use at most one sentence.

2 Analysis and Design

7. (10 pts.) You designed a CMOS inverter to have a $V_M = V_{DD}/2$. However, its fabrication was not perfect. Impurities mixed in with the acceptor ions introduced strain in the NMOSFET, increasing its carrier mobility by 50%. What is the impact on $V_M$?
8. (10 pts.) Generalize the concept of carry-select addition to multiplication. Show the diagram of a carry-select combinational multiplier for two 3-bit numbers. Indicate the impact on performance, assuming that the MUX overhead is negligible. You may use boxes labeled HA, FA, and MUX without showing their transistor-level designs.
9. **(15 pts.)** Draw a diagram of an SRAM with 16 addresses, each of which stores one bit. Take your design down to transistor level, but use hierarchy. Focus on correctness, not efficiency for this question. Your inputs are the four address lines. Implementing the read functionality is sufficient.
10. (15 pts.) Determine the period of oscillation for a ring of three balanced inverters with minimal-width NMOSFETs. Explicitly state any simplifying assumptions you make. The diffusion region lengths are all 0.5 µm, but don’t assume that my stating this requires that you use it.

Question 10 was the last question. You are done. Have a good break.
## Reference material

<table>
<thead>
<tr>
<th></th>
<th>$C_{OX}$</th>
<th>$C_D$</th>
<th>$C_j$</th>
<th>$m_j$</th>
<th>$\phi_b$</th>
<th>$C_{jsw}$</th>
<th>$m_{jsw}$</th>
<th>$\phi_{bsw}$</th>
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<tbody>
<tr>
<td>NMOS</td>
<td>6</td>
<td>0.31</td>
<td>2</td>
<td>0.5</td>
<td>0.9</td>
<td>0.28</td>
<td>0.44</td>
<td>0.9</td>
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<tr>
<td>PMOS</td>
<td>6</td>
<td>0.27</td>
<td>1.9</td>
<td>0.48</td>
<td>0.9</td>
<td>0.22</td>
<td>0.32</td>
<td>0.9</td>
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### MODELS FOR CMOS DEVICES

#### CMOS (0.25 µm) – Unified Model

<table>
<thead>
<tr>
<th></th>
<th>$V_{TH}$ (V)</th>
<th>$\gamma$ (V^2 A^2)</th>
<th>$V_{DSAT}$ (V)</th>
<th>$k'$ (A/V^2)</th>
<th>$\lambda$ (V^-1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>0.43</td>
<td>0.4</td>
<td>0.63</td>
<td>115 x 10^-6</td>
<td>0.06</td>
</tr>
<tr>
<td>PMOS</td>
<td>-0.4</td>
<td>-0.4</td>
<td>-1</td>
<td>-30 x 10^-6</td>
<td>-0.1</td>
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#### CMOS (0.25 µm) – Switch Model ($R_{eq}$)

<table>
<thead>
<tr>
<th>$V_{DD}$ (V)</th>
<th>1</th>
<th>1.5</th>
<th>2</th>
<th>2.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS (kΩ)</td>
<td>35</td>
<td>19</td>
<td>15</td>
<td>13</td>
</tr>
<tr>
<td>PMOS (kΩ)</td>
<td>115</td>
<td>55</td>
<td>38</td>
<td>31</td>
</tr>
</tbody>
</table>

#### CMOS (0.25 µm) – BSIM Model

See Website: [http://bwr.eecs.berkeley.edu/lcBook](http://bwr.eecs.berkeley.edu/lcBook)

<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$kT/q$</td>
<td>25.875 mJ/C</td>
</tr>
<tr>
<td>NMOSFET $I_S$</td>
<td>21.0 pA</td>
</tr>
<tr>
<td>PMOSFET $I_S$</td>
<td>41.8 pA</td>
</tr>
<tr>
<td>$n$ (for $I_D$ calculation)</td>
<td>1.5</td>
</tr>
</tbody>
</table>

\[
V_M = \left( V_{Th} + \frac{V_{DSATn}}{2} \right) + r \left( V_{DD} + V_{Th} + \frac{V_{DSATp}}{2} \right) \frac{1 + r}{k_P V_{DSATp}} = \frac{\nu_{satp} W_p}{\nu_{satn} W_n}
\]
VALUES OF MATERIAL AND PHYSICAL CONSTANTS

<table>
<thead>
<tr>
<th>Name</th>
<th>Symbol</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Room temperature</td>
<td>(\gamma)</td>
<td>300 ((\approx) 27°C)</td>
<td>K</td>
</tr>
<tr>
<td>Boltzmann constant</td>
<td>(k)</td>
<td>(1.38 \times 10^{-23})</td>
<td>J/K</td>
</tr>
<tr>
<td>Electron charge</td>
<td>(q)</td>
<td>(1.6 \times 10^{-19})</td>
<td>C</td>
</tr>
<tr>
<td>Thermal voltage</td>
<td>(\phi_T = kTq)</td>
<td>26</td>
<td>mV (at 300 K)</td>
</tr>
<tr>
<td>Intrinsic Carrier Concentration (Silicon)</td>
<td>(n_i)</td>
<td>1.5 \times 10^{10}</td>
<td>cm(^{-3}) (at 300 K)</td>
</tr>
<tr>
<td>Permittivity of Si</td>
<td>(\varepsilon_s)</td>
<td>(1.05 \times 10^{-12})</td>
<td>F/cm</td>
</tr>
<tr>
<td>Permittivity of SiO(_2)</td>
<td>(\varepsilon_m)</td>
<td>(3.5 \times 10^{-13})</td>
<td>F/cm</td>
</tr>
<tr>
<td>Resistivity of Al</td>
<td>(\rho_{Al})</td>
<td>(2.7 \times 10^{-8})</td>
<td>(\Omega)-m</td>
</tr>
<tr>
<td>Resistivity of Cu</td>
<td>(\rho_{Cu})</td>
<td>(1.7 \times 10^{-8})</td>
<td>(\Omega)-m</td>
</tr>
<tr>
<td>Magnetic permeability of vacuum</td>
<td>(\mu_0)</td>
<td>(12.6 \times 10^{-7})</td>
<td>Wb/Am</td>
</tr>
<tr>
<td>Speed of light (in vacuum)</td>
<td>(c_0)</td>
<td>30</td>
<td>cm/nsec</td>
</tr>
<tr>
<td>Speed of light (in SiO(_2))</td>
<td>(c_{as})</td>
<td>15</td>
<td>cm/nsec</td>
</tr>
</tbody>
</table>

Definitions useful in gate sizing

\[ G = \prod_{i=1}^{n} g_i \]  
\[ H = \frac{C_{in}}{C_{useful}} \]  
\[ b = \frac{C_{total}}{C_{useful}} \]  
\[ B = \prod_{i=1}^{n} b_i \]  
\[ F = GBH \]  
\[ \hat{f} = g_i h_i = \sqrt{F} \]  
\[ \hat{h}_i = \frac{\hat{f}}{g_i} = \frac{C_{i, out}}{C_{i, in}} \]  
\[ D_i = G_i h_i + p_i \]  

For sizing inverters, \(\forall i \sum b = g = 1\).
FORMULAS AND EQUATIONS

Diode
\[ I_D = I_S(e^{\frac{V_d}{V_T}} - 1) = \frac{Q_D}{\tau_T} \]
\[ C_J = \frac{C_D}{(1 - V_D' / \Phi_D)^m} \]
\[ K_{eq} = \frac{-\Phi_D}{(V_{\text{high}} - V_{\text{low}})(1 - m)} \times \frac{[(\Phi_D - V_{\text{high}})^{1-m} - (\Phi_D - V_{\text{low}})^{1-m}]}{} \]

MOS Transistor
\[ V_T = V_{TH} + \gamma(\sqrt{-2\Psi_T} + V_{SB} - \sqrt{-2\Psi_T}) \]
\[ I_D = \frac{k\sqrt{W}}{2L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \] (sat)
\[ I_D = \frac{V_{GS} - V_T}{2} \] (velocity sat)
\[ I_D = I_s e^{\frac{V_{GS} - V_T}{V_T}} \] (subthreshold)

Deep Submicron MOS Unified Model
\[ I_D = \begin{cases} 0 & \text{for } V_{GT} \leq 0 \\ k' \frac{W}{L}(V_{GT} - V_{min} - \frac{V_{GS}^2}{2})(1 + \lambda V_{DS}) & \text{for } V_{GT} \geq 0 \end{cases} \]
with \( V_{min} = \min(V_{GT}, V_{DD}, V_{DSAT}) \)
and \( V_{GT} = V_{GS} - V_T \)

MOS Switch Model
\[ R_{eq} = \frac{1}{2I_{DSAT}(1 + \lambda V_{DD})} \left( I_{DSAT} + \frac{V_{DD}}{2} \right) \]
\[ = \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} \left( 1 - \frac{5}{6} \lambda V_{DD} \right) \]

Inverter
\[ V_{OH} = f(V_{OL}) \]
\[ V_{OL} = f(V_{OH}) \]
\[ V_{M} = f(V_{M}) \]
\[ t_p = 0.69 R_C C_L = \frac{C_L}{I_{avg}} \]
\[ P_{avg} = C_L V_{DD} V_{swing} f \]
\[ P_{stat} = V_{DD} P \]

Static CMOS Inverter
\[ V_{OH} = V_{DD} \]
\[ V_{OL} = GND \]
\[ V_{M} = \frac{V_{DD}}{1 + r} \]
\[ V_{IL} = V_{M} - \frac{V_{M}}{g} \]
\[ V_{IL} = V_{M} + \frac{V_{DD} - V_{M}}{g} \]
with \( g = \frac{1}{1 + r} \)
\[ t_p = \frac{f_{pL} + f_{pH}}{2} = 0.69 C_L \left( \frac{R_{eq} + R_{rep}}{2} \right) \]
\[ P_{av} = C_L V_{DD} f \]

Interconnect
Lumped RC: \( t_p = 0.69 RC \)
Distributed RC: \( t_p = 0.38 RC \)
RC-chain:
\[ \tau_N = \sum_{i=1}^{N} R_i C_j = \sum_{i=1}^{N} C_j \]
Transmission line reflection:
\[ p = \frac{V_{eff}}{V_{inc}} \]
\[ p = \frac{I_{eff}}{I_{inc}} \]

CMOS COMBINATIONAL LOGIC

Transistor Sizing using Logical Effort
\[ F = \frac{C_L}{C_G} = \prod_{i=1}^{N} \frac{f_{i}}{b_i} \]
\[ G = \prod_{i=1}^{N} g_i \]
\[ D = t_{p0} \sum_{j=1}^{N} \left( p_j + \frac{g_j}{\gamma} \right) \]
\[ B = \prod_{i=1}^{N} b_i \]
\[ H = FGB \]
\[ D_{min} = t_{p0} \left( \sum_{j=1}^{N} p_j + \frac{N(H)}{\gamma} \right) \]