Homework Four

EECS 303: Advanced Digital Logic Design
Assigned 11 November
Due date to be announced (no earlier than 18 November)

You may discuss the assignment with your classmates. However, you need to write down your solutions independently. Please make sure your answers are legible. You can manually produce the circuit diagrams or use a graphics package with a logic gate library, e.g., `xfig`.

1. **(10 pts)** Covering
   - Name a logic design problem that can be solved by unate covering.
   - Name a logic design problems that can be solved by binate covering.
   - Given the following POS expression

$$F(A,B,C,D) = (A+B+C)(A+C+\overline{D}\,)(B+D)(\overline{A}\,+\overline{B}\,+\overline{C}\,+\overline{D}\,)$$

     (a) Write the unate or binate covering table to solve the problem of finding a satisfying assignment of variables for this function.
     (b) Find a satisfying assignment to variables such that a minimal number of variables is true. Check your assignment by plugging into the original expression or by using a Karnaugh map.

2. **(15 pts)** Implement the following Boolean functions in a hazard-free manner in the original SOP or POS format. In other words, add exactly those cubes required to prevent hazards.
   (a) $F(A,B,C) = B\ \overline{C}\ + \overline{A}\ C$
   (b) $F(A,B,C,D) = \sum(0,4,5,6,7,9,11,13,14)$
   (c) $F(A,B,C) = (A+B)(\overline{B}\ + A)$
   (d) $F(A,B,C,D) = \prod(0,1,3,5,7,8,9,13,15)$

3. Design a 4-bit binary increment by one counter using only rising edge-triggered and/or falling edge-triggered T flip-flops. The T flip-flops have asynchronous resets.
   (a) **(10 pts)** Give the circuit diagram for the counter.
   (b) **(10 pts)** Give the timing diagram for the circuit counting from 0010 through 0101. Show all T flip-flop outputs.
   (c) **(10 pts)** Show the circuit diagram for a rising or falling edge-triggered T flip-flop using only a D flip-flop and two-input NAND gates. Show your intermediate steps.

4. **(20 pts)** Minimize the following incompletely specified Moore FSM. Formulate as a binate covering problem, if necessary.

Current State	Next State (i)		Output
	0	1	
A	B	E	0
B	D	B	1
C	C	X	X
D	F	F	X
E	E	X	0
F	X	A	1

5. Please design a machine, M, that will produce an output of one for all the following input sequences and an output of zero for any other input sequences.

   (a) Any sequence beginning with 10

   (b) Any sequence ending with 11

   (c) The sequence 110

   Please do your design in the following steps:

   (a) **(5 pts)** Write a regular expression for this specification.

   (b) **(5 pts)** Draw the NFA state diagram for M.

   (c) **(15 pts)** Derive a DFA state diagram for M.

   (d) **(5 pts)** Derive a Moore FSA for M.

   (e) **(5 pts)** Write the state transition table for M's FSA.

   (f) **(15 pts)** Use an implication chart to minimize the number of states.

   (g) **(5 pts)** Draw the minimized state diagram. How many states are required to implement the machine? How many state variables are required to implement the machine?

   (h) **(10 pts)** Do heuristic state assignment.

   (i) **(5 pts)** Explain, in five or fewer sentences, the approach you would use to derive the state equations and full gate-level schematic. **Estimate** (you don't need to do it) how long it would take you to actually do this.