ECE 303: Advanced Digital Logic Design
Midterm Exam

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1. **(10 pts.)** Karnaugh maps

   (a) Why does the use of Karnaugh maps not guarantee arrival at an optimal (minimal literal count) solution to the two-level combinational logic minimization problem?

   (b) Use Karnaugh maps to derive minimal SOP expressions for a 3:2 priority encoder.

2. **(15 pts.)** Quine-McCluskey

   (a) Why does the use of the Quine-McCluskey method not guarantee arrival at an optimal (minimal literal count) solution to the combinational logic minimization problem?

   (b) Find a minimal two-level implementation of the following function, using the Quine-McCluskey method and other transformations of your choice. Use only NAND and NOR gates in your implementation.

   $$f(a,b,c) = \sum(0,1,2,3,5) + d(4) \tag{1}$$

   (c) What is the proper name for the second phase of the Quine-McCluskey algorithm?

3. **(25 pts.)** Espresso

   (a) What is the main difference between Espresso and MIS when used for combinational logic minimization?

   (b) Consider the following cover

Cube				Set
×	×	0	1	1
1	1	×	1	1
1	×	1	1	1
×	0	1	×	×

   Mimic the method used by Espresso to find the relatively essential, totally redundant, and partially redundant cubes in the cover. Then formulate the selection of partially redundant cubes as a unate covering problem instance and solve the instance, writing a SOP expression for the cover. To save you time, I will list the ones here: 1, 5, 9, 13, 15.

4. **(20 pts.)** Composition

   (a) What is the minimal number of transistors required to built a 4:1 multiplexer using a CMOS logic gate or transmission gate based design style? You need show only one design but it must use the style allowing the minimal number of transistors. Do not neglect the cost of inverters.

   (b) What is the minimal number transistors required to built an 2^n:1 multiplexer, if you do not count transistors used for signal restoration? You may find the following fact useful:

$$\sum_{i=1}^{n} 2^i = 2^{n+1} - 2 \tag{2}$$

5. **(20 pts.)** If it is necessary to restore a signal after it passes through three transistors, show a minimal CMOS logic gate based implementation of the following function. Although you need not draw transistors, you must understand how they are used to construct logic gates to answer this question correctly. You may find algebraic manipulation useful. Incorrect implementations will be judged more harshly than correct but non-minimal implementations. You may assume access to complemented and uncomplemented inputs.

$$f(a,b,c,d) = \sum(2,3,6,7,9,12) \tag{3}$$