

$$f = \bar{a}\bar{b}\bar{c}\bar{d} + \bar{a}b\bar{c}\bar{d} + a\bar{b}\bar{c} + b\bar{c}\bar{d} + a\bar{b}c + \bar{b}cd$$

cube	kernel?	benefit
$\bar{a}$	<del><math>\bar{b}\bar{c}\bar{d} + b\bar{c}\bar{d}</math></del>	n.a.
$a$	$b\bar{c} + \bar{b}c$	1
$\bar{b}$	$a\bar{c}\bar{d} + cd + ac$	2
$b$	$a\bar{c} + \bar{c}\bar{d} + \bar{a}c\bar{d}$	2
$\bar{c}$	$\bar{a}\bar{b}\bar{d} + b\bar{d} + ab$	2
$c$	$\bar{b}\bar{d} + a\bar{b} + \bar{a}b\bar{d}$	2
$\bar{d}$	<del><math>\bar{a}\bar{b}\bar{d} + \bar{a}b\bar{c}</math></del>	n.a.
$d$	$b\bar{c} + \bar{b}c$	1
$\bar{b}c$	$\begin{matrix} d+a \\ a+d \end{matrix}$ same	<del>2</del> Actual benefit = 6
$b\bar{c}$	$\bar{b}\bar{c} + bc$	2
$\bar{a}\bar{d}$	$\bar{b}\bar{c} + bc$	2

$$f = \bar{a}\bar{b}\bar{c}\bar{d} + \bar{a}b\bar{c}\bar{d} + (a+d)(\bar{b}\bar{c} + bc)$$

cube	kernel?	benefit
$\bar{a}$	<del><math>\bar{b}\bar{c}\bar{d} + b\bar{c}\bar{d}</math></del>	n.a.
$\bar{d}$	<del><math>\bar{a}\bar{b}\bar{c} + abc</math></del>	n.a.
$\bar{a}\bar{d}$	$\bar{b}\bar{c} + bc$	2

$$f = \bar{a}\bar{d}(\bar{b}\bar{c} + bc) + (a+d)(\bar{b}\bar{c} + bc)$$

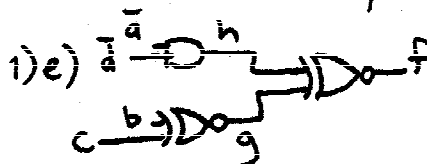
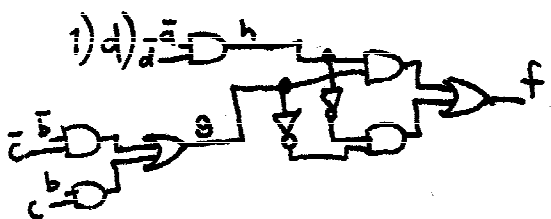
1) b)  $g = \bar{b}\bar{c} + bc$  (4 lit.)  
 $h = \bar{a}\bar{d}$  (2 lit.)

Thus,  $\bar{g} = b\bar{c} + \bar{b}c$  and  $\bar{h} = \overline{\bar{a}\bar{d}} = a+d$

So  $f = hg + \bar{h}\bar{g}$  (4 lit.)

1) c) 12 literals for kernel extraction

10 literals for kernel extraction and decomposition

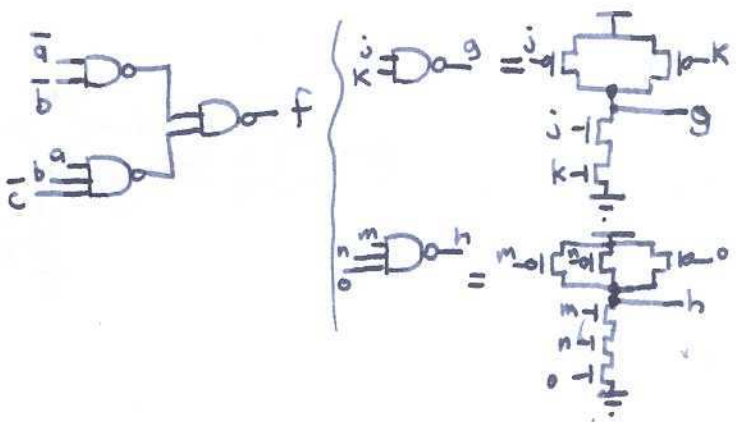


- 2)a) power down linear  
 performance down linear  
 energy constant (if switching power dominates leakage)
- 2)b) power down quadratic ( $P = IV = V^2/R$ )  
 performance down linear (to compensate)  
 energy down linear
- 2)c) switching power consumption results from current when gate outputs change. Leakage power is constant and results from some current flow through channels of off MOSFETs. It gets worse as  $V_{DD} \rightarrow V_{TH}$
- 2)d) 

	b	c
a	0	1
	x	1

$$f = \bar{a}\bar{b} + abc$$

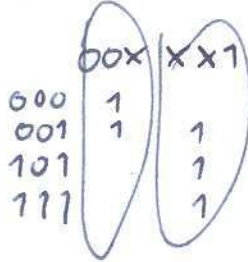
$$f = \frac{\bar{a}\bar{b} + abc}{\bar{a}\bar{b} + abc}$$

$$f = \frac{\bar{a}\bar{b} \cdot abc}{\bar{a}\bar{b} \cdot abc}$$

- 3)a) Given a table with entries of 1 and 0, select a subset of columns s.t. each row contains at least one 1 in a selected column and the cardinality or cost of the columns is minimized.
- 3)b) A set of problems for which nobody has found optimal polynomial time ~~solutions~~ algorithms. Any instance of an NP-complete problem may be converted to an instance of another NP-complete problem in polynomial time. Solutions can be verified in polynomial time.
- 3)c) The second stage of 2M can be solved in polynomial time, i.e., two-level logic minimization can be done optimally in polynomial time.
- 3)d) All can be solved in polynomial time by conversion of instances.

4)a)

000	000v	00X
001	001v	
101		X01v
111	101v	0X1v
X011	011v	1X1v
	111v	X11v

XX1



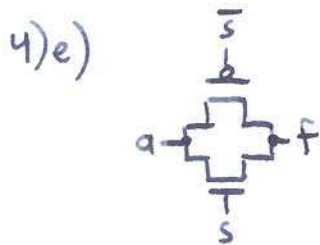
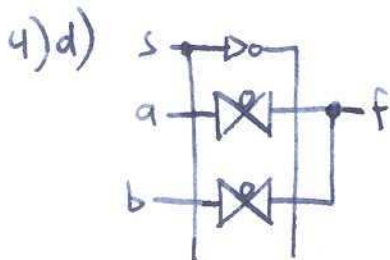
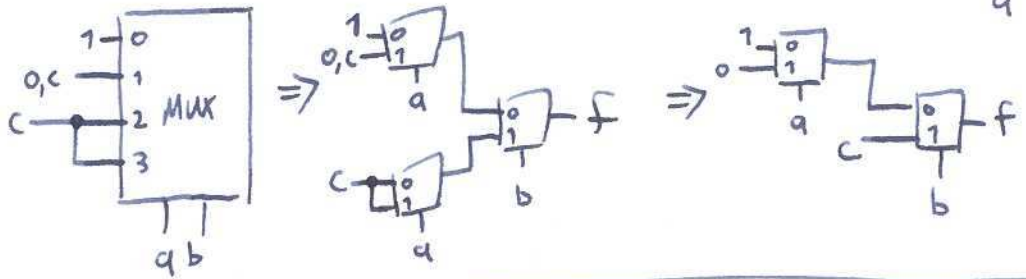
$f = \bar{a}\bar{b} + c$

4)b) Yes. All primes essential. Two-level minimization is hard becauseunate covering can require backtracking

4)c)

a	b	c	f
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	X
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Better possible: 



5)a) PAL/PLA: Simple, two-level prog. logic.

ROM/PROM/EPROM: Non-volatile data storage.

Flash memory: Writable non-volatile storage.

FPGAs: Powerful general reconfigurable logic. Volatile. Expensive in volume.

Full Custom: Fast, low-power. Cheap in volume but requires difficult design and expensive mask/process.

5)b) ROM: Read-only memory. Cannot be programmed.

PROM: May be programmed once.

EPROM: May be erased and reprogrammed.

Erasing requires exposure to UV light.

EEPROM: May be electrically erased.

Flash memory: May have devices erased in blocks to increase speed.