Variability and DFM

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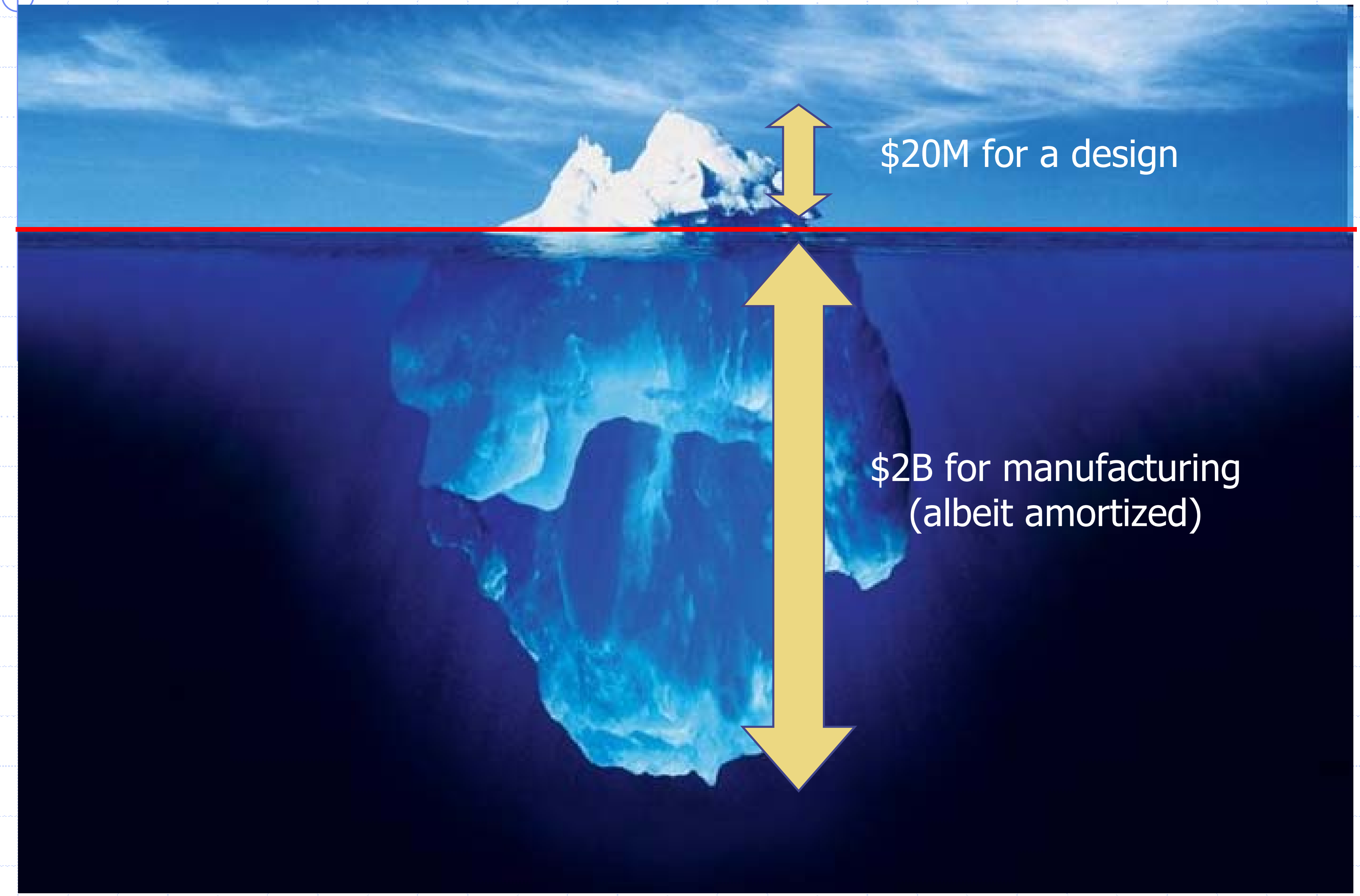
Motivation

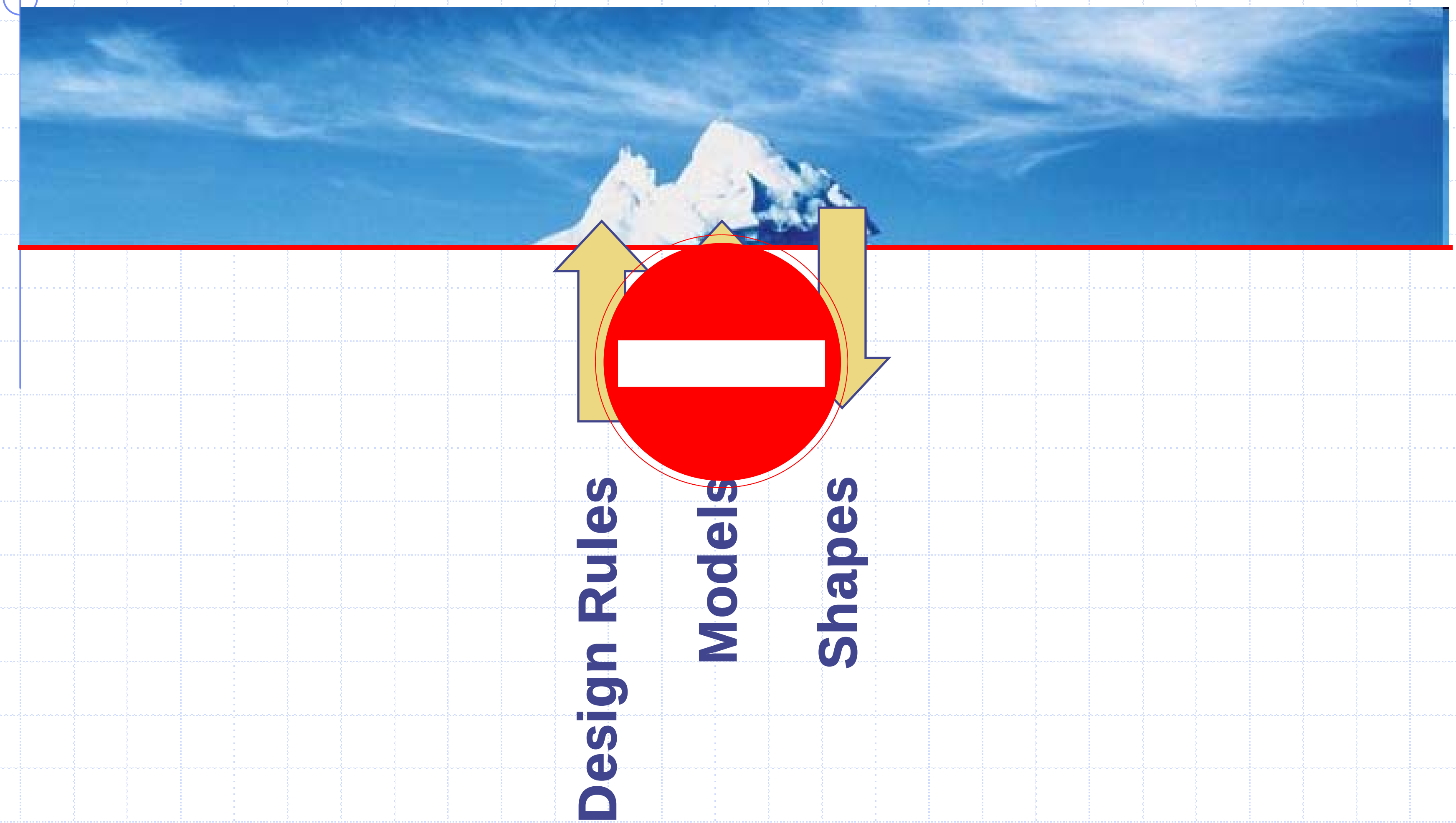
- Variability is a constant presence in the IC manufacturing process.
- The presence of variability impacts the quality of IC's.
- Quality is most easily relatable to profitability, which is in turn related to yield.

- The study of the relationship between variability and yield, and how to enhance design/fine tune process so that a higher yield can be achieved is called "Design for Manufacturing" or DFM.

Investment on an IC Product



Mead/Conway Principle



Outline

- Introduction to Variability
- A Taxonomy of Variability
- Random and Systematic Variability
- Variability Characterization
- Impact on Circuit Operation
- Variability Analysis
- Yield Optimization/Improvement
- DFM Trends and Outlook

- Homework Assignment

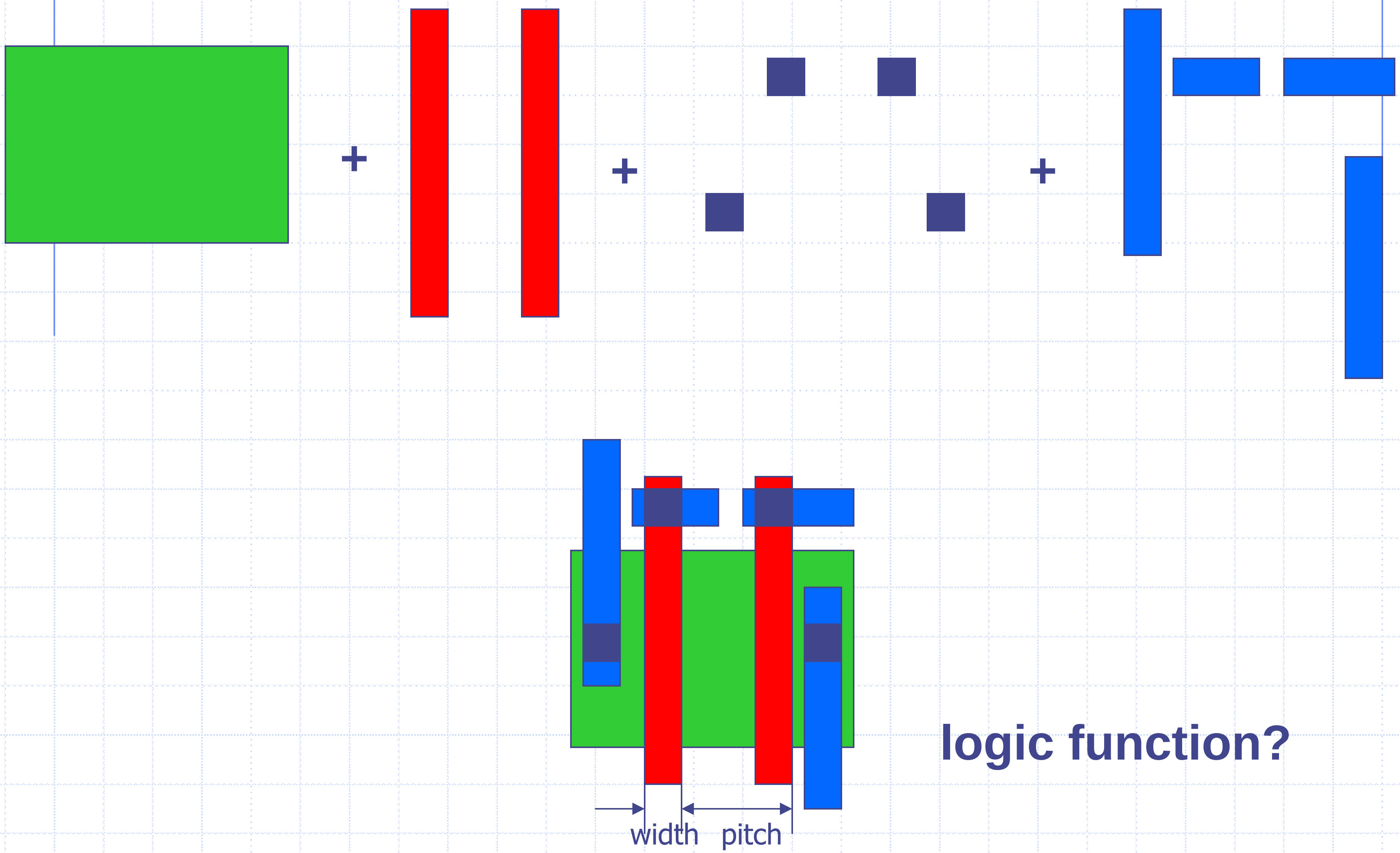
Introduction to Variability

- Variability comes about not only because of lack of uniformity, but also because of lack of knowledge about the non-uniformity
- Every device on every chip is NOT identical!
- These fluctuations result in different performance for each chip…
- Fluctuations imply unpredictability, and can also imply unprofitability.

Example: Litho-induced Variability

- Lithography is the key step in the patterning
- Has been the driving force behind the continuous scaling for past three decades

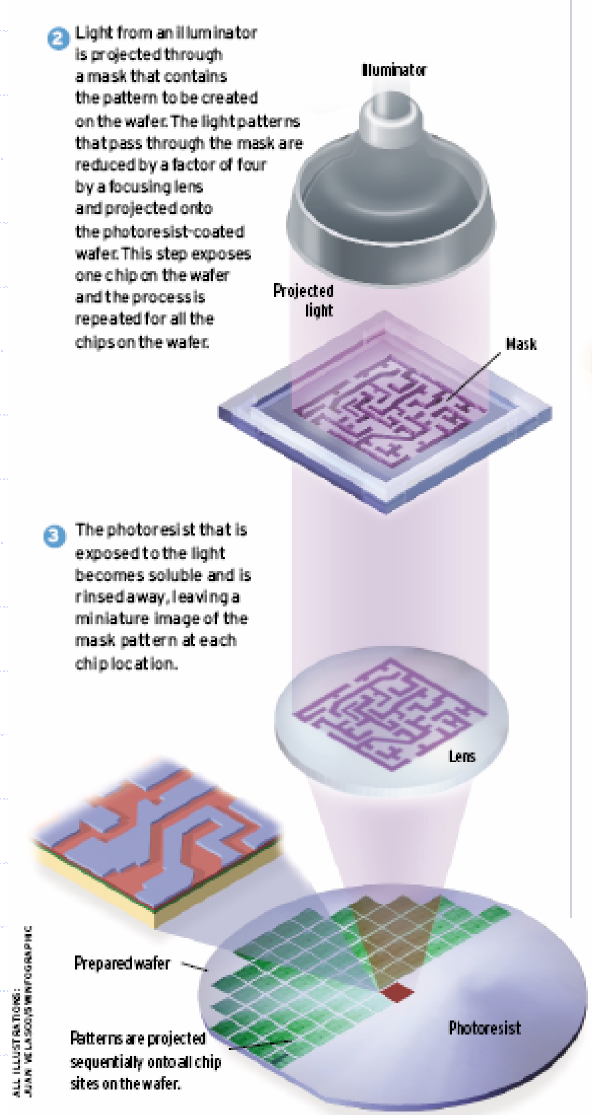
Patterning: Key Step in Manufacturing



logic function?

Microlithography: Physics + Chemistry

- Photolithography is as much as a chemistry process as a physics process
- Optical component
  - Project the desired pattern to the wafer surface with as small distortion as possible
  - High intensity and high contrast on the wafer surface
- Chemical component
  - Reacts to the patterning light intensity with small distortion
  - Reacts to the patterning light as fast as possible



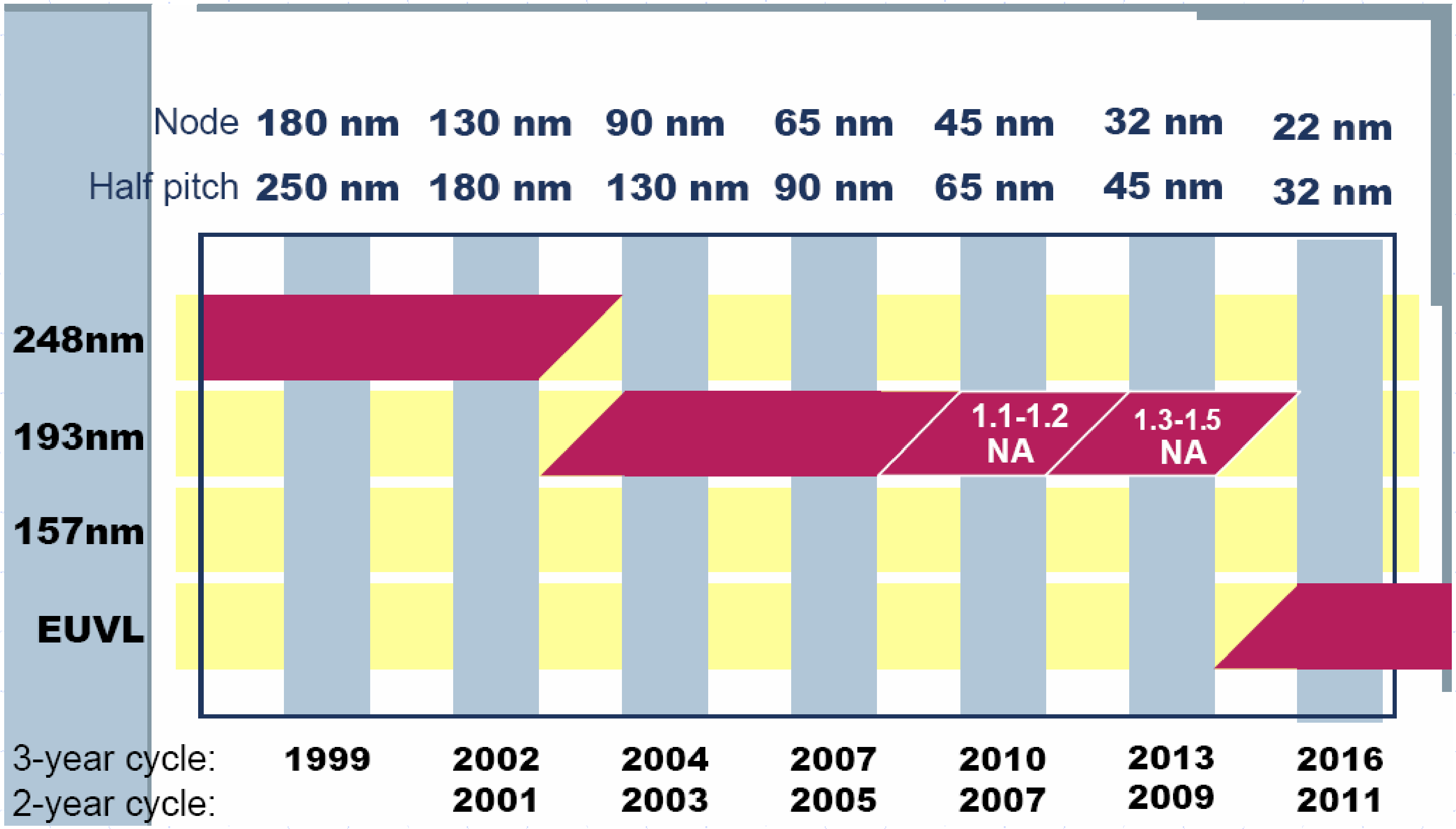
source: IEEE Spectrum

A Cool $50M Toy for Hardcore Geeks…

- High precision machine
- Capable of processing over 100 wafers/hour

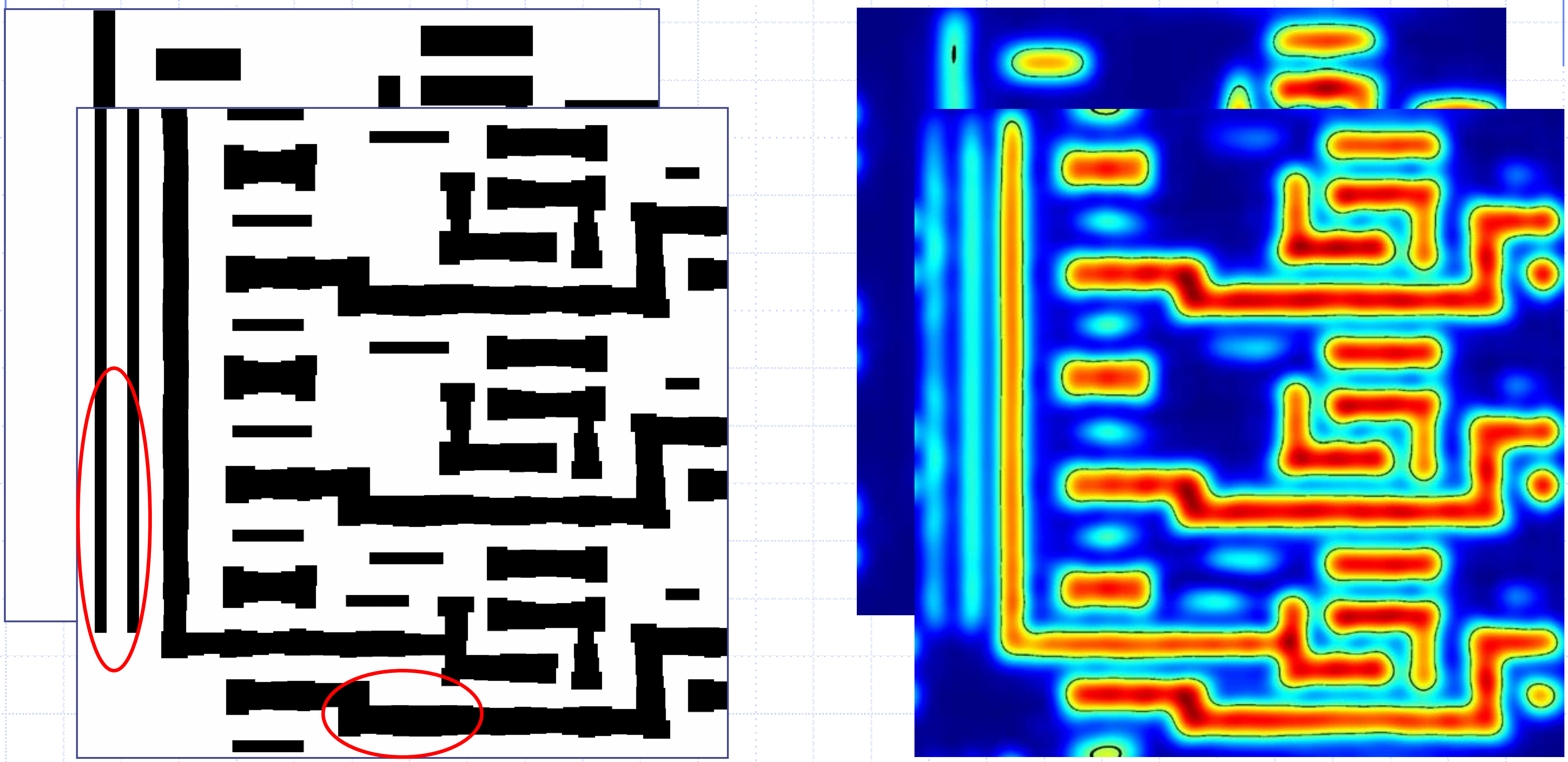
Eye-candy: Zeiss Starlith® 1700i Lens

ITRS Lithography Roadmap



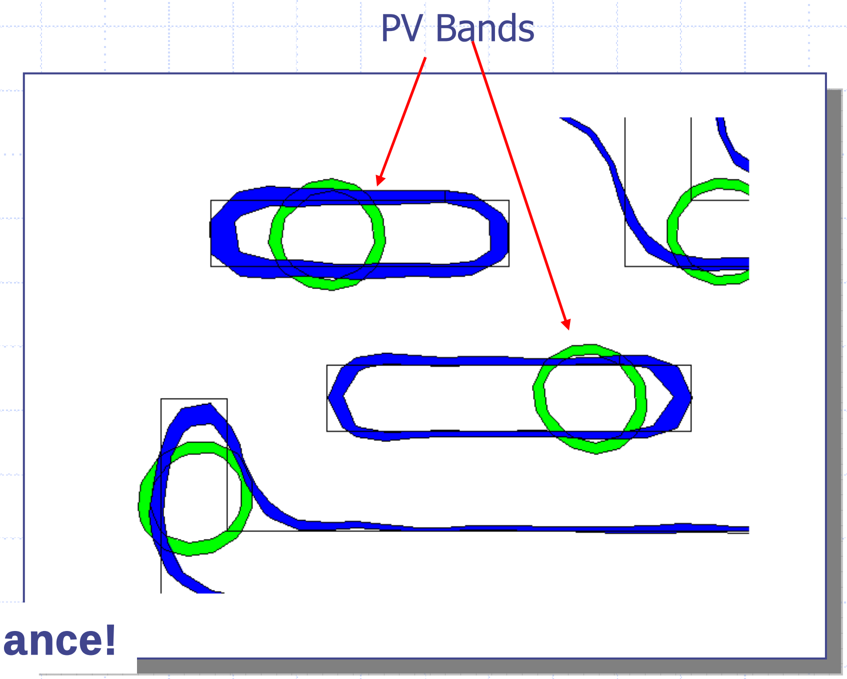
Sub-wavelength Lithography is Lossy

- What you see is NOT what you get!



Lithography Related Variability

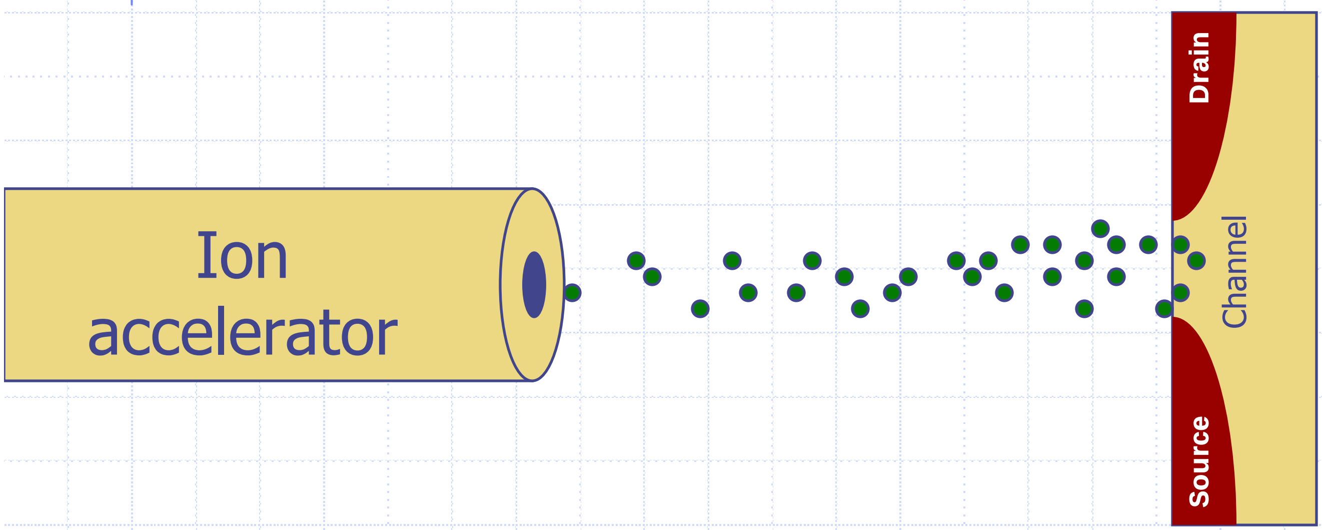
- Mask related variability (a few nm)
  - E-beam exposure noise
  - Loading effects
  - Mask defects
- OPC related variability (a few nm, up to 10nm)
  - OPC error
  - Model accuracy
- Wafer level variability (a few nm)
  - Wafer leveling
  - Lens aberration
  - Dose uniformity
- Photo-resist variability (a few nm)
  - Line edge roughness
- Etch related variability (a few nm)
  - Etch loading effects
- Design related variability



Implication on both FEOL and BEOL performance!

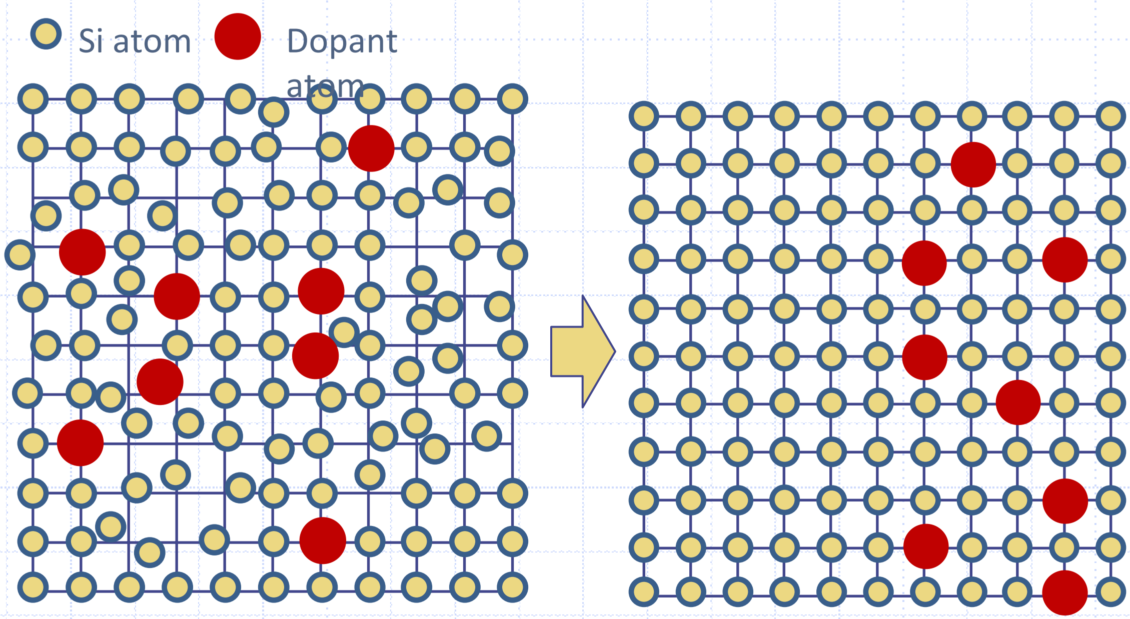
Another Example: Dopant Activation

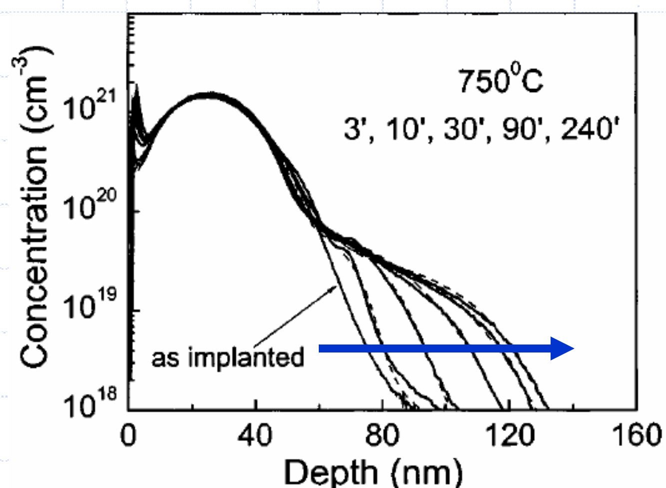
- In the process of creating a MOSFET, the threshold voltage is controlled by "implanting" dopant atoms in the channel.



Doping Activation

- After doping, annealing process is applied to activate dopant atoms
- Faster annealing is required to achieve high level of activation without cause unwanted diffusion
  - Effectiveness of annealing is measured by the peak temperature (activation temperature). Prolonged annealing can cause excessive diffusion of dopants)

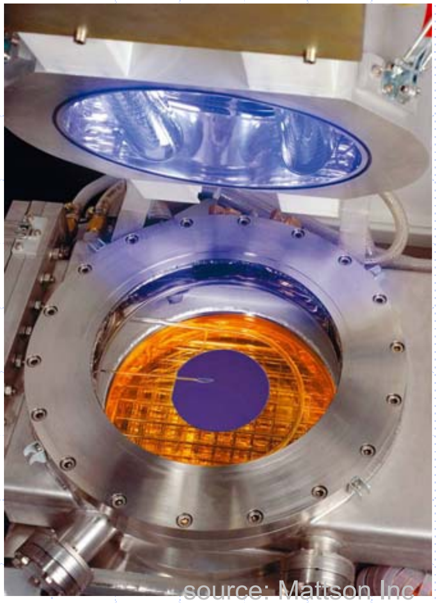


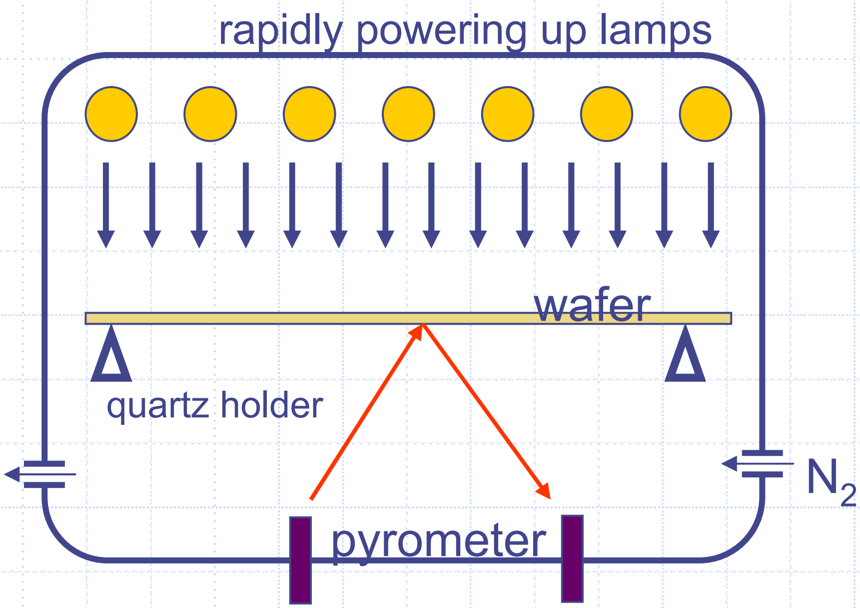


source: Y. Kim

Mechanism for Fast Heat Transfer

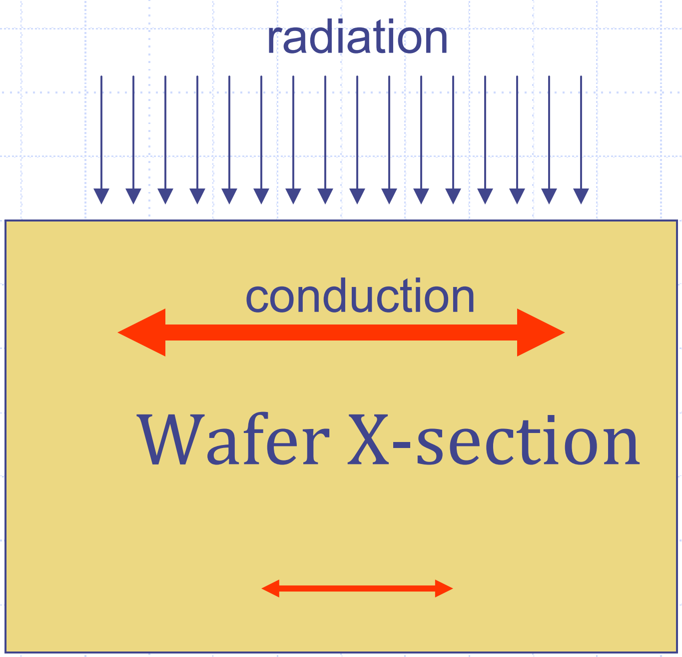
- Three basic mechanisms for heat transfering:
  - Conduction, convection and radiation
- To achieve ultra-shallow junctions, rapid thermal annealing is required, e.g., spike annealing

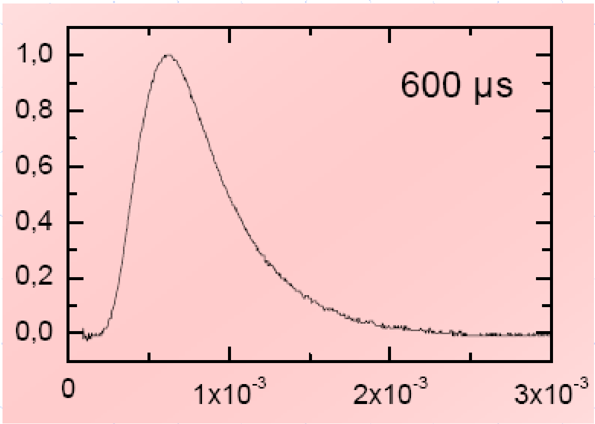




Rapid Thermal Transferring

- The activation temperature is determined by the balance between radiation and conduction
- Rapid thermal annealing means there is little time for conduction to achieve equilibrium

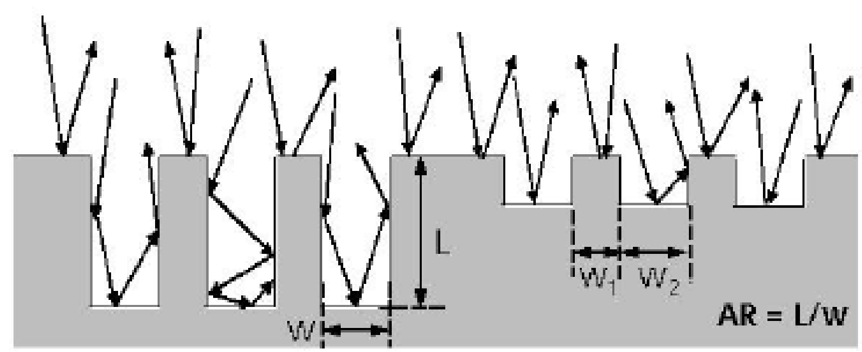




Reflectivity Differences

- The amount of energy a surface can absorb during the annealing process is related to the surface reflectivity
  - Empirically observed reflectivity differences
  - Thorough study requires solving of Maxwell equations near the surface
  - In one theory it is attributed to the “trapping” of photons in the STI trenches

Region	Reflection Coefficient
N+ source/drain	0.57
P+ source/drain	0.57
Gate over isolation	0.54
Gate over Transisto	0.45
Trench Isolation	0.20

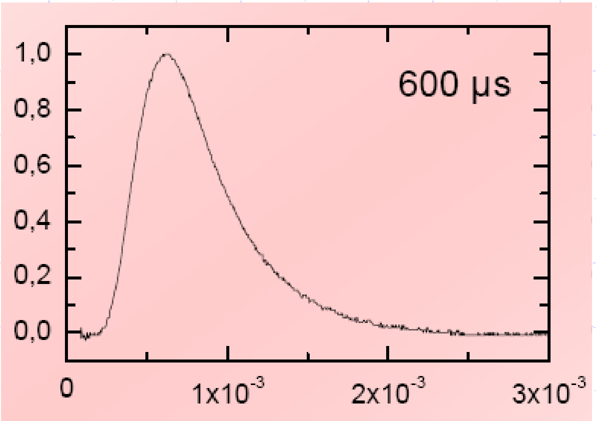


Large Aspect ratio AR Small Aspect ratio AR

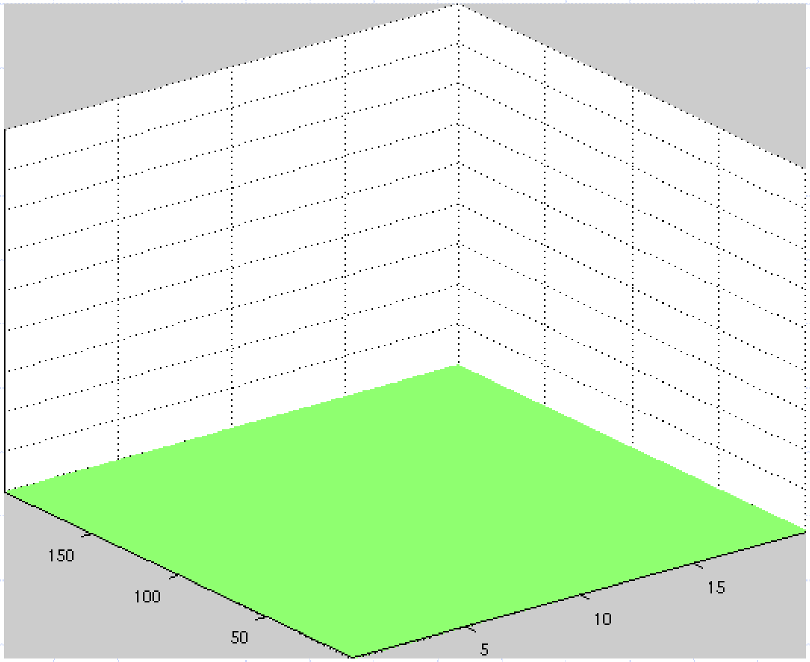
source: E. Granneman

Temperature Differences

- Regions with different reflectivity can have different activation temperature
- Difference in activation temperature causes difference in FET performance.

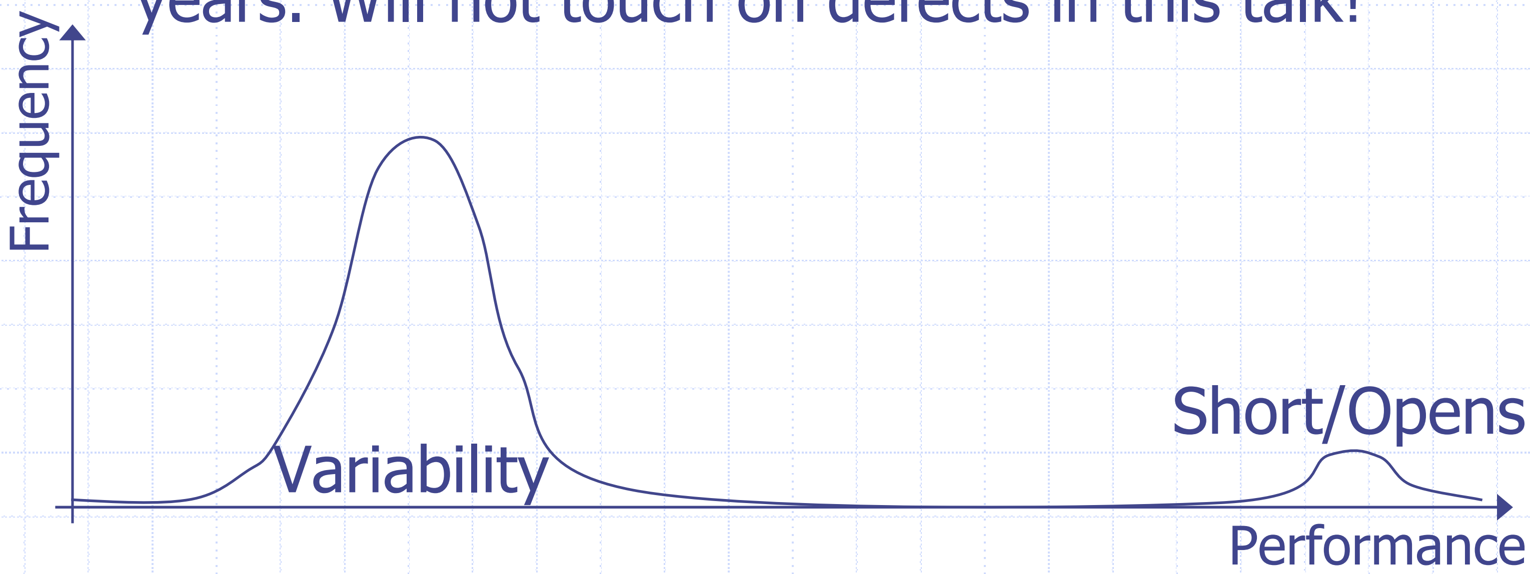


Annealing power profile



Variability vs. Defects

- Variability is one component of design-related yield, the other one is DEFECTS.
  - Defects change TOPOLOGY, Variability changes performance.
  - Has been the topic of active research in the past 30 years. Will not touch on defects in this talk!



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Variability Distribution

- Since the IC fabrication process is based on several hierarchical batch operations, variability in each operation tends to exhibit itself in a different way.

- In the RTA example, we might expect regions with higher densities of exposed STI area to differ from the regions with lower density
  - But how do we build effective models so that those effects can be incorporated into design flow in a meaningful way
  - How about other phenomena?

IC Manufacturing Hierarchy

- MOSFET
- Gate (includes many MOSFETs)
- Macro (many gates)
- Unit (includes many macros)
- Chip (IC, includes many units)
- Wafer (includes many chips)
- Lot (includes many wafers)
- Machine/Mask Set (used for specific lot/wafer)
- Facility (used for many lots)

IC Manufacturing Hierarchy

- MOSFET
- Gate (incl
- Macro (m
- Unit (inclu
- Chip (IC, includes many units)

Within Die
Designer has some control

- Wafer (includes many chips)
- Lot (inclu
- Machine/
- Facility (u

fic lot/wafer)

Die-to-Die
Designer has little control

Variability Sources

Physical

- Changes in characteristics of devices and wires.
- Caused by IC manufacturing process & wear-out.
- Time scale: 10^9sec (years).

Environmental

- Changes in V_{DD}, Temperature, local noise coupling.
- Caused by the specifics of the design implementation.
- Time scale: 10^{-6} to 10^{-9}sec (clock tick).

Variability Physical Distribution

Physical:

- Die to die variation
  - ***Imposed*** upon the design (constant regardless of design).
  - Modeled via worst-case files.
- Within-die variation
  - ***Co-generated*** between design and process (depends on details of the design).
  - Example: nested vs. isolated poly-silicon ΔL.

Environmental:

- Only makes sense within-die.

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Random vs. Systematic?

- Systematic variability occurs when a particular variation is caused by or related to known phenomena.
  - Example: chips on the edge of the wafer get more heat, therefore have thicker oxides…
- In such cases, the designer has the ability to control the magnitude and impact of the particular variability.
  - Therefore its impact can be compensated at design time.

Example of Systematic Variability

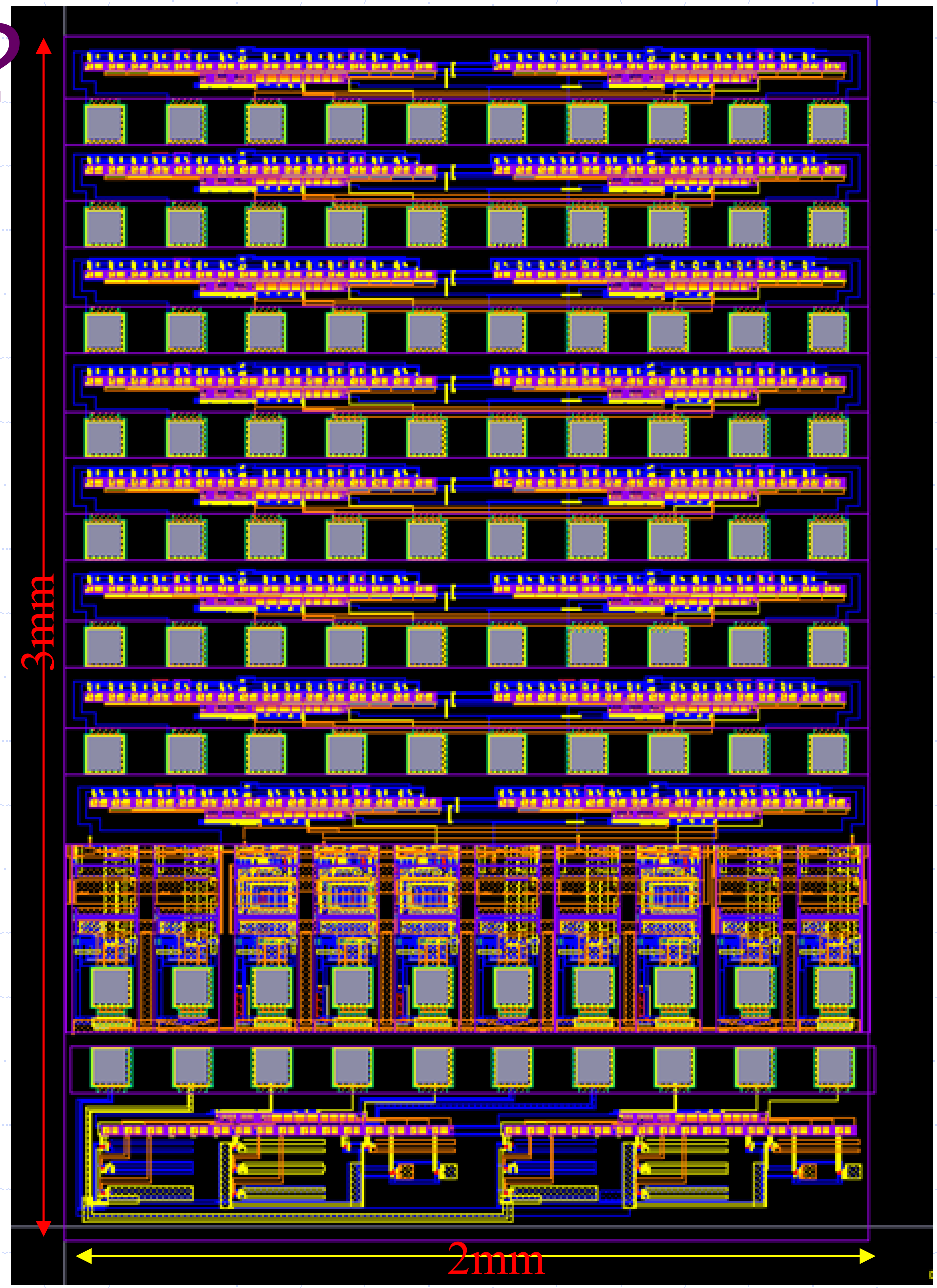
- In earlier technologies, the fabrication process caused differences between devices which we laid out horizontally or vertically.

- Such an offset, when understood, can be taken into account during design.

- Key, of course, is the “understood” part.

How Do We Know?

- Test chip designed to explore dependence on orientation.
- Fabricated in MOSIS 0.35μ process.
  - Ancient…
- Variety of Ring Oscillator structures.
  - Vertical/Horizontal etc…
  - Have the advantage of being easy to measure.



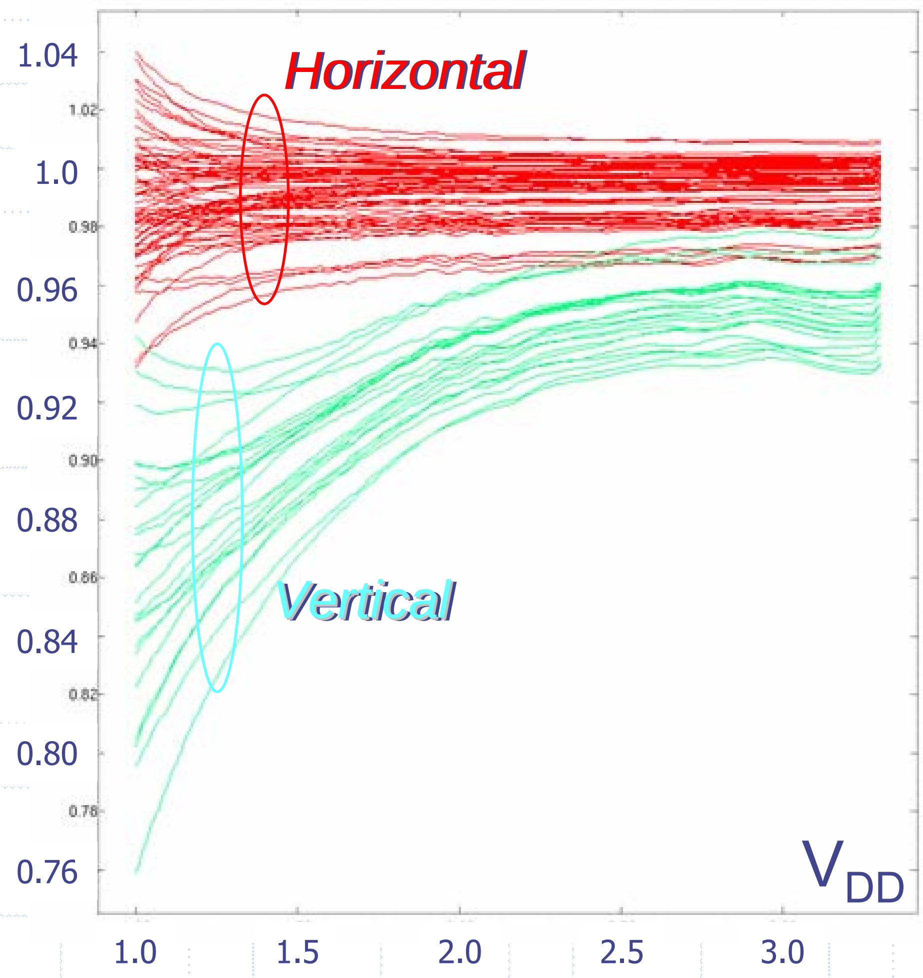
Result

- Die shot.
- Proof that at least one chip existed!
- Wouldn't want you to think I was not pulling a fast one on you!

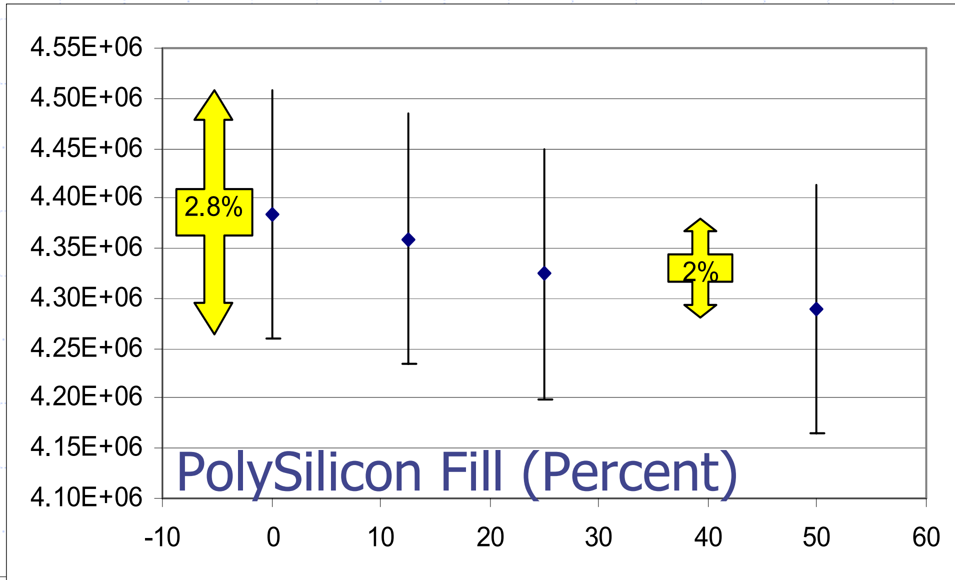
Observed Output

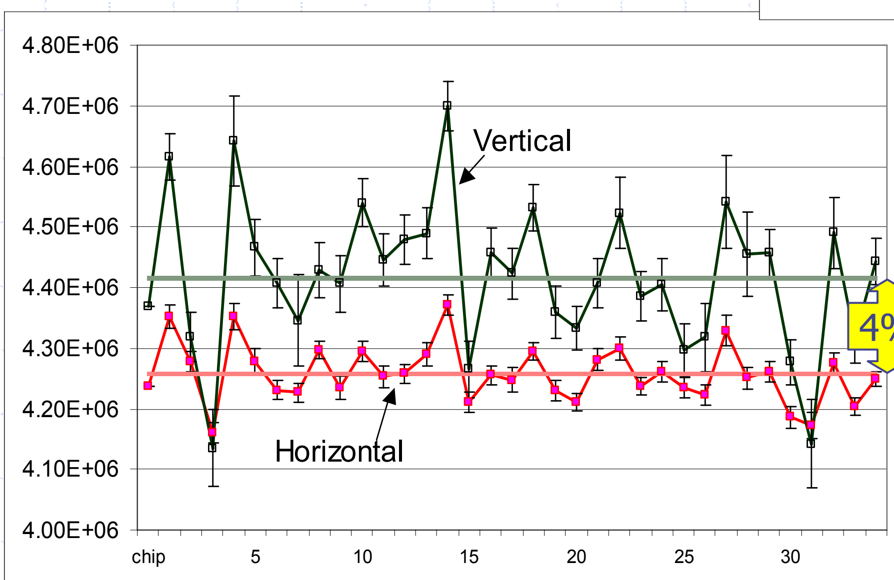
- Comparison of vertical vs. horizontal RO frequency.
  - 24 die tested.
- Clear delta between the two (identical) layouts.
- More difference at lower values of V_{DD}.
  - Implication: V_T.
  - File for future reference!

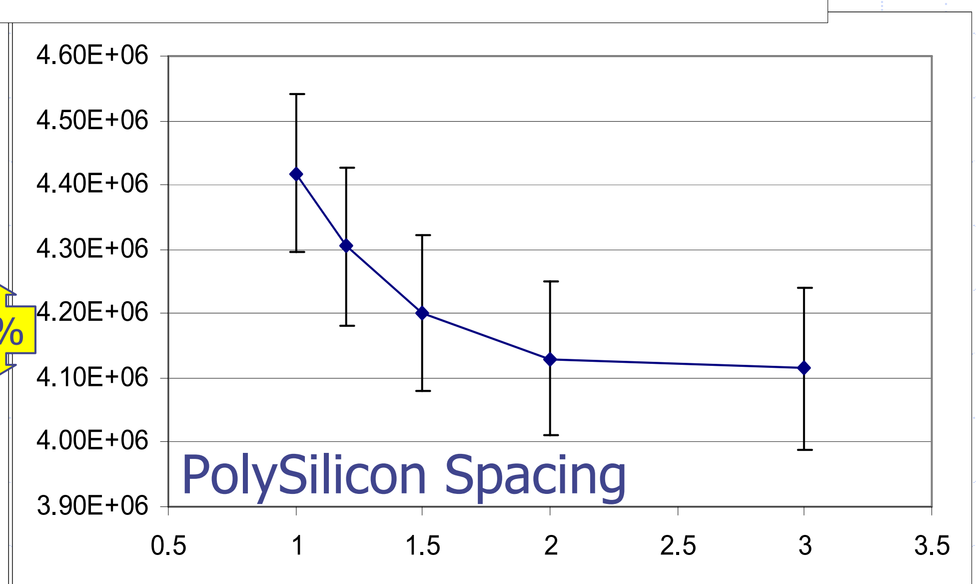
Ratio to 1st Horizontal



Other Systematic Effects







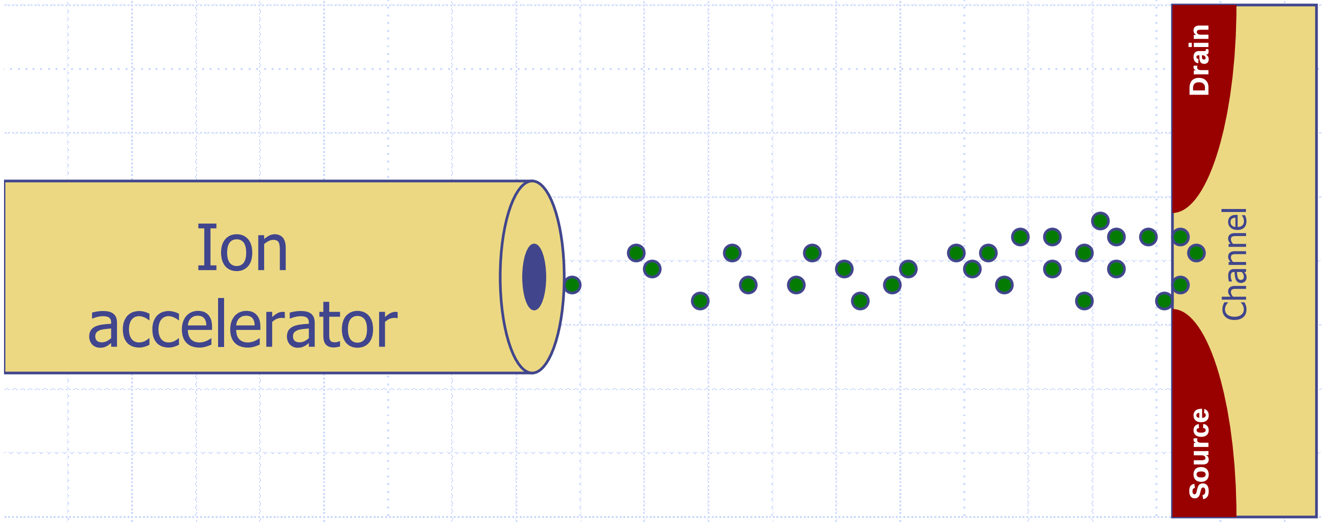
What about Random?

- It is tempting to think of everything as having a "cause" and therefore being systematic.
  - If we have a cause and an effect, and we can evaluate the relationship between them, then we can make a model.
  - A model may be Physics-based or just empirical.

- But… some phenomena are so complex that we are not able to create tractable models, therefore we must treat them as random.

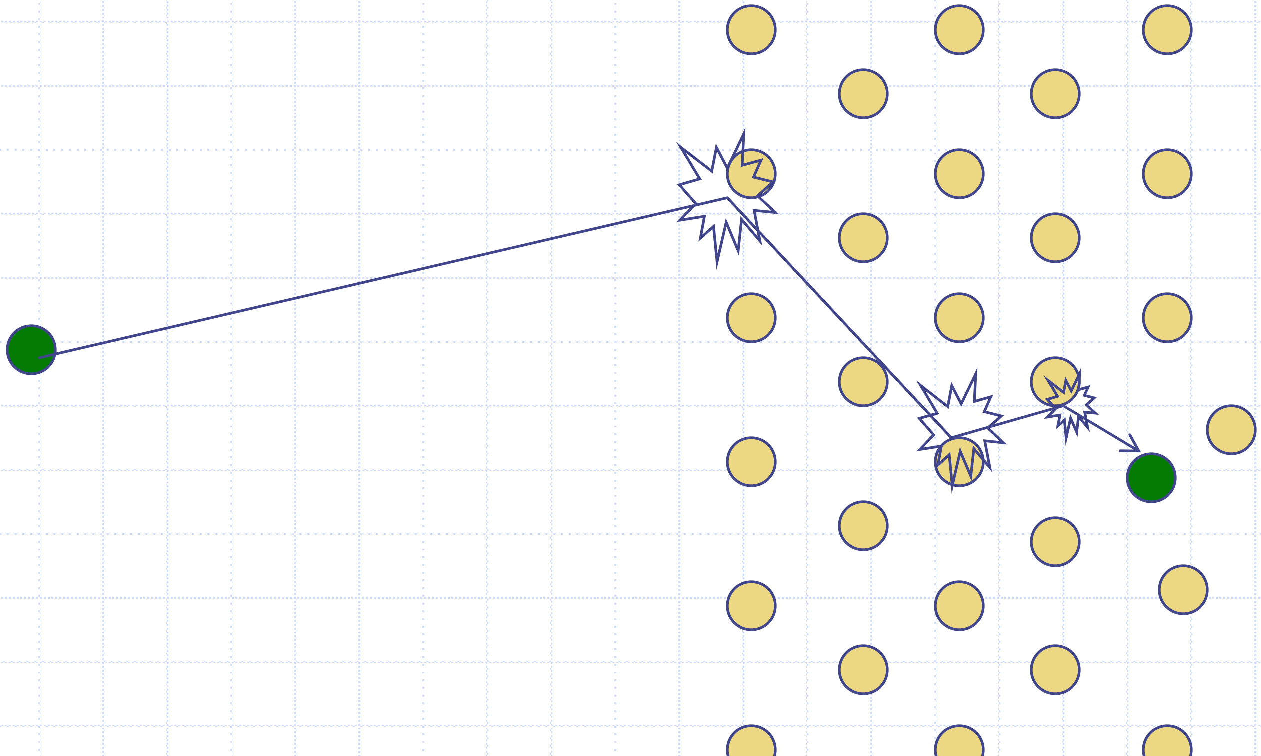
Implanting Example Again

- As we have seen, the threshold voltage is controlled by "implanting" dopant atoms in the channel.



Implantation at the Atomic Level

- Each implanted atom goes through a violent set of collisions before settling down into the Si crystal, displacing it locally.



Why is Implantation Random

- For any given particle, a small perturbation in the initial direction velocity can cause a large change in the eventual resting location.

- Such systems are deemed “chaotic”.
  - The study of dynamic systems is very interesting.

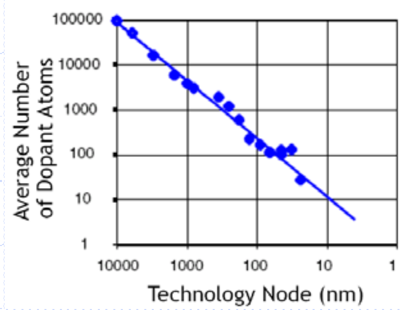
- The “butterfly effect” in weather is an example of such a phenomena.
  - A butterfly flapping it’s wings in <insert favorite place here> can cause a hurricane in Kansas.

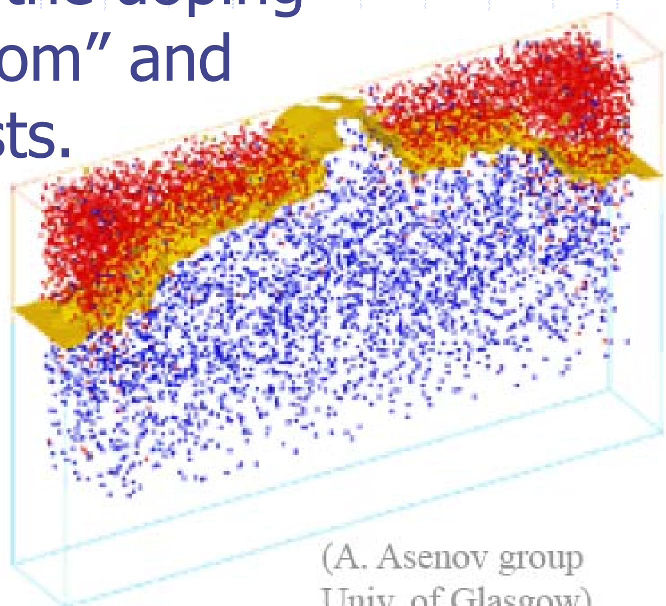
But why is implantation RANDOM

- In earlier technologies, the channel of a MOSFET was home to many many dopant atoms.
- While we cannot predict the location of every dopant atom individually, we can predict the statistical probability that an atom will reach a given depth.
- Given such a prediction, we can make estimates of the dopant atom density vs. depth.

What has Changed?

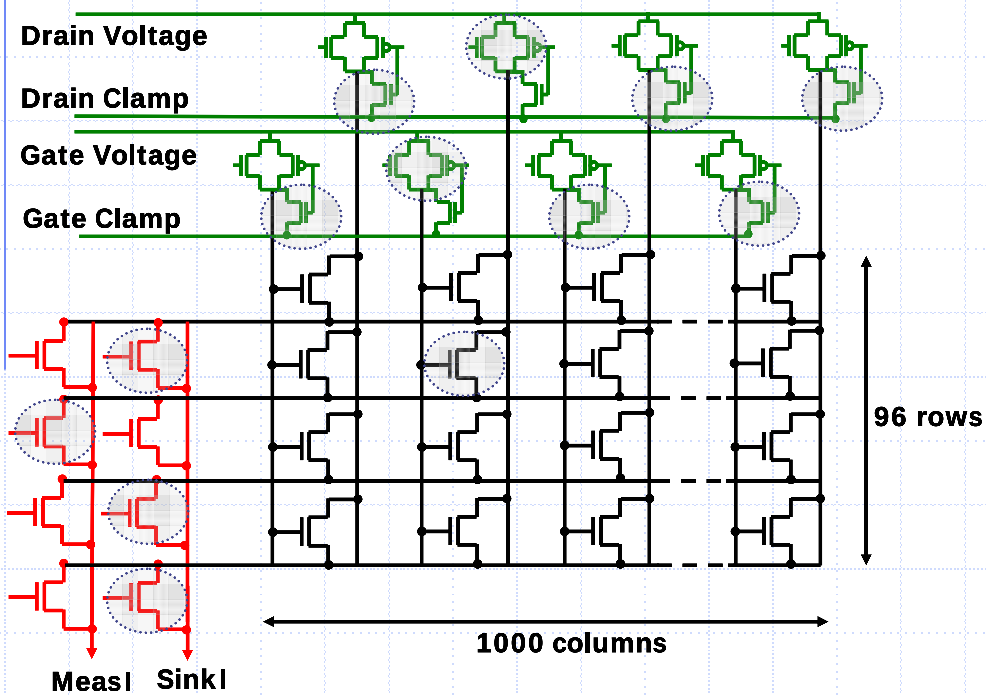
- In modern devices, the channel is very small (40 by 100nm). The number of dopant atoms is countable (hundreds), so we no longer get the averaging/smoothing effect of big numbers.
- Therefore… in modern MOSFETs, the doping of the channel is somewhat "random" and no known cause/effect model exists.
  - Simply $N_A = N(\mu, \sigma)$

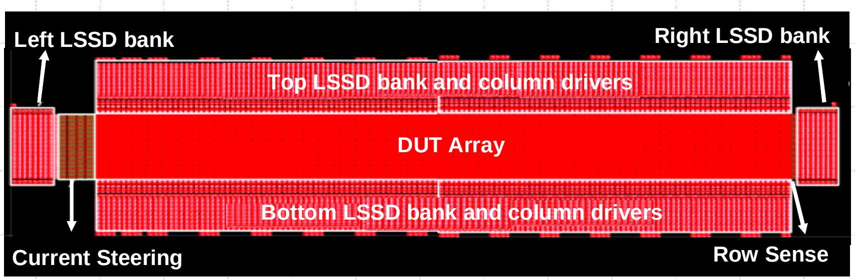




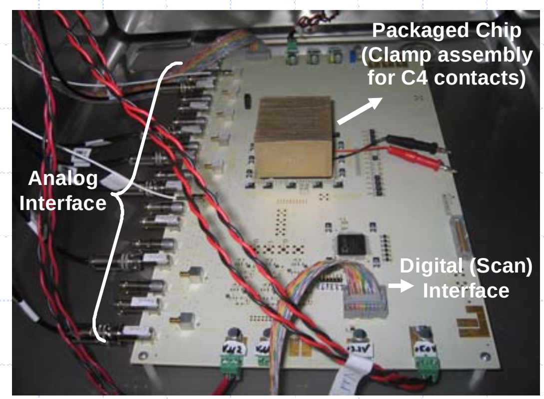
(A. Asenov group Univ. of Glasgow)

How Do We Know?

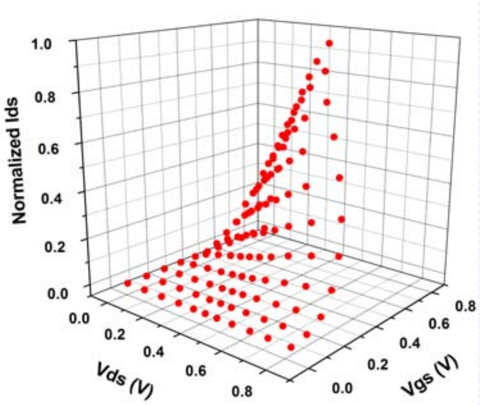


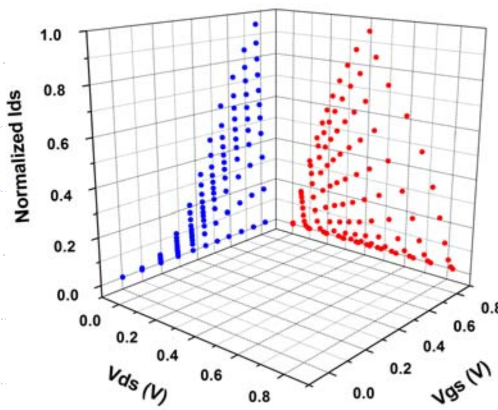


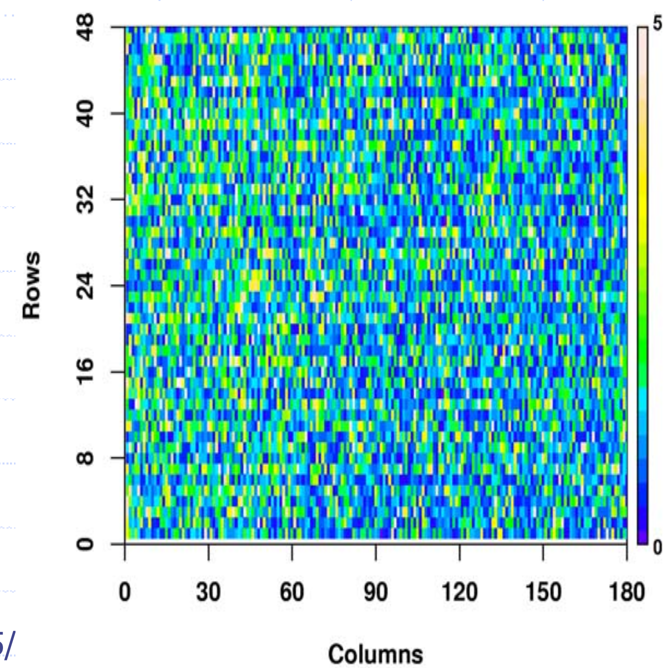
- Test structure to explore the limits of device variability.
- Small sized devices arranged in an addressable array.
- Current is "steered" in array to allow the measurement of individual devices.
- 96 rows, 1000 columns – 96,000 total devices.



Observed Output







- Measure electrical behavior of the devices by sweeping drain and gate voltages.
  - Extract parameter statistics through parameter extraction.
- Threshold Voltage statistics.
  - No spatial correlation.
  - Random dopant effect is the dominant source of variation.

Variability vs. Uncertainty

- Variability: known quantitative relationship to a source (readily modeled and simulated).
  - Designer has option to *null* out impact.
  - Example: power grid noise.
- Uncertainty: sources unknown, or model too difficult/costly to generate or simulate.
  - Usually treated by some type of worst-case analysis.
  - Example: ΔL within die variation.

- Lack of modeling resources often transforms variability to uncertainty.
  - Example: nearest neighbor noise coupling.

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Variability Characterization

- Two fundamental goals:

- Understanding the sources and magnitude of physical variability in the manufacturing process.
  - This is most often used to insure that the process is under control.
- Modeling/Representing these variabilities in a manner useful for IC design.
  - This is needed in order to create a design which can survive the variability.
- (Both has to be done in a timely fashion and at a reasonable cost)

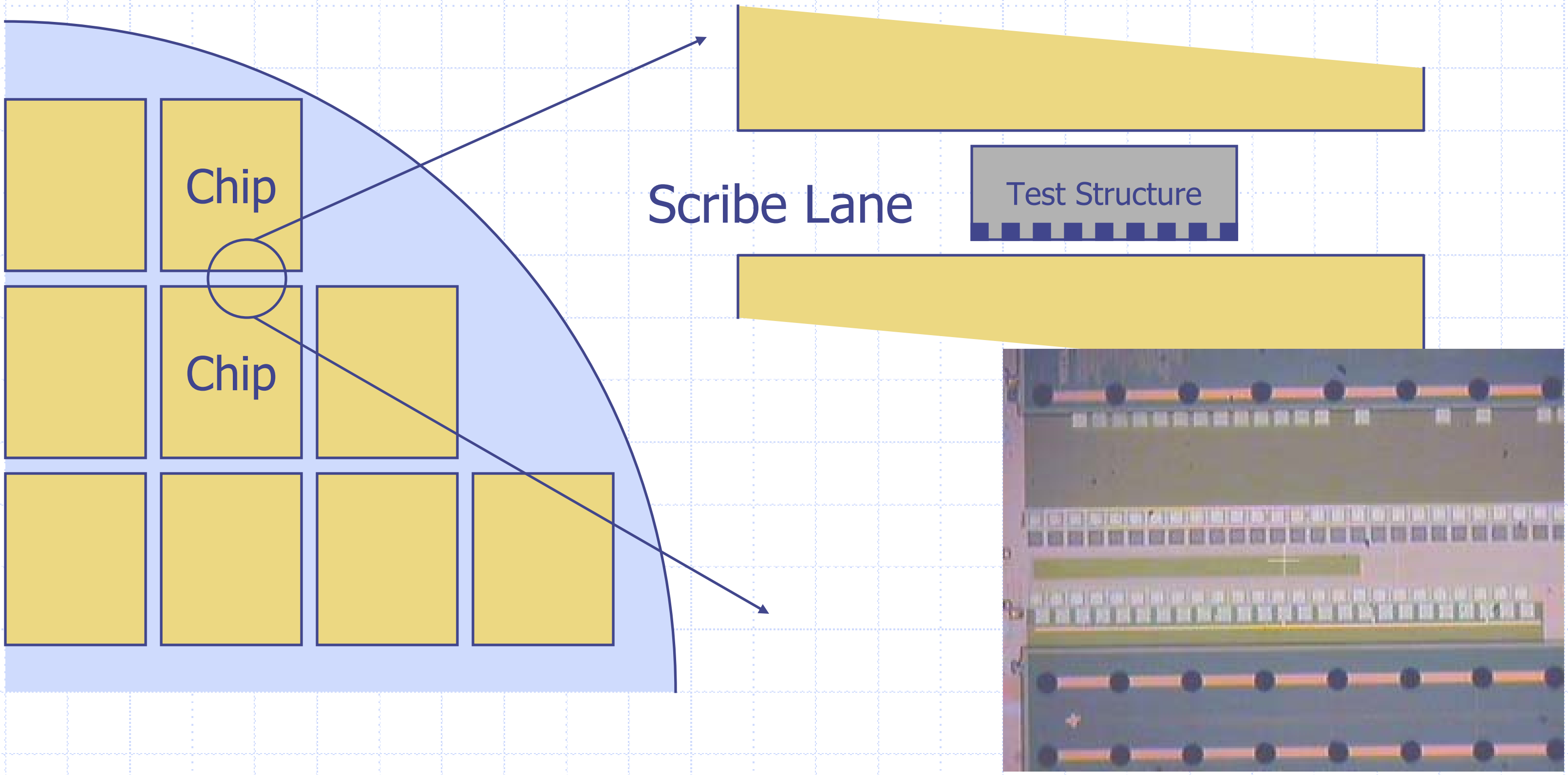
Technology Characterization

- Since the process has many sources of random and systematic variability, and since they are not always well understood, it is important that they are "monitored" in order to insure that the process is performing as specified.

- Such monitoring is done routinely in the manufacturing line.

Technology Characterization

- In order to use a minimum of overhead, technology characterization usually utilizes the "scribe lanes" between chips on a wafer.



Silicon Information Density

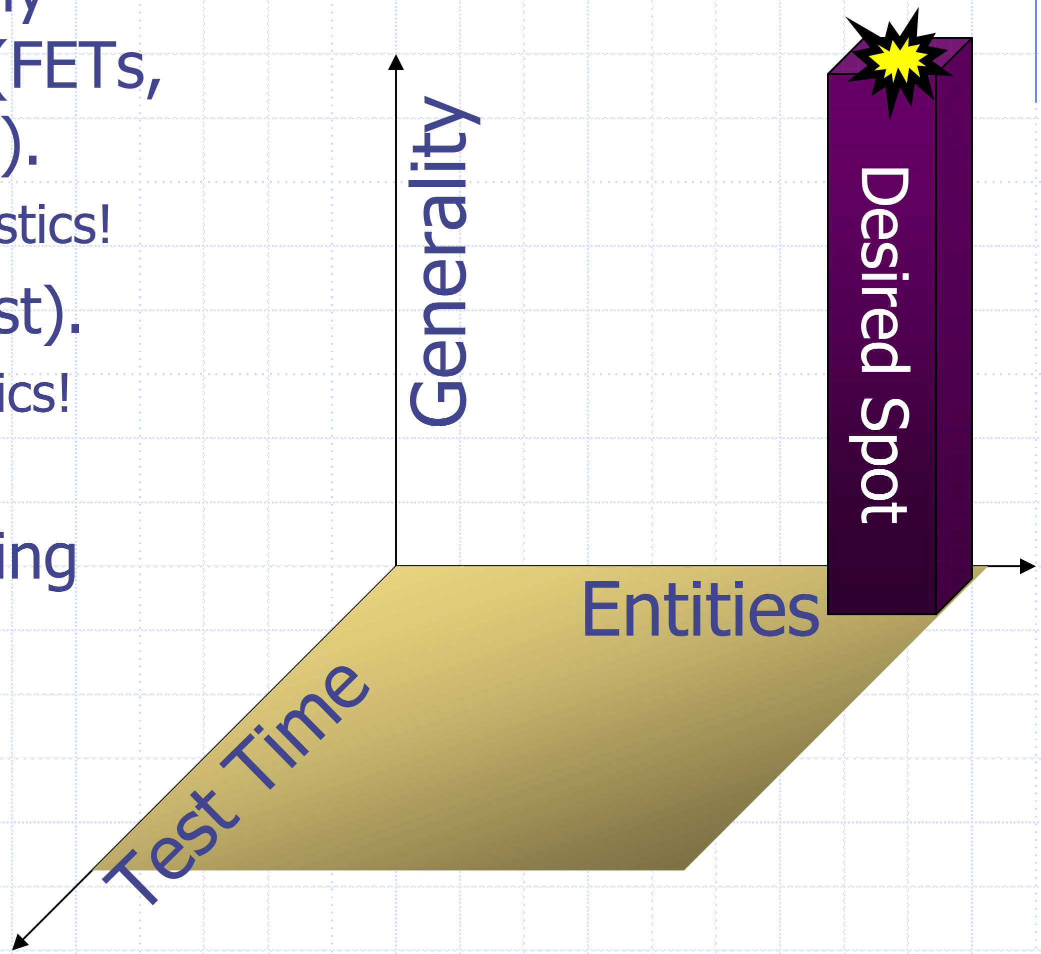
- The efficiency with which we can perform precise variability characterization is going to become important.
  - No longer sufficient to do it once (technology bring-up). Need to continually model and re-evaluate.
  - As EDA tools ramp up on understanding process, they will enable new methods of design optimization (e.g. during re-spins).

- Need vastly more information from scarce Si & test resources (increase density)!

Test Structure Quality?

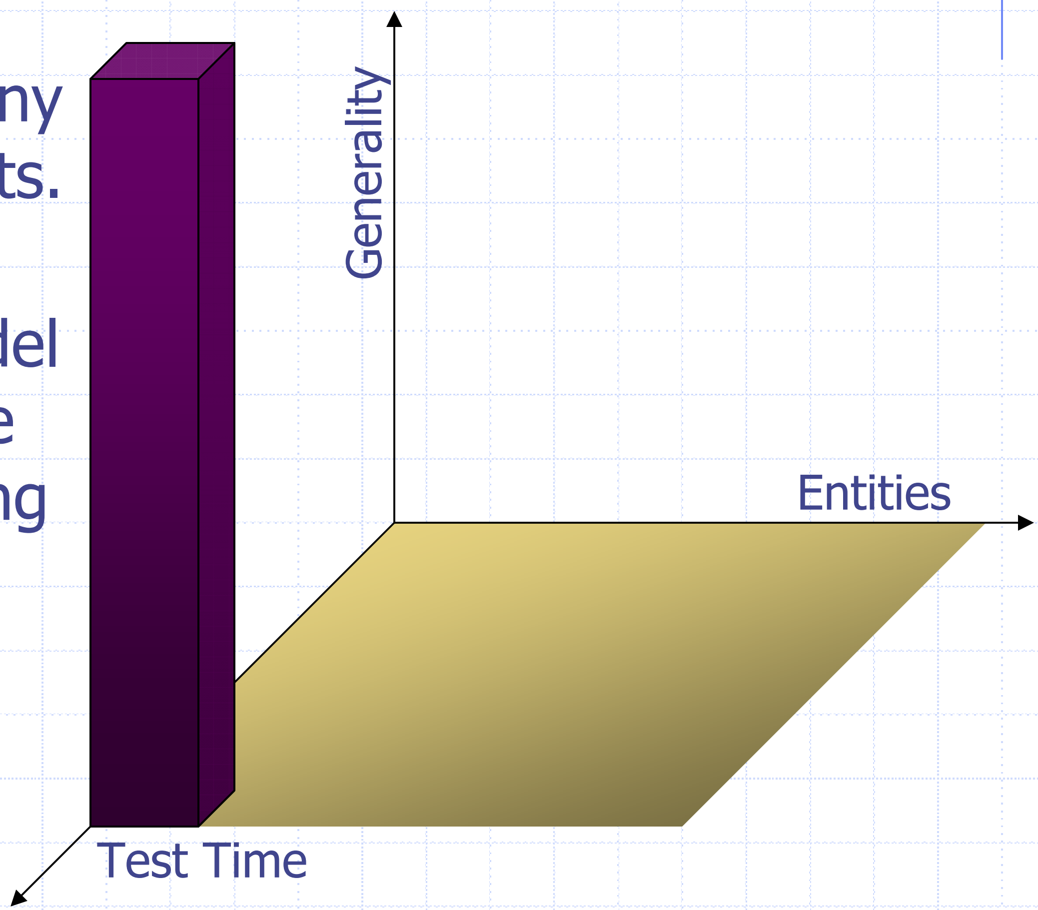
Three relative measures:

- Number of individually measurable entities (FETs, ring oscillators, etc…).
  - Many entities $\Rightarrow$ statistics!
- Test time (or test cost).
  - Lower cost $\Rightarrow$ statistics!
- Generality of result: suitability for predicting design outcome.
  - Modeling & EDA.



Example: Device Characterization

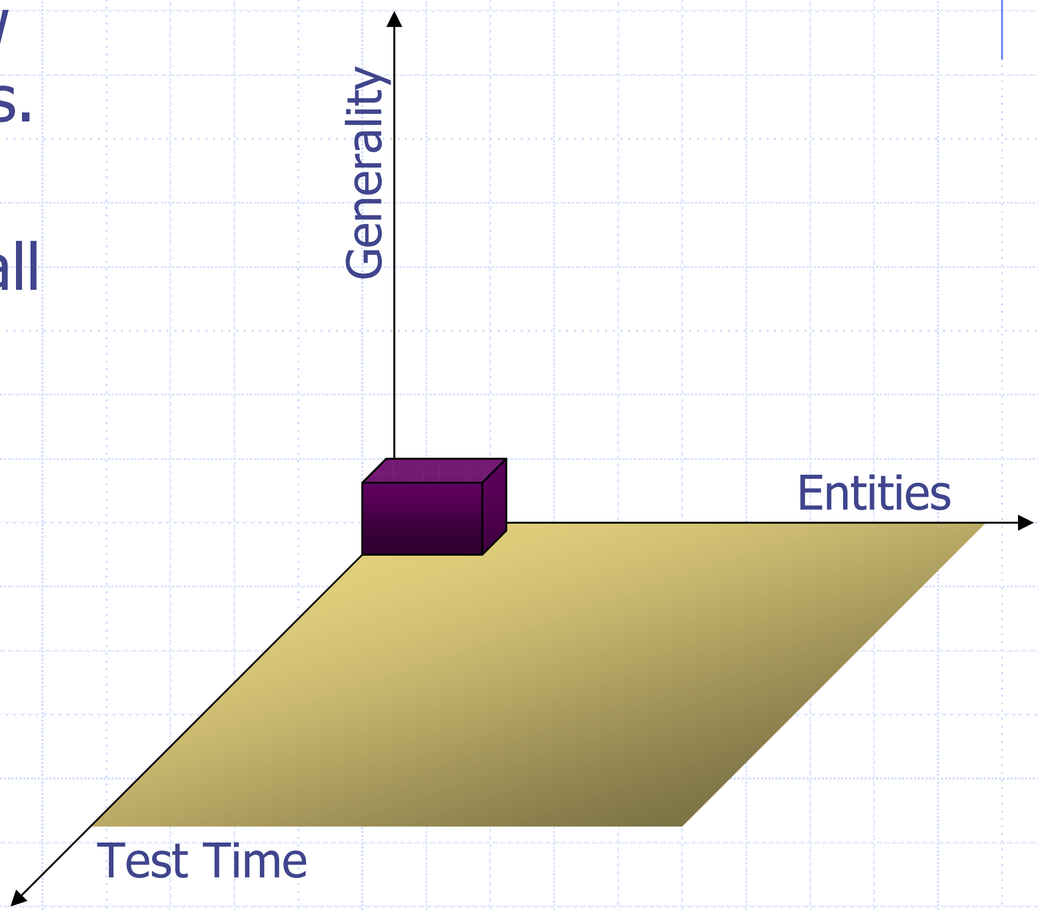
- Small number of devices with various dimensions.
  - Entities ↓.
- Typically measure many current / voltage points.
  - Analog test time ↑.
- Used to generate model parameters, which are the basis for everything else… (e.g. BSIM)
  - i.e. generality ↑↑.



Example: Ring Oscillators (ROs)

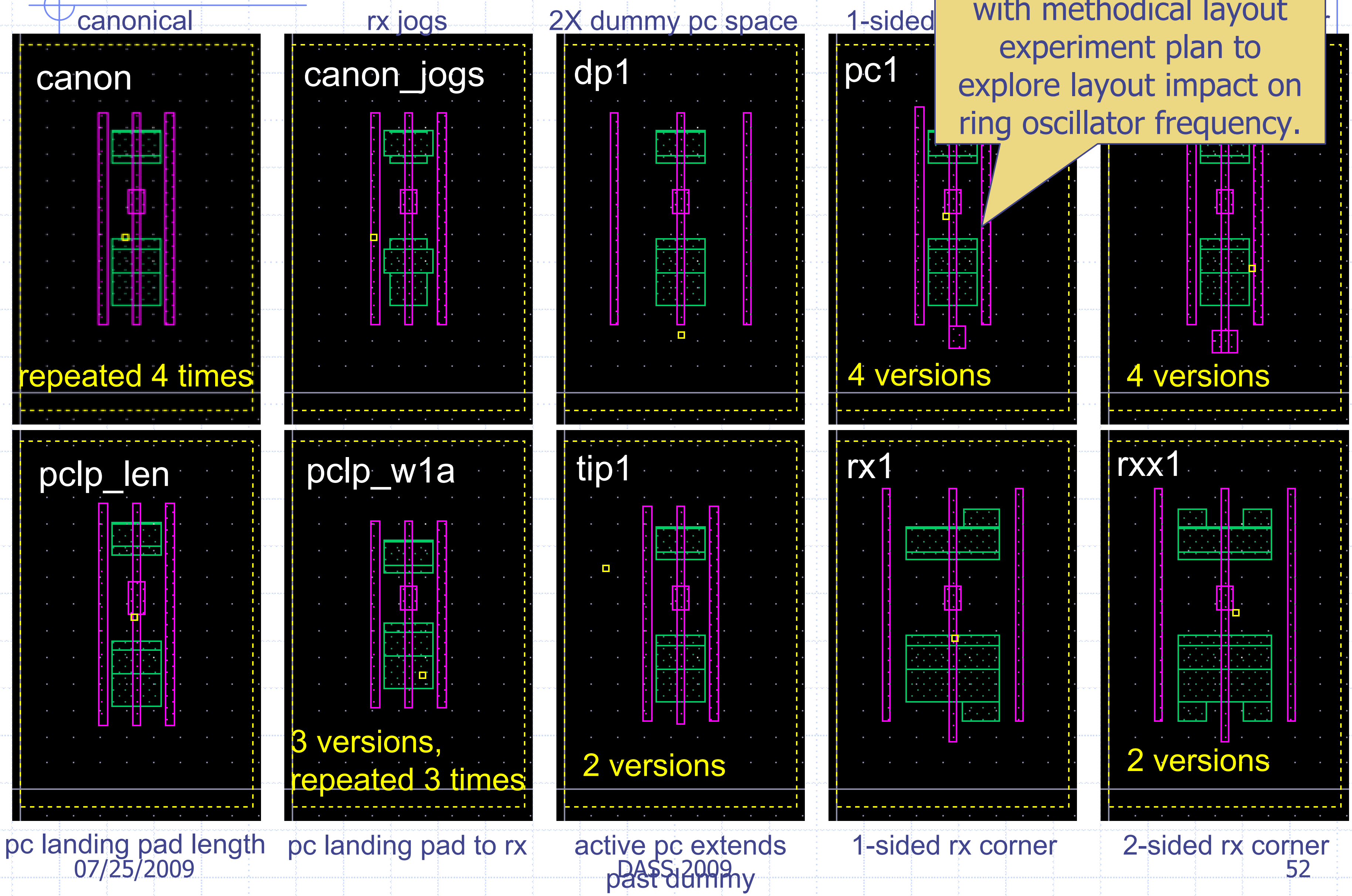
- Few ROs per unit.
  - Entities ↓.
- Typically measure few frequency & I_{DD} points.
  - Fast test ↓.
- Useful to assess overall health of process, but result is unique to RO structure.
  - i.e. generality ↓.

  - Remember this fact!

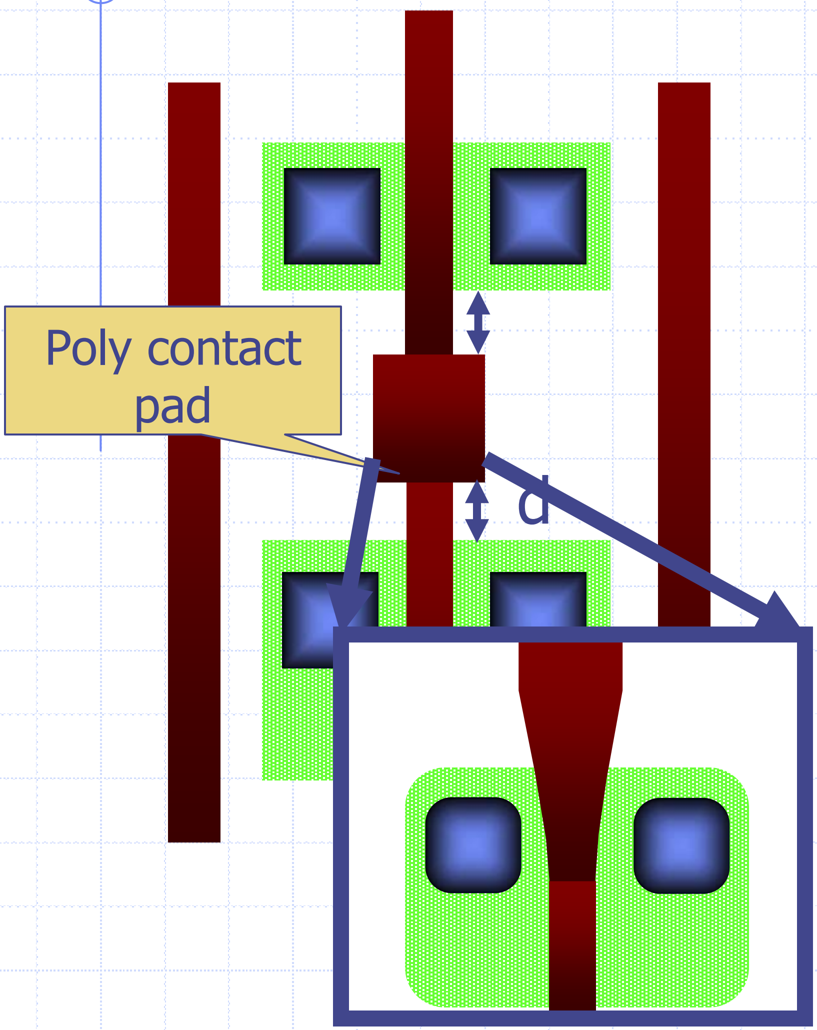


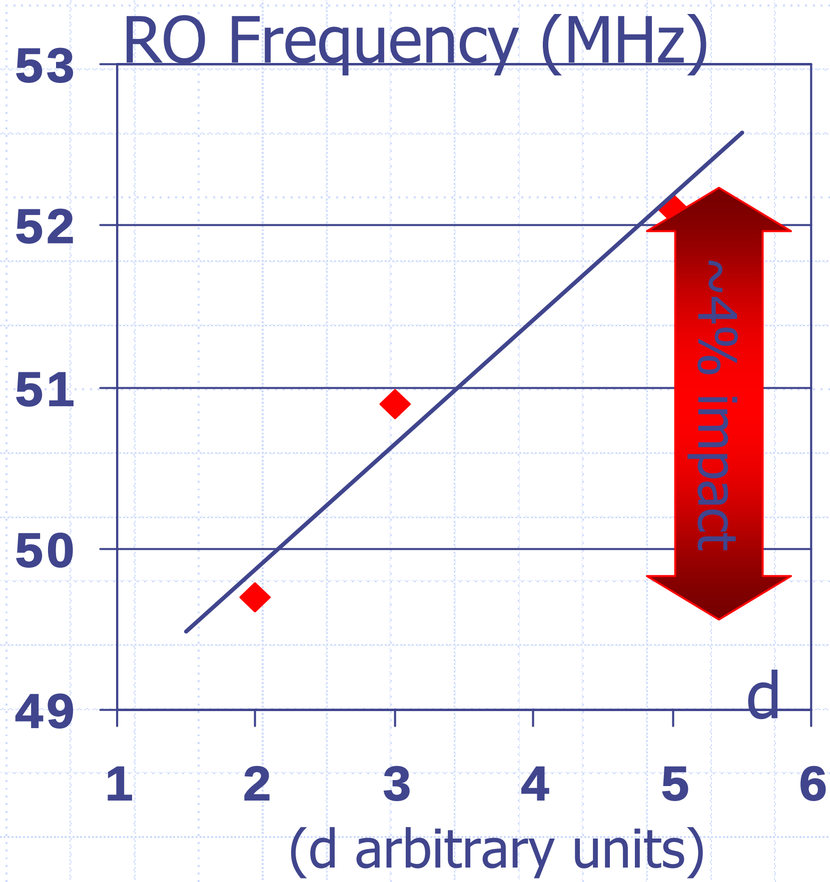
Test Structure Example

Variety of CMOS inverters with methodical layout experiment plan to explore layout impact on ring oscillator frequency.



Test Structure Output





Technology Representation

- Deals with how the results of technology characterization are summarized for design.
- Must recognize that the full complexity of the manufacturing process is not of great interest to any designer… (yawn).
- What is the appropriate level of representation for process capability and process variability?

Design/Technology Interface

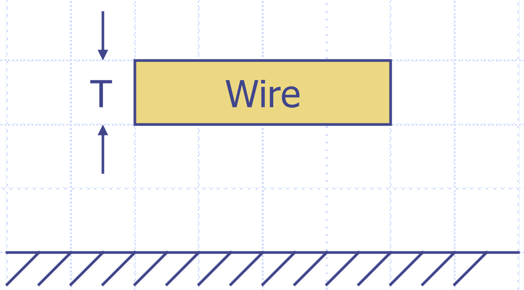
- The classical interface has been a combination of design rules and electrical models.
- Design rules represent limits on the layout that can be manufactured in a given process.
  - These are becoming more complex, and we will come back to this later.
- Electrical models represent the behavior of the active and passive elements of the chip.
  - Active: MOSFET.
  - Passive: R, C, L, wire, etc…

Electrical Models

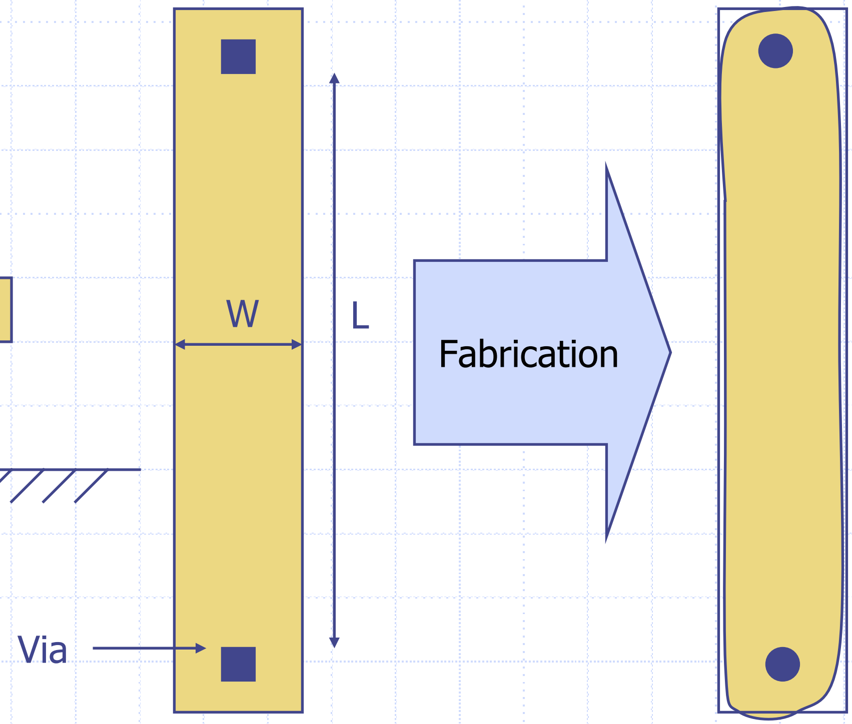
- Simplest case… Wire resistance.
- $R = (\rho / T)\,(L - \Delta L) / (W - \Delta W)$

The ρ/T term is often combined into a quantity called the "sheet resistance"

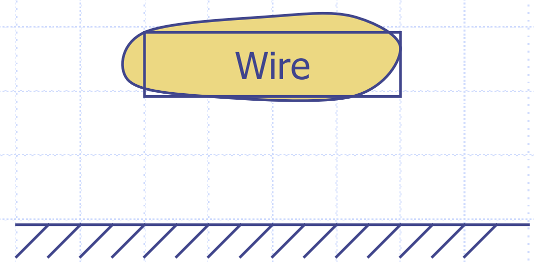
Parameter	Explanation
ρ	Static resistivity in ohms/meter
T	"effective" wire thickness
L, W	Dimensions of wire
ΔL, ΔW	Offsets to wire dimensions



Side View



Layout



Electrical Model Parameters

- Even for something as simple as a resistor, there are a number of quantities that need to be known in order to calculate the resistance.
- Variations in T, ΔL, and ΔW will change the value of the resistance.
- Values of T, ΔL, and ΔW may be represented as ranges or distributions!
- If ΔW is related to W, L, or some other layout factor then we would classify it as systematic variation! Otherwise it is random.

Complex Electrical Models

- Resistors are quite simple devices…
- MOSFETs require much more complex representations.
  - They are non-linear devices.
  - They are strongly voltage dependent (it is a switch after all).
  - They have both current as well as charge.
- So MOSFET models have many more parameters (10s to many 100s).
  - But a few are "primary" variables.

So What?

- MOSFET models are complex, and typically require many parameters.
  - Even though a few are primary. The rest are for smoothing purposes.
- How do we get values for these parameters?
  - Recognizing that these values may just be “estimates”.
- How do we get the associated statistics?
  - Recognizing that the statistics may not be stationary.

"Parameter Extraction"

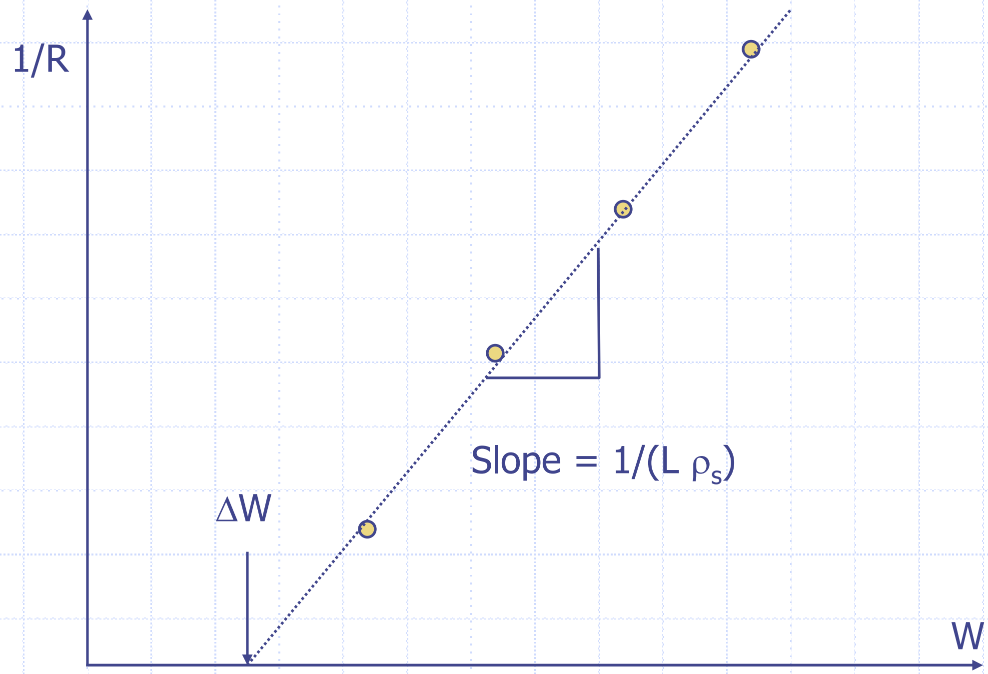
- Given the observed behavior of a device, and a set of equations describing the behavior, identify the values of the "parameters" in the equations.

- For a resistor, we had written:
  - $R = \rho_s (L - \Delta L) / (W - \Delta W)$

- So if I measure a number of LONG resistors with varying W, I can…

Resistor Modeling

- Long L means L » ΔL, so equation is:
  - $R = \rho_s L / (W - \Delta W)$
- Can get ΔW and ρ_s by linear least squares…



More Complex Models

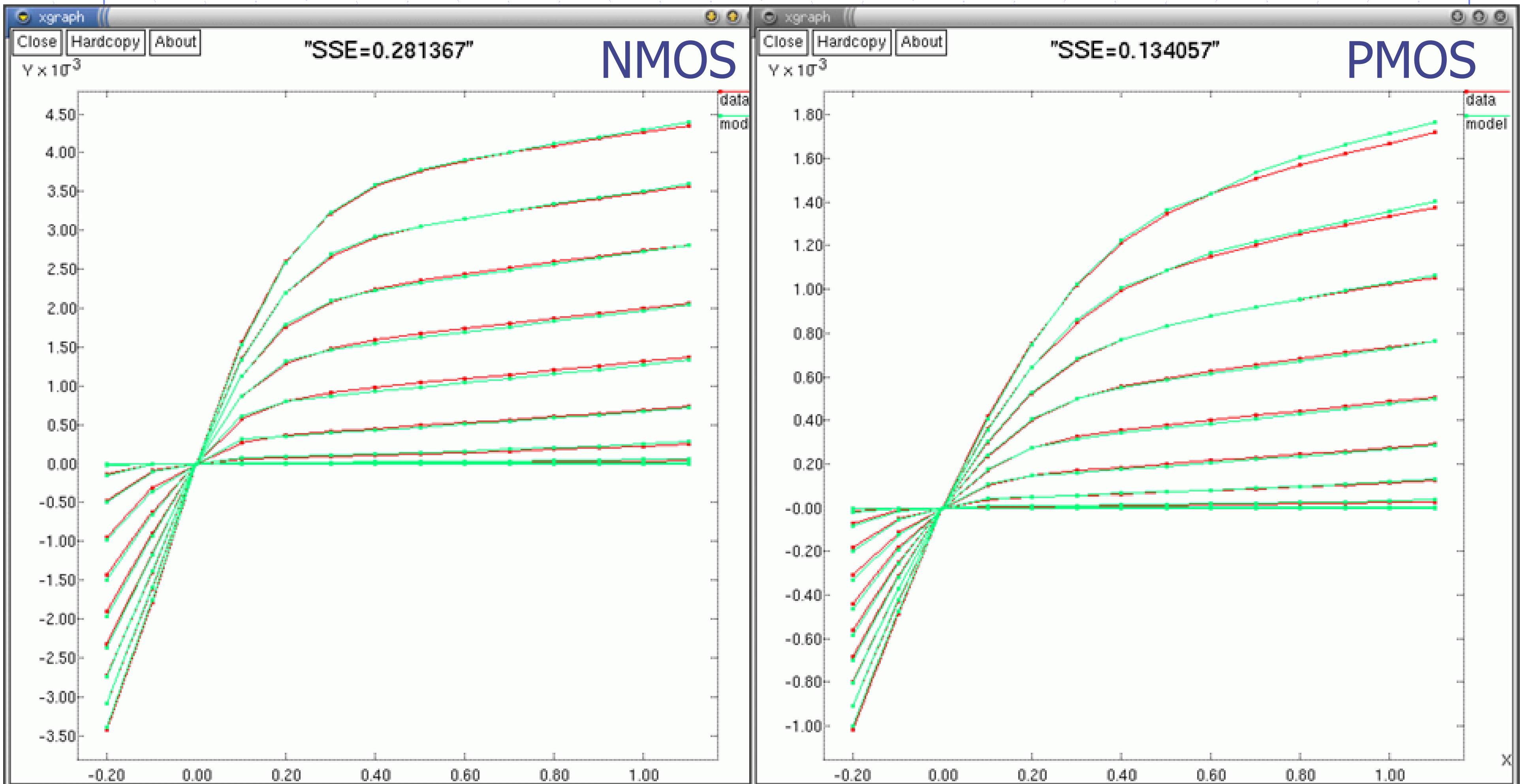
- For MOSFET and other models, simple graphical methods are not generally possible.
- Numerical techniques, Non-Linear Least Squares, are usually used.
  - Not an easy problem, especially in higher dimensions.
- Formulation:

$$\min_P \| y - f(x, P) \|_2$$

Parameter	Explanation
y	Output of interest, drain current.
x	Input to the model, terminal voltages
P	Vector of model parameters

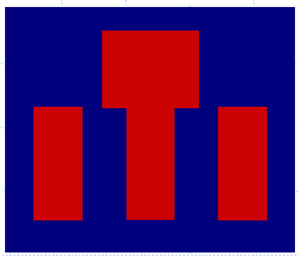
Example of Parameter Extraction

- Fits resulting from an in-house tool.

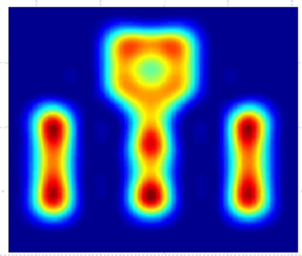


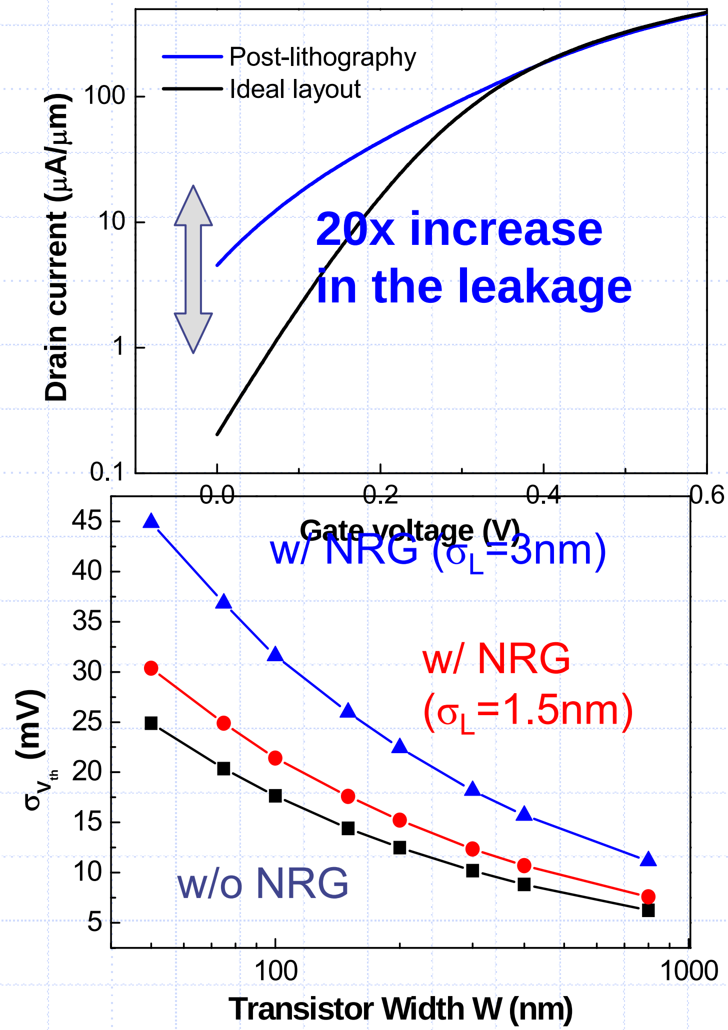
Modeling of Non-Rectangular Poly Gates

Layout



Post-litho



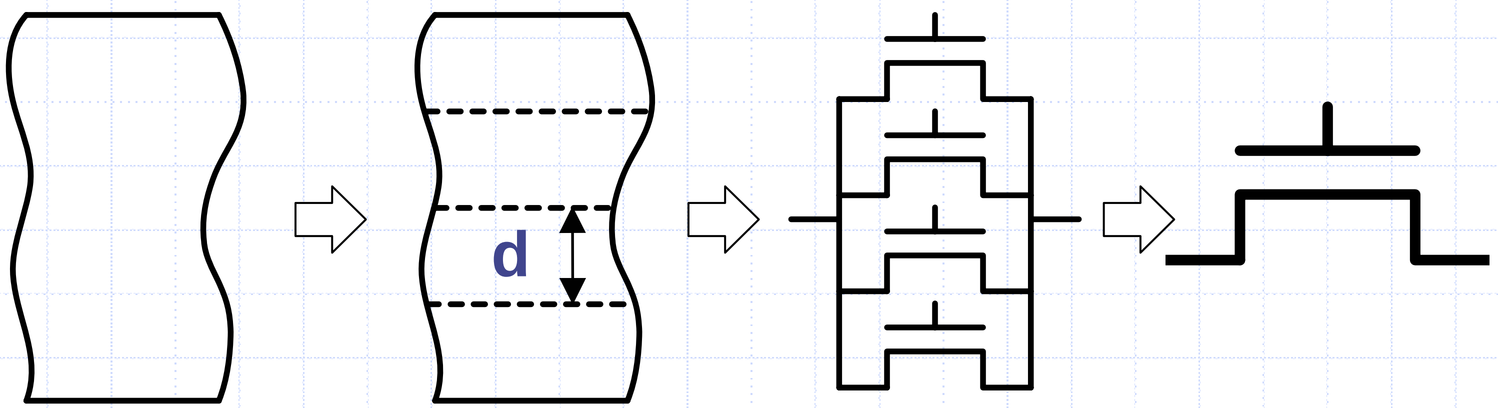


Source: Y. Cao

- FET driving strength interacts with RDF and layout
- Gate slice with shorter length dominates the variation and the leakage

Simulation and Modeling

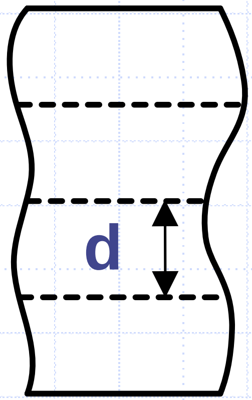
- Lithography simulation: available to predict NRG effect
- TCAD: a traditional problem with 3D Monte-Carlo atomistic simulations
- Compact modeling: desirable for efficiency and flexibility

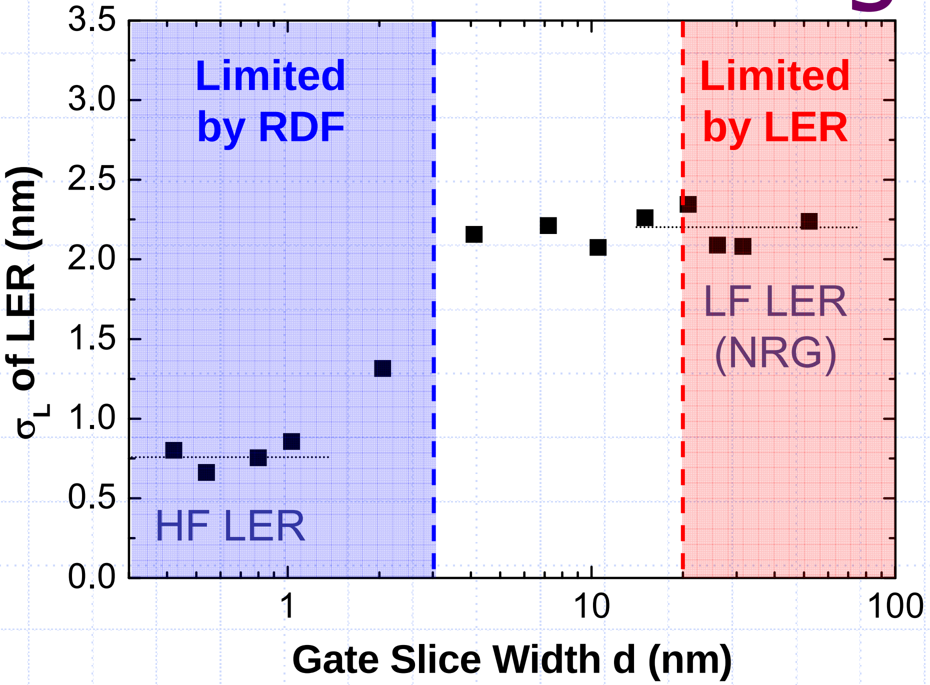


- Gate slicing: How to select the slice width?

Source: Y. Cao

The Limitations of Gate Slicing





- Upper bound: spatial period of LER
- Lower bound: the correlation length of random channel potential
- The summation of current is only applicable to $\boldsymbol{I_{on}}$, not I_{off}

$$I_{off} \propto \exp\left(-\frac{V_{th}}{nkT/q}\right) \qquad I_{on} \propto \left(V_{gs} - V_{th}\right)$$

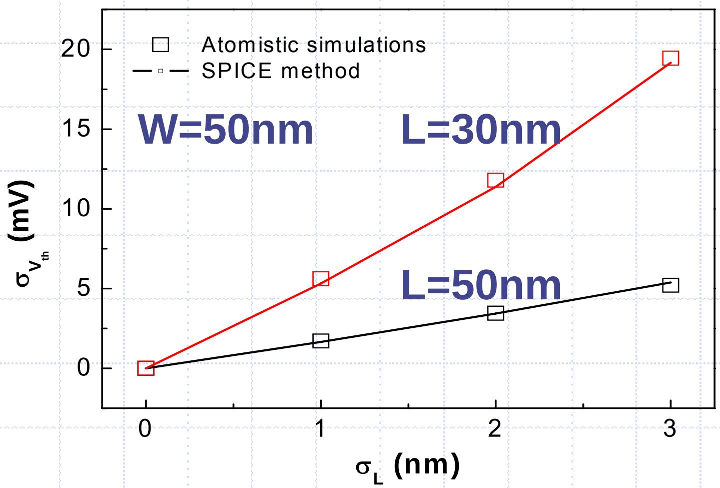
[J. Croon, IEDM, '02]

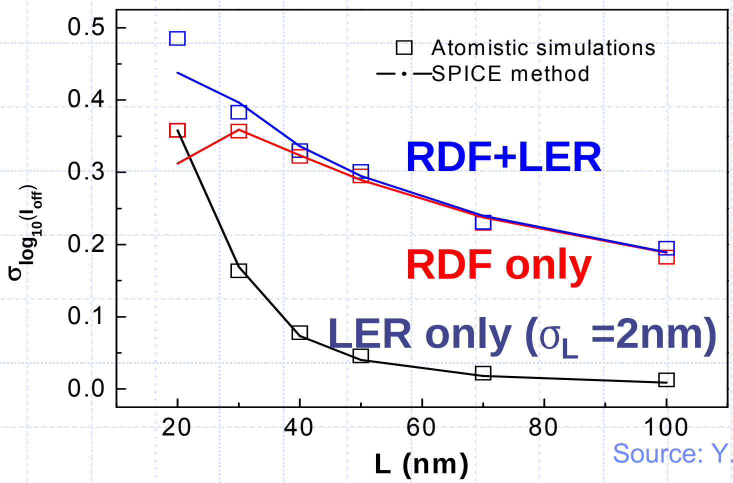
Modeling and Simulation Procedure

- Starting point: A non-rectangular gate shape with σL due to LER and σVth due to RDF

1. Gate slicing at appropriate slice width
2. Assignment of random Vth to each slice depending on its W, L, and σVth
3. Sum the current together from each slice, then extract Vth variation from Ion

→ Finish an equivalent transistor model for Vth variation under both RDF and LER

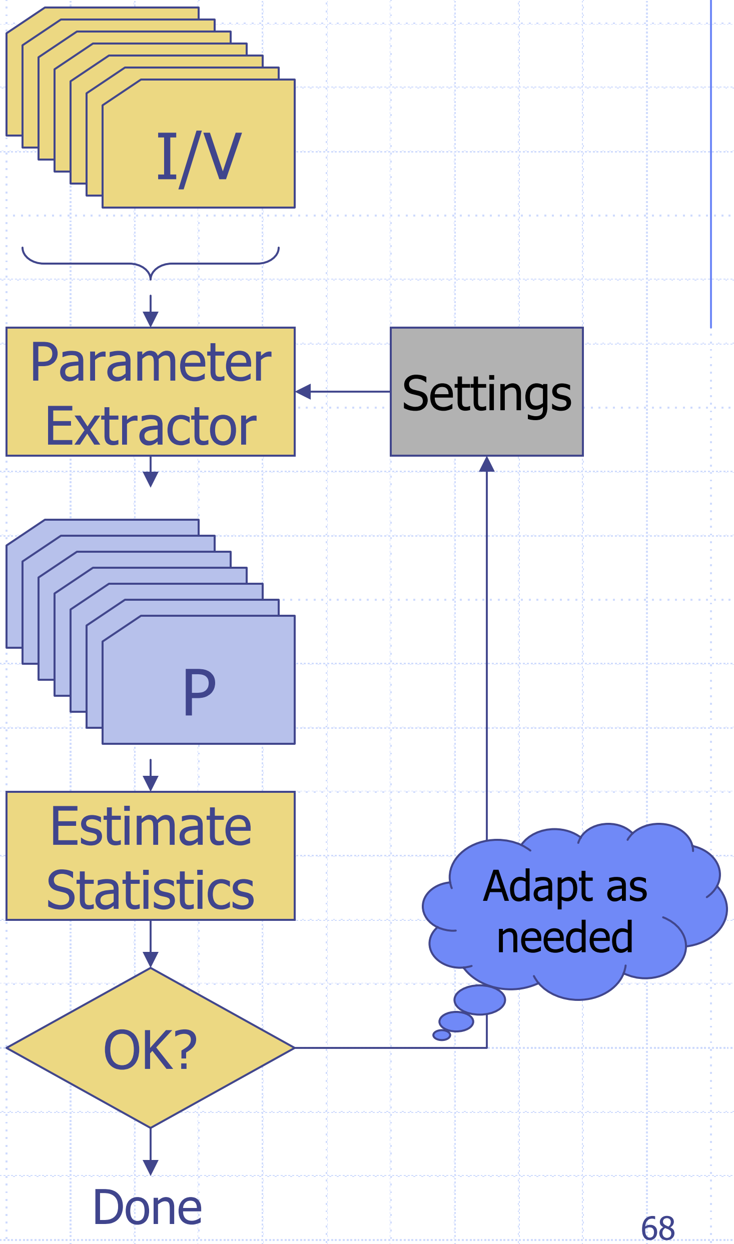




Source: Y. Cao

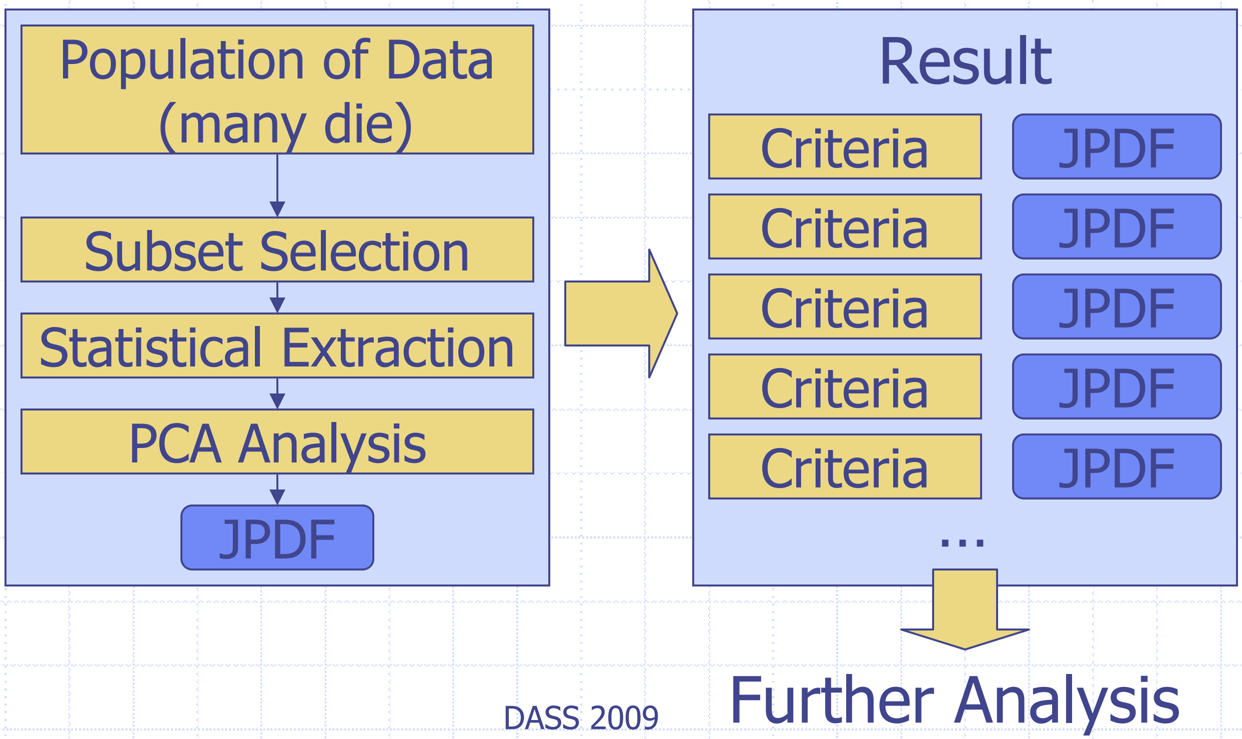
Statistical Fitting

- More complex than nominal fitting.
- Need the statistics of the resulting parameters to be "physical".
- Normal least squares fitting process requires stabilization in order to insure physicality.
- Physical ≡ correlation!
  - Because the parameters are a reflection of underlying physics of variation.



Spatial Distribution Discovery

- By doing extraction for spatial subsets (area within die) or for different die, we can infer random, systematic, within-die & die-to-die dependencies.

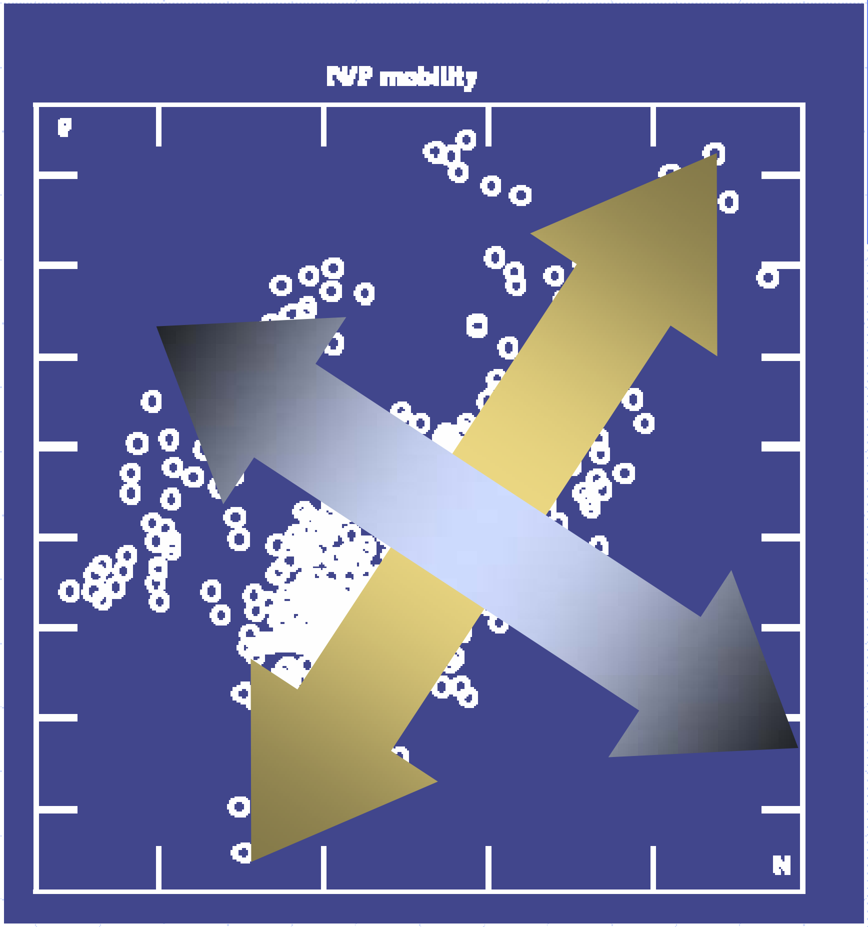


Model Parameter Representation

- There are few CAD tools that can deal with parameter distributions.
- There are few designers who want to deal with distributions.
- So… distributions are often summarized or bounded using "extreme cases".
  - Worst Case Design.
  - Corner Case Design.

Process Corners

- From the joint probability density of the model parameters, one may “select” parameter combinations that are extreme.
- Assumption: extreme parameters lead to extreme performance.
- Result: bounding of resulting performance!
- We will come back to this.



Outline

- Introduction to Variability
- A Taxonomy of Variability
- Random and Systematic Variability
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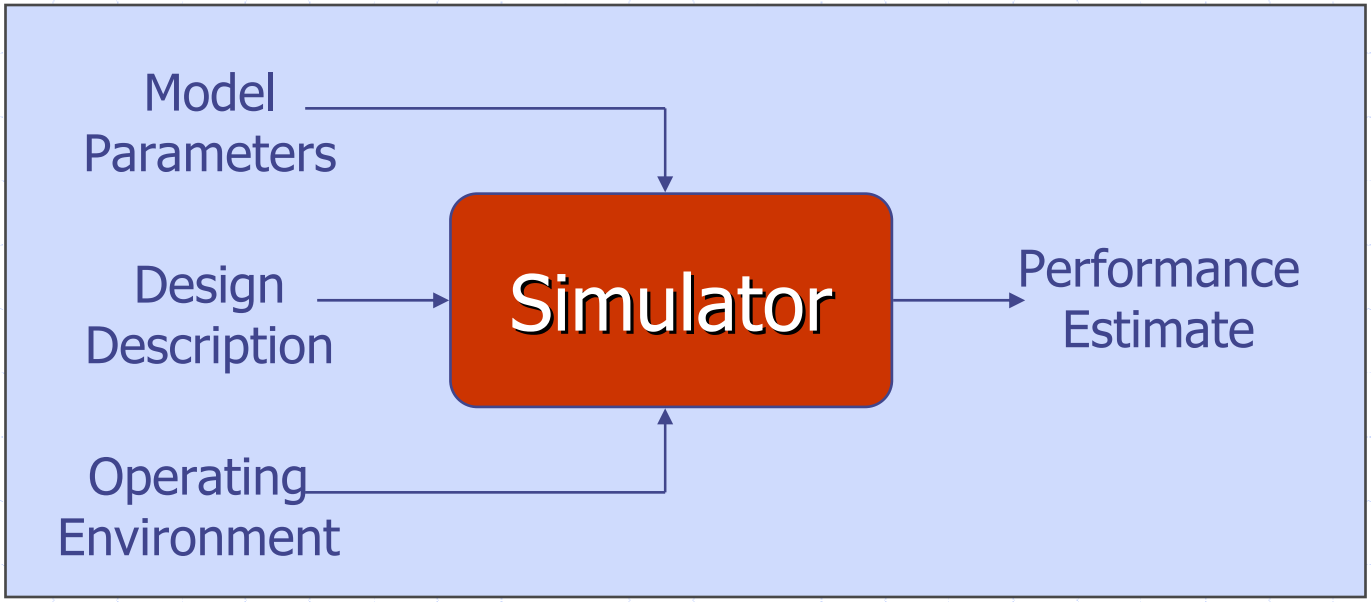
- Homework Assignment

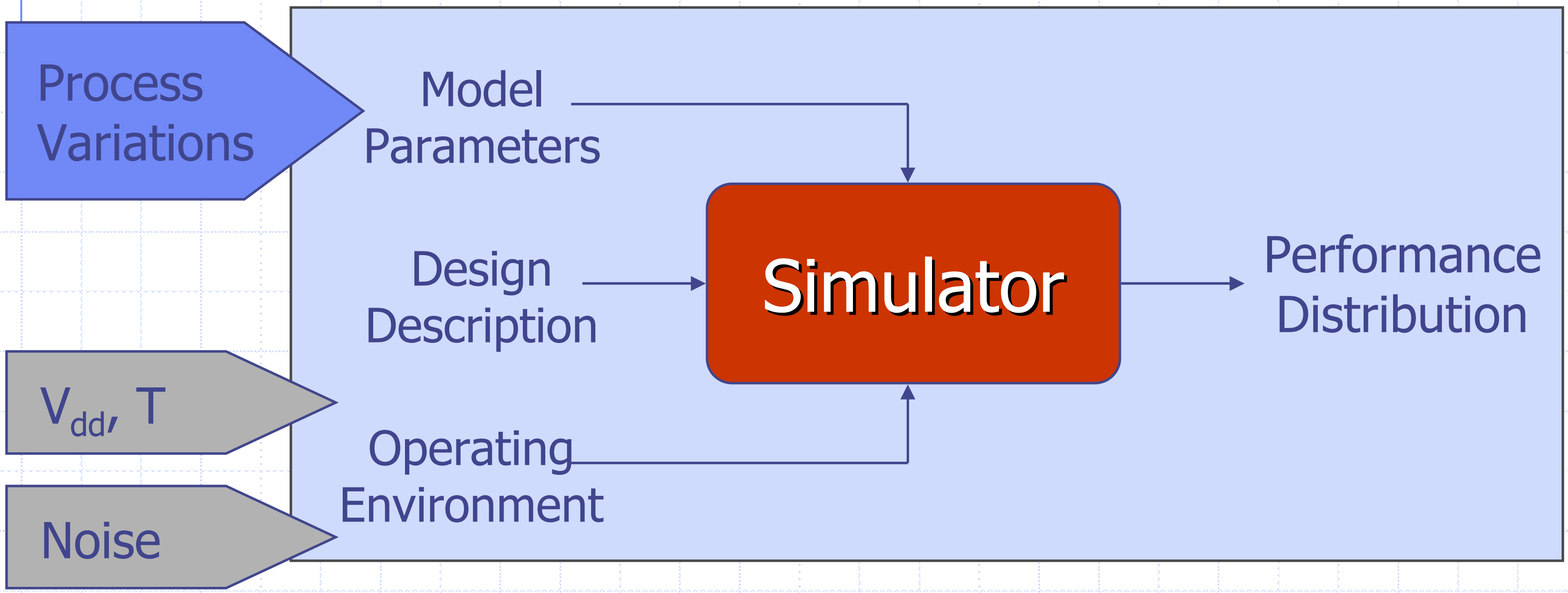
Performance Estimation

- Our industry is unique in one of it's most basic assumptions… No prototyping possible!
- Assumptions:
  - Performance measured by simulation.
  - Technology represented by model parameters.
  - Parameters have statistical distributions.



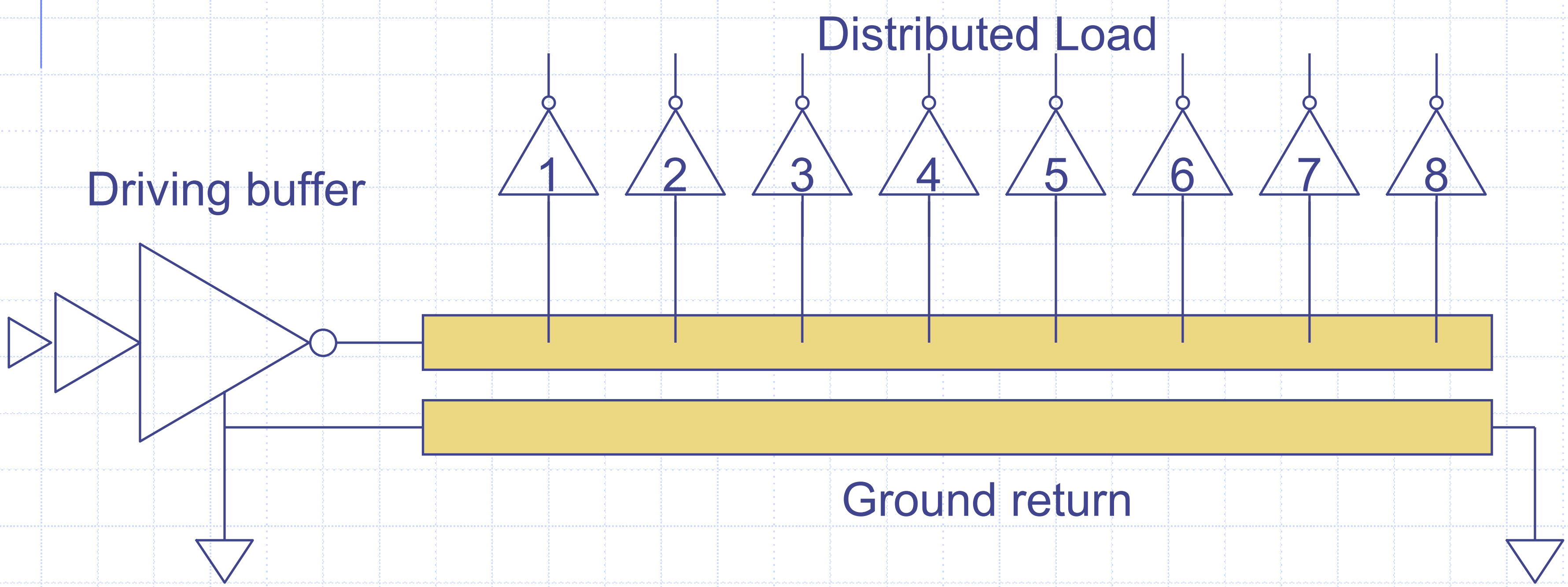
Estimating Performance Variability

- Once we can get a single value of performance, we can surely get the distribution of performance using techniques such as Monte-Carlo analysis.
  - More efficient techniques are possible of course.



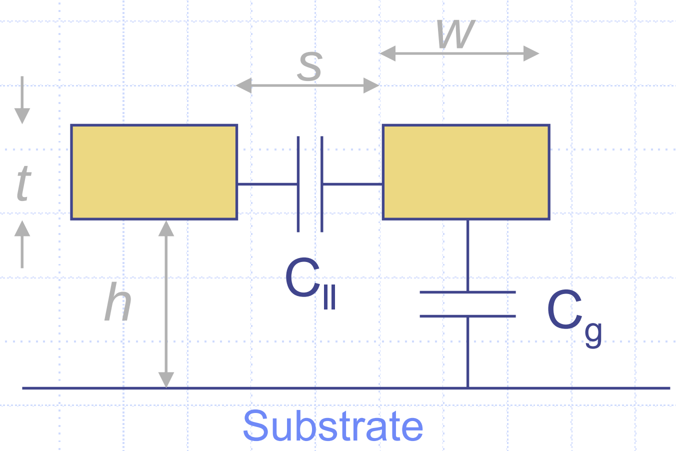
Simulation Example

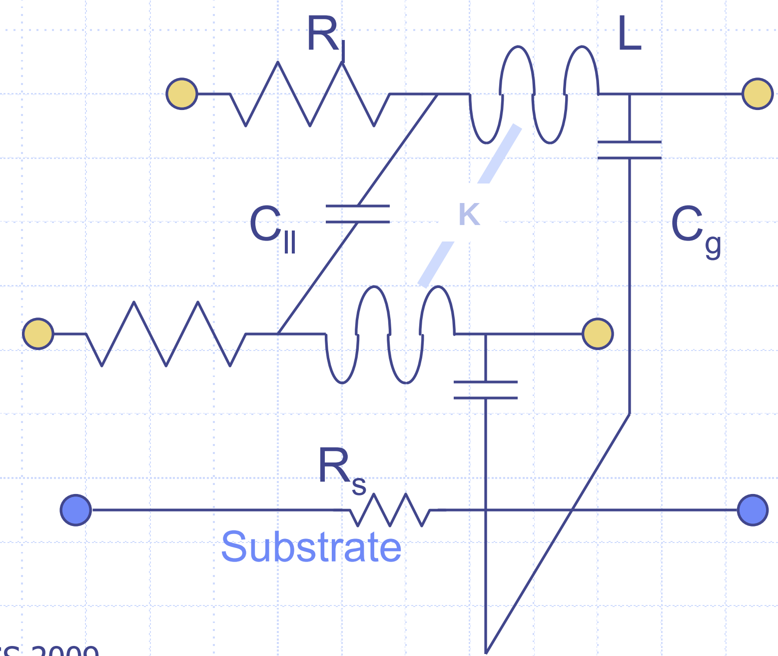
- Fictitious clock interconnect.
  - Long (1cm) wire on top-most metal layer.
  - Inductive ground-return path added.



Modeling

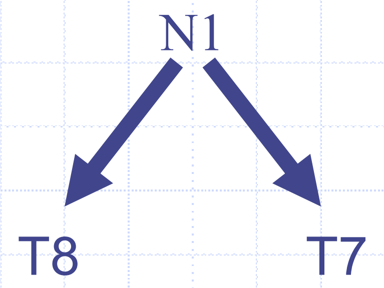
- Devices:
  - Sample of 450 extracted MOSFET parameter sets.
- Interconnect:
  - R, L and C as function of geometry (w,s,t,h).
  - All coupling modeled.
  - *Variations* from technology specification.
- Substrate:
  - Resistive.

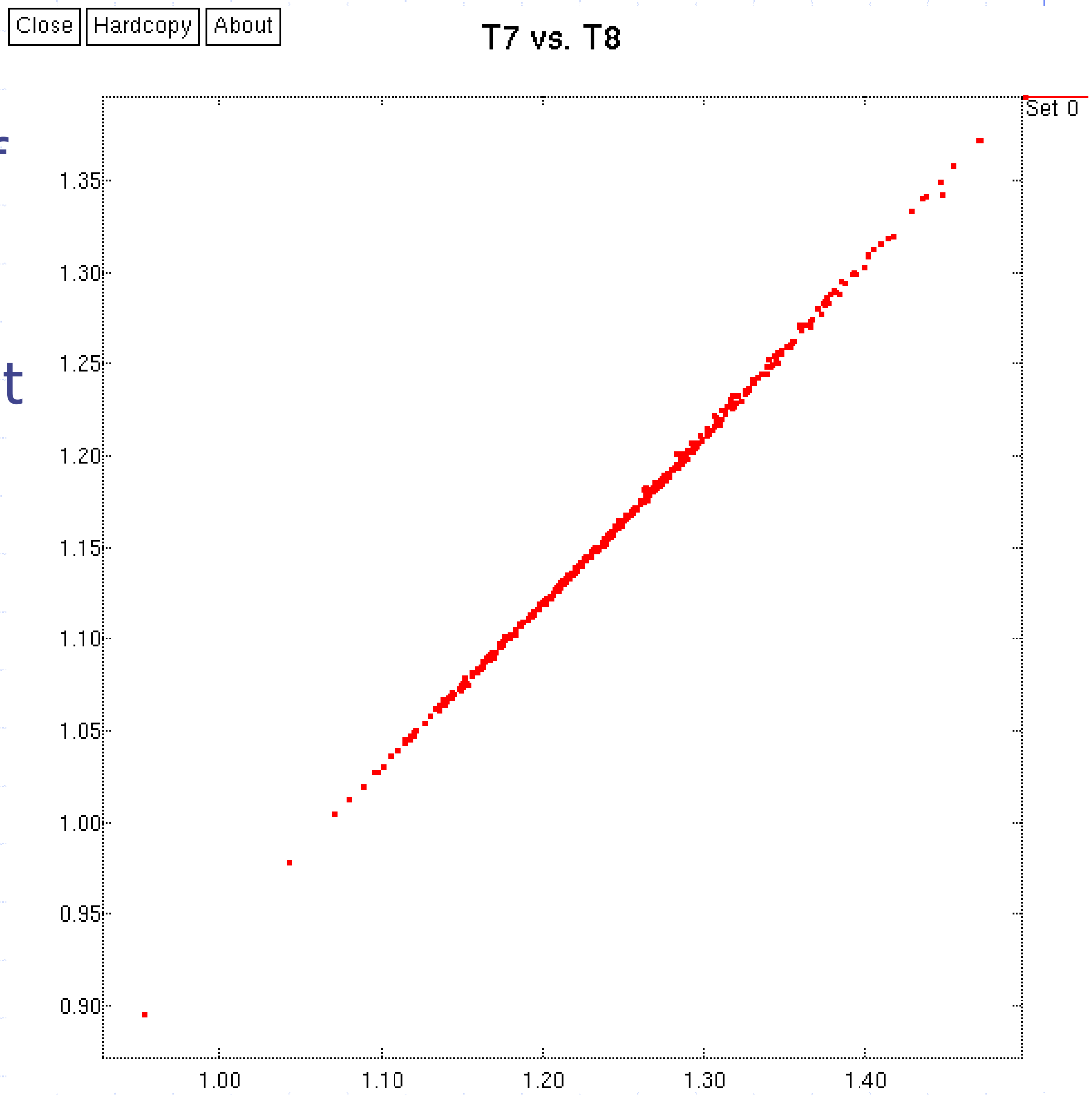




Simulation of Variations

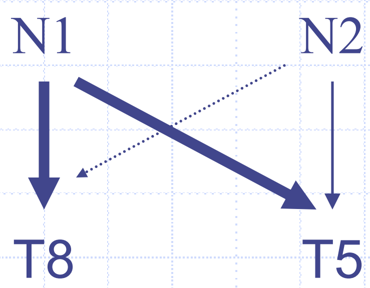
- Simulate circuit for all 450 sets of MOS model parameters.
- Measure delays at all taps.
- Delays at last 2 taps are very highly correlated.

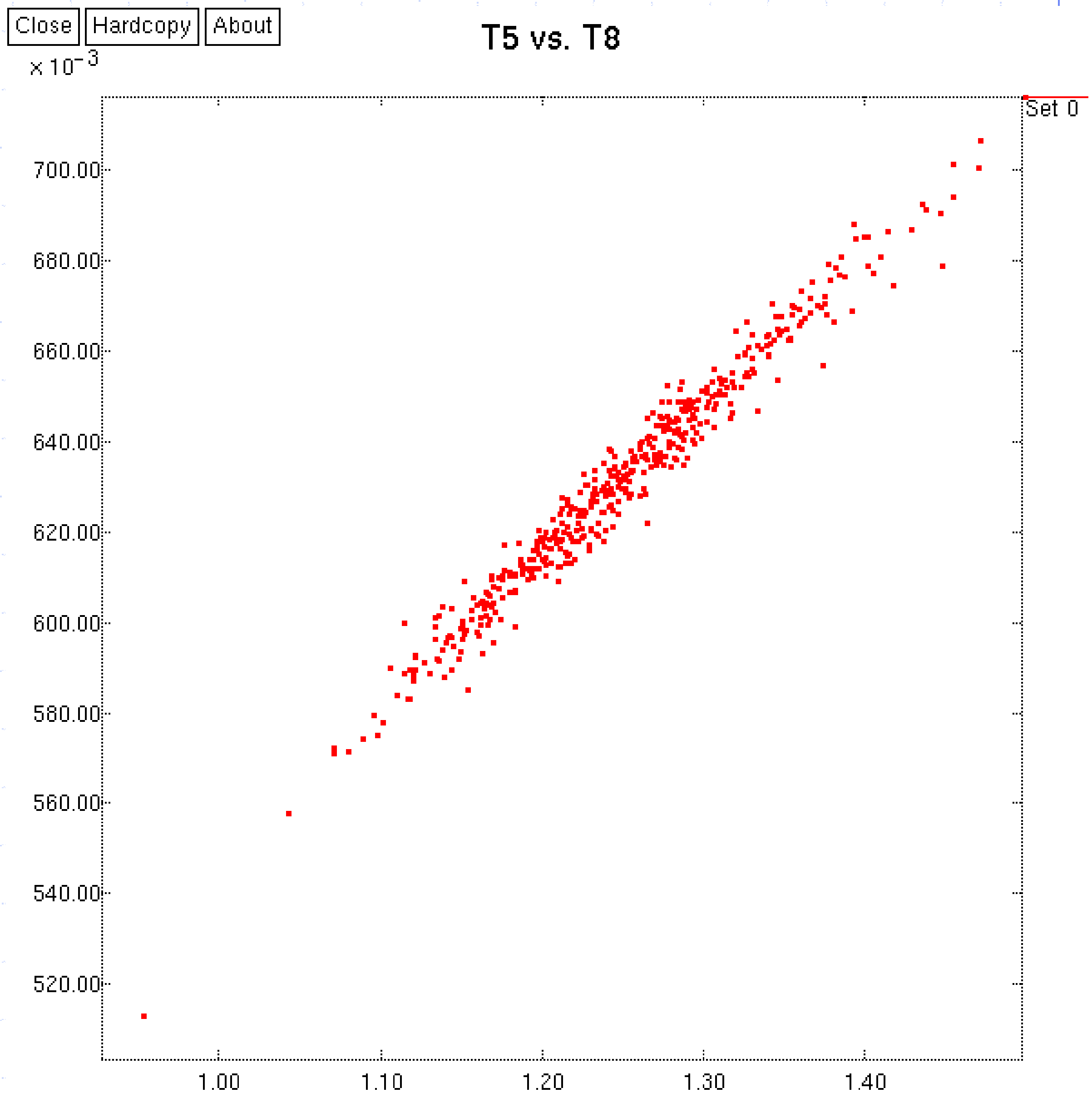




More Variations

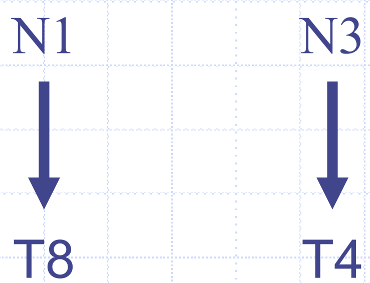
- Delays at taps 8 and 5 are *less* correlated.
- The 2 delays have different sensitivities to underlying noise sources!

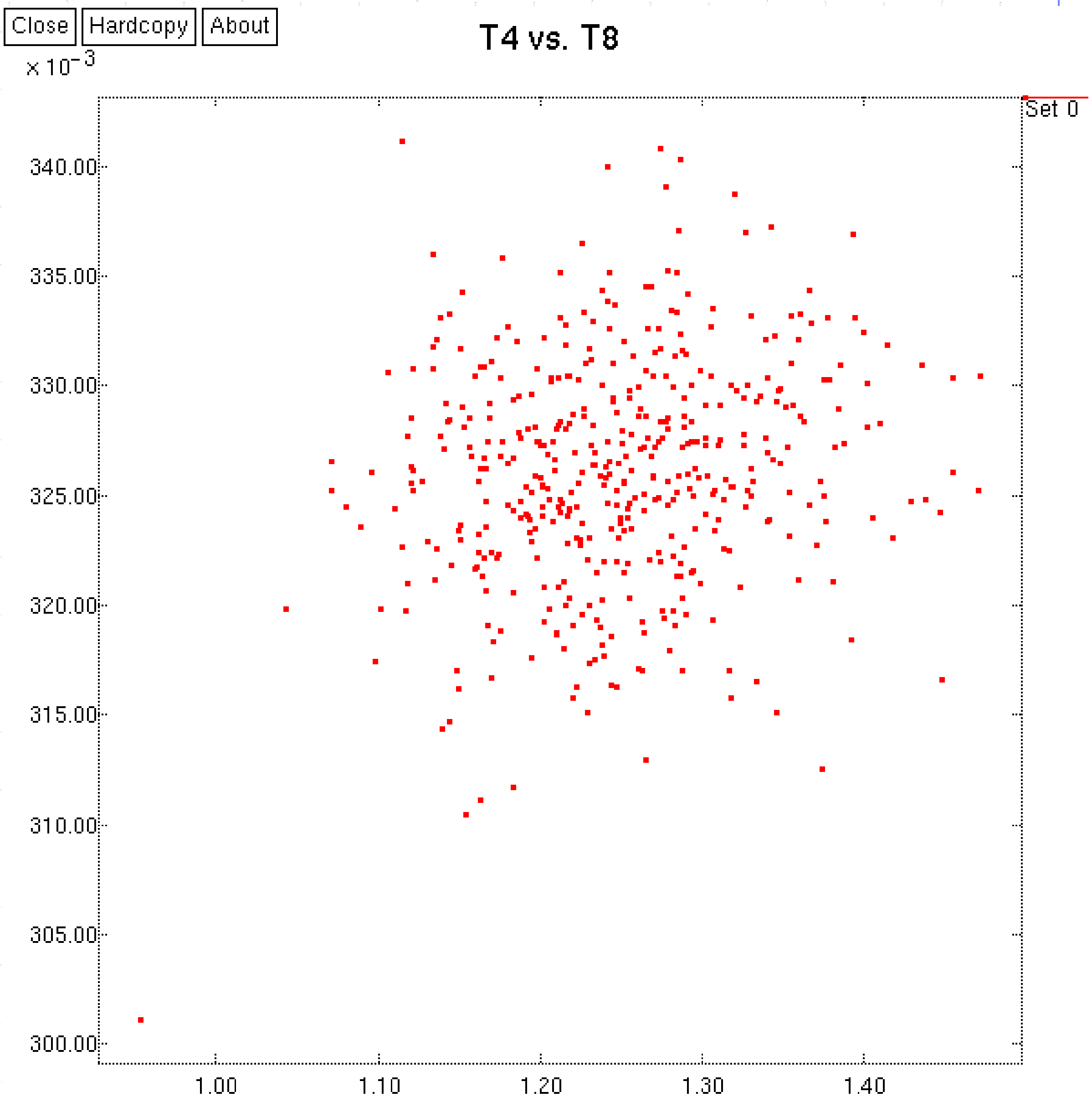




More Variations

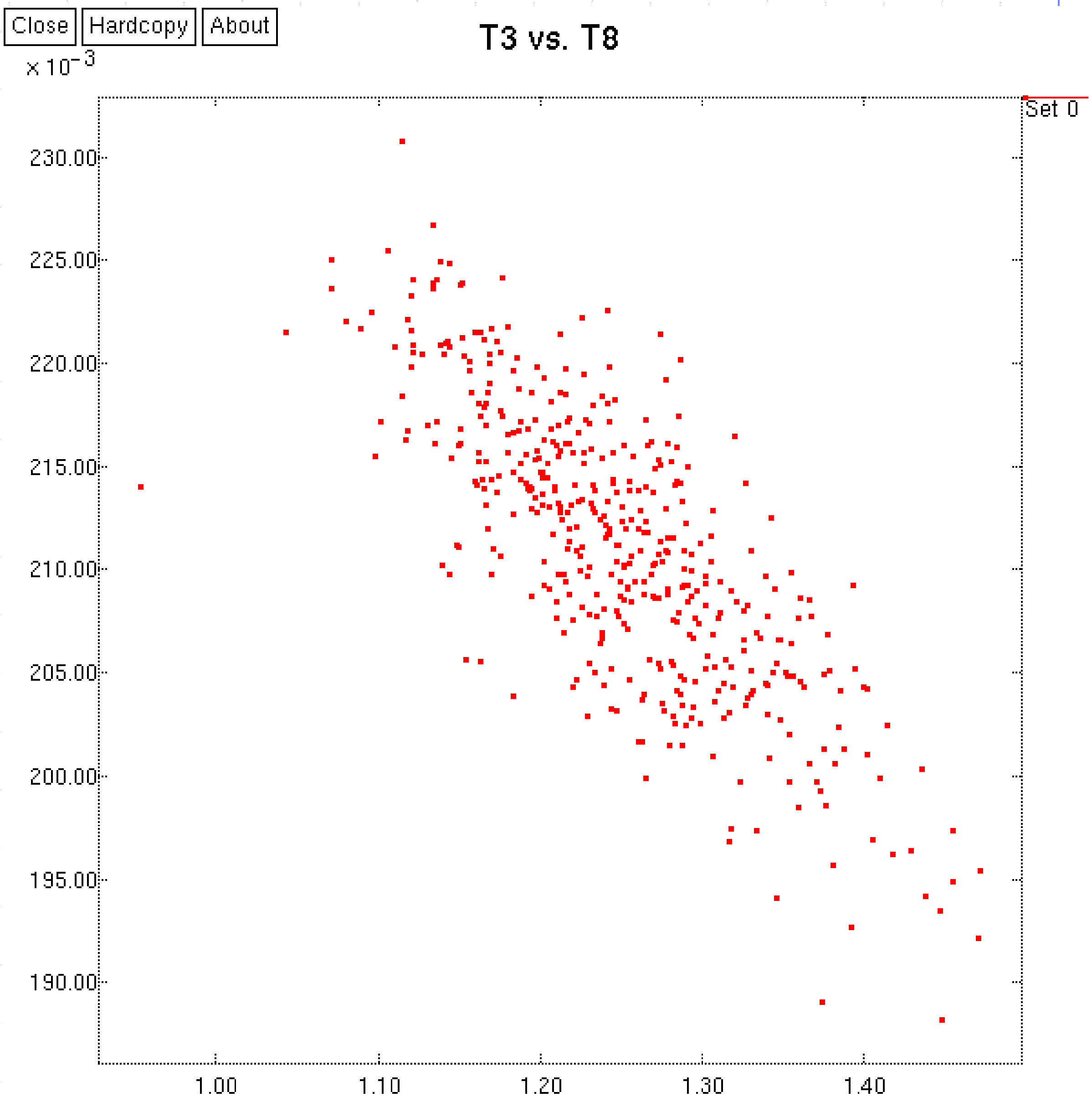
- Delays at taps 8 and 4 are *not* correlated.
- This means underlying noise sources are *independent*!





More Variations

- Delays at taps 8 and 3 are negatively correlated.
- *Reason*:
  - variations in wire resistance.
  - resistive *shielding*.



Lesson Learned

- If you include one source of variability, you should not be surprised if everything comes out correlated!
- If you include multiple sources of variability, you should be prepared to do some analysis to understand the interactions.
- No tools exist to do this work…
- Spice + R + scripts + Graphic statistics package usually enough.

Variability and Timing

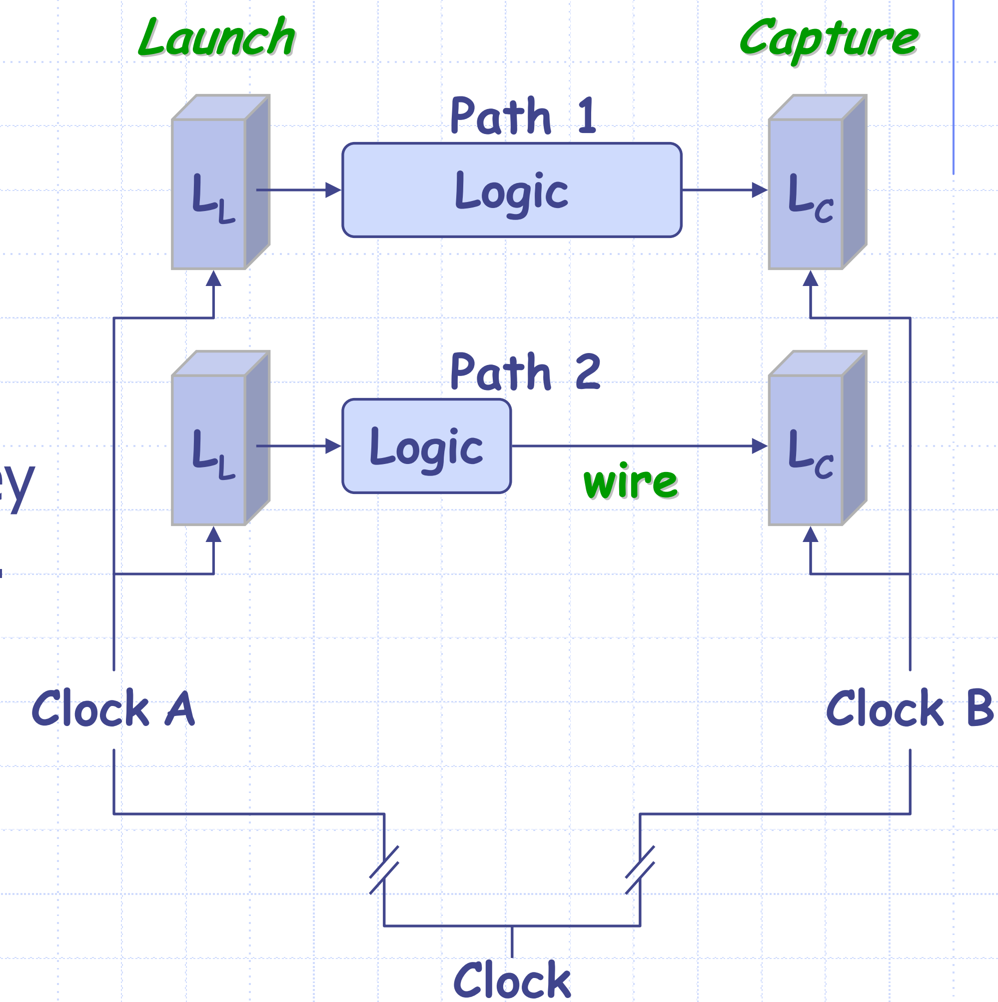
- The bulk of design is on digital synchronous systems.

- Such systems are well studied, and a formal theory of timing correctness exists.
  - Presumably covered in any VLSI design course you can take.

- Such systems represent the bulk of Si $’s, and therefore a lot of attention is paid to their performance and yield.

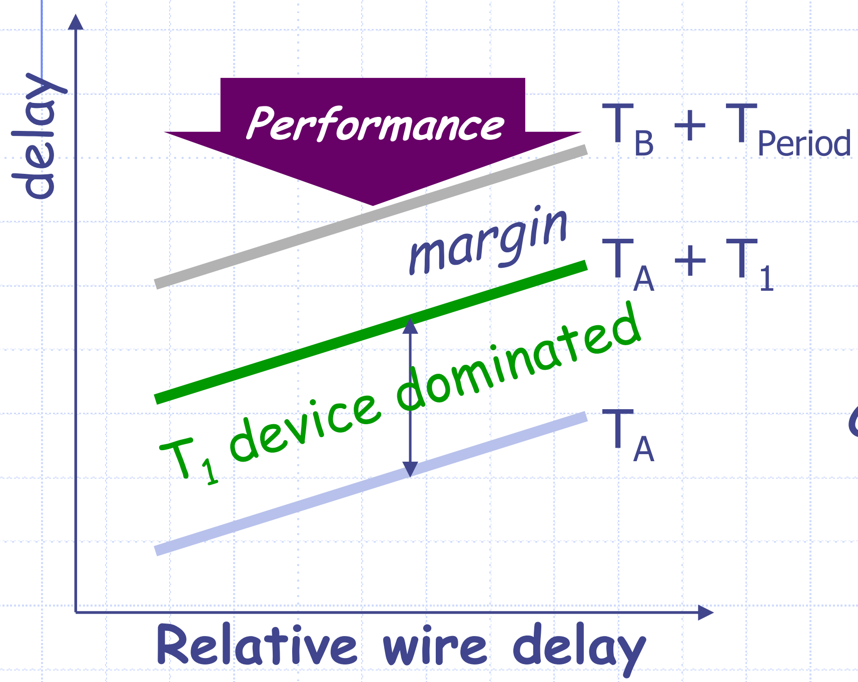
Impact of Variability on Timing

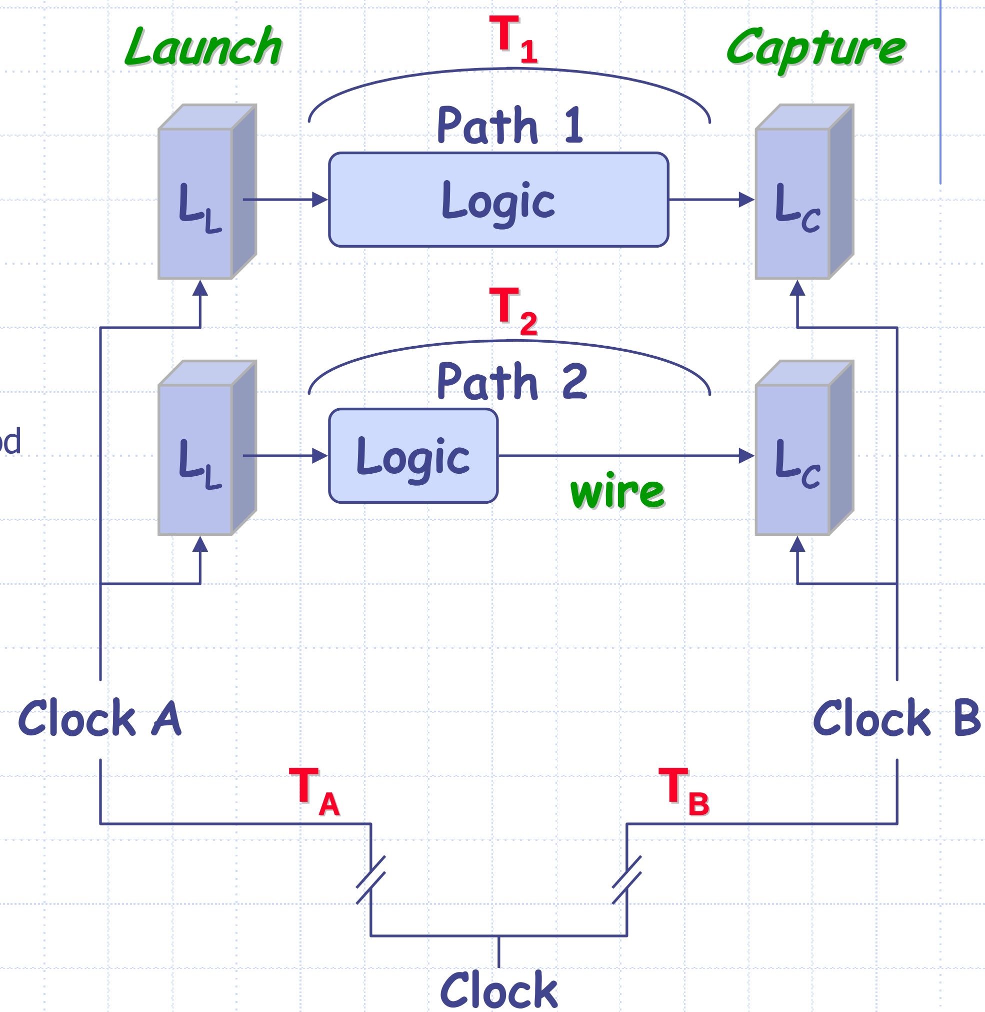
- Timing in a synchronous digital circuit:
  - Single distributed clock.
  - Logic *bounded* by clocked latches.
- **Correctness**: signals obey certain timing inequalities.
- **Performance**: clock period.
- **Robustness**: timing margin in the presence of variability.



Variability and Timing

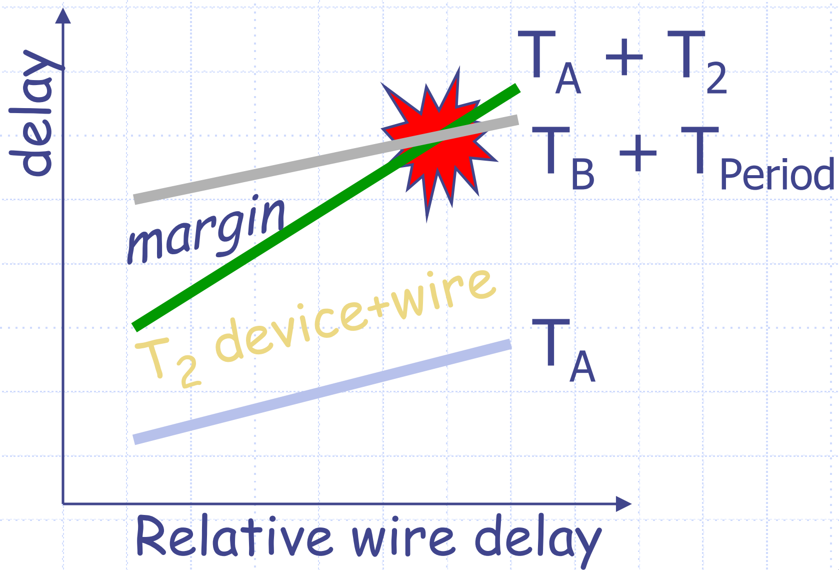
- $T_A + T_1 \leq T_B + T_{Period}$
- $T_A + T_1 \geq T_B$
- $T_A + T_2 \leq T_B + T_{Period}$

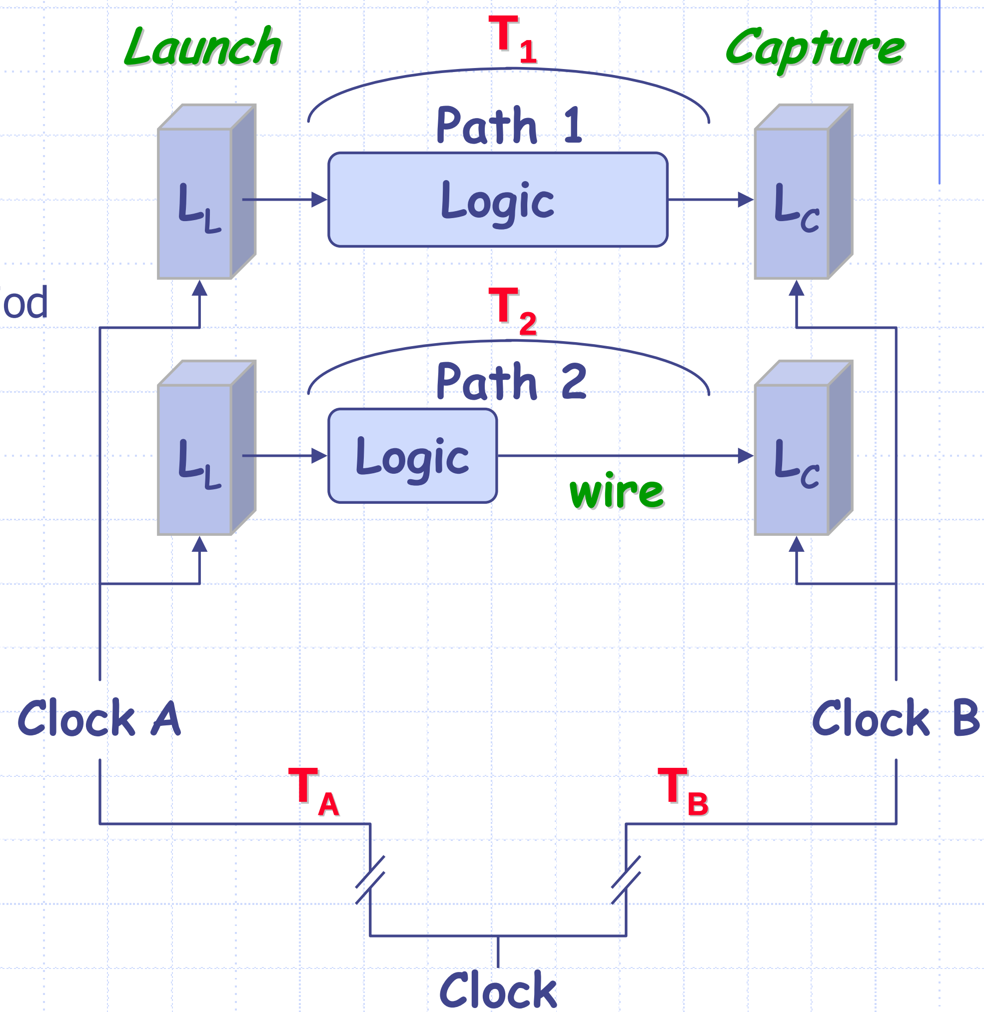




Timing Correctness

- $T_A + T_2 \leq T_B + T_{Period}$





☞ Wire & Device variability need not be correlated!

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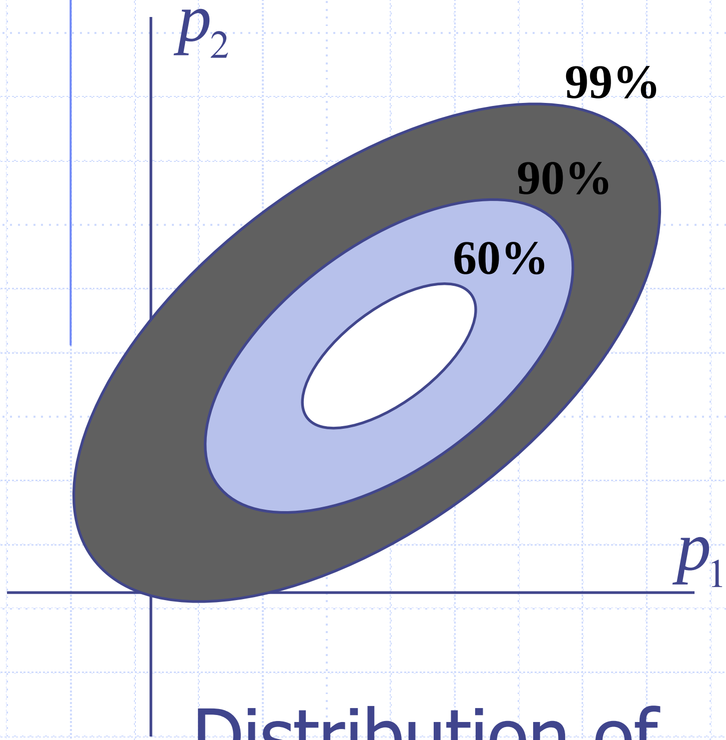
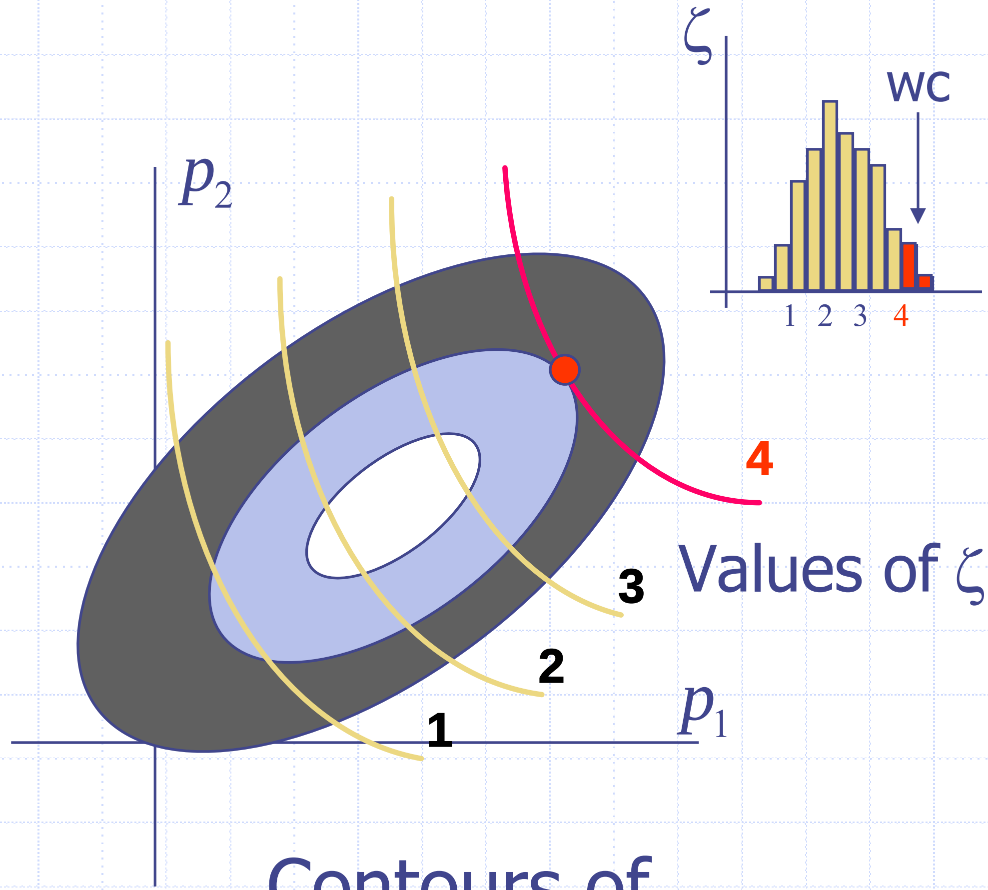
Classical Variability Analysis

- Given:
  - A design specification.
  - Target performance, ζ.
- Determine:
  - The expected $n\sigma$ spread of ζ.
    - Worst or extreme case analysis.
  - Or…
  - The distribution of ζ.
    - Yield estimation.

Statistical Performance Basics



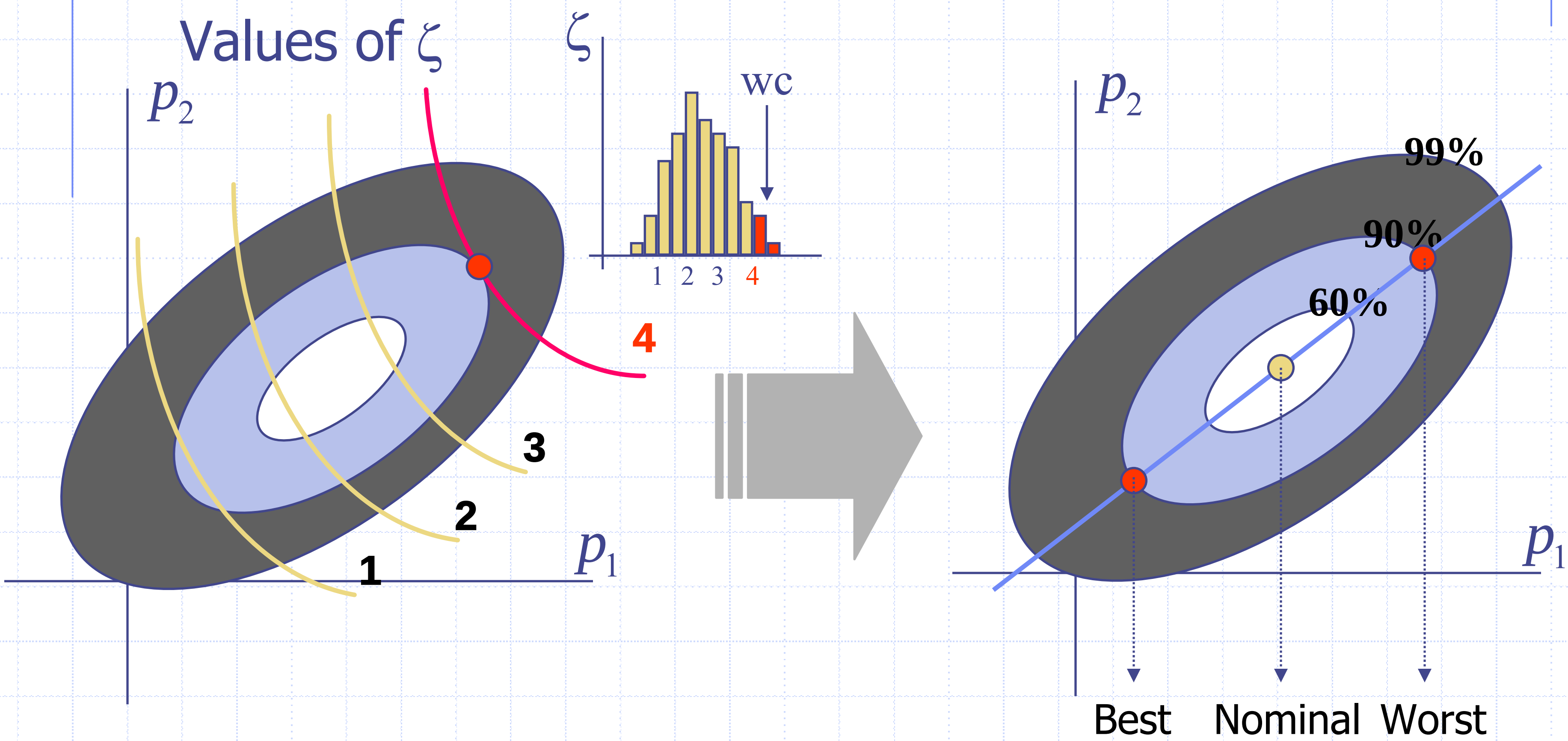
Distribution of
Model Parameters



Contours of
Performance Values

Worst Case Analysis

- Perform analysis on one or more *typical* circuits and apply resulting parameters to all circuits.

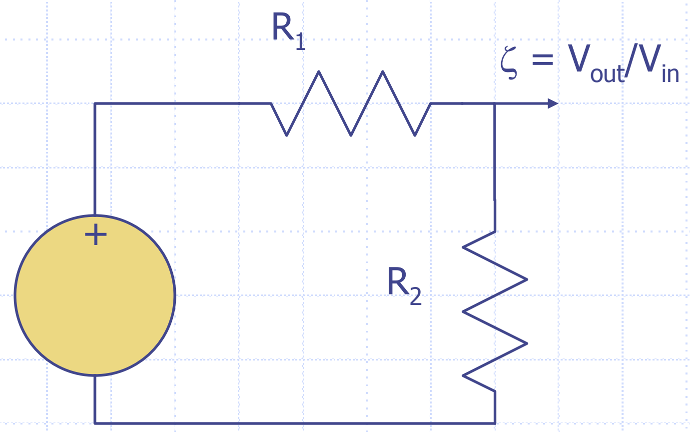


Formal Definition

- Given the distribution of parameters P, and a mapping from parameters P to performance ζ, find the setting of P, P_{WC}, which results in a value of ζ, ζ_{WC}, which bounds a specific % ω of the ζ population.
- Knowing ζ_{WC} means that we know that the probability that ζ is better than ζ_{WC} is ω!
- So if ζ_{WC} is our specification limit, then we know that the yield is bounded by ω.

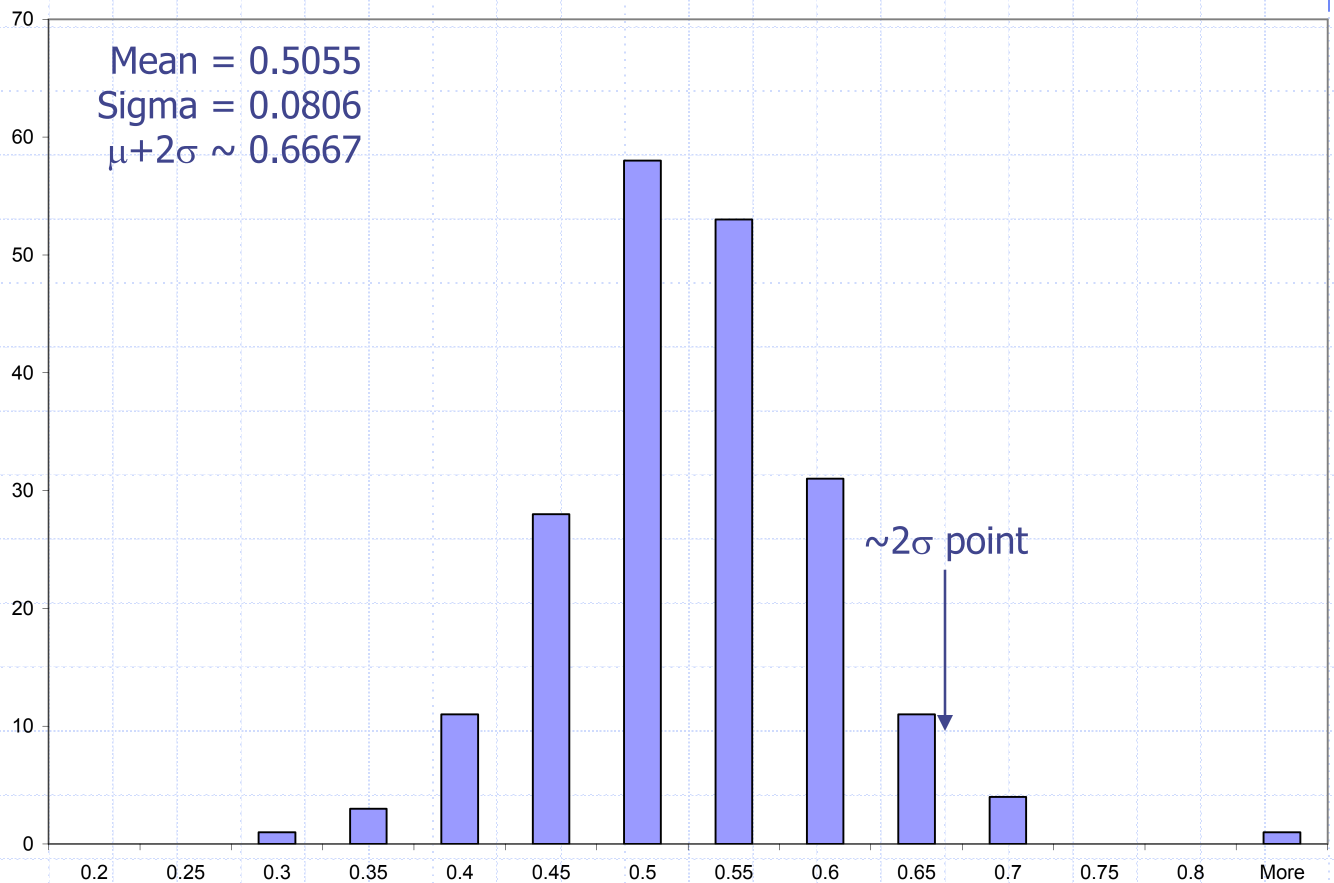
Worst Case Example

- World's simplest circuit, a voltage divider.
- Performance is value of divisor, V_{out}/V_{in}.
- $\zeta = R_2 / (R_1 + R_2)$
- Assume $R_{12} = N(5,1)$
- Assume R's are independent



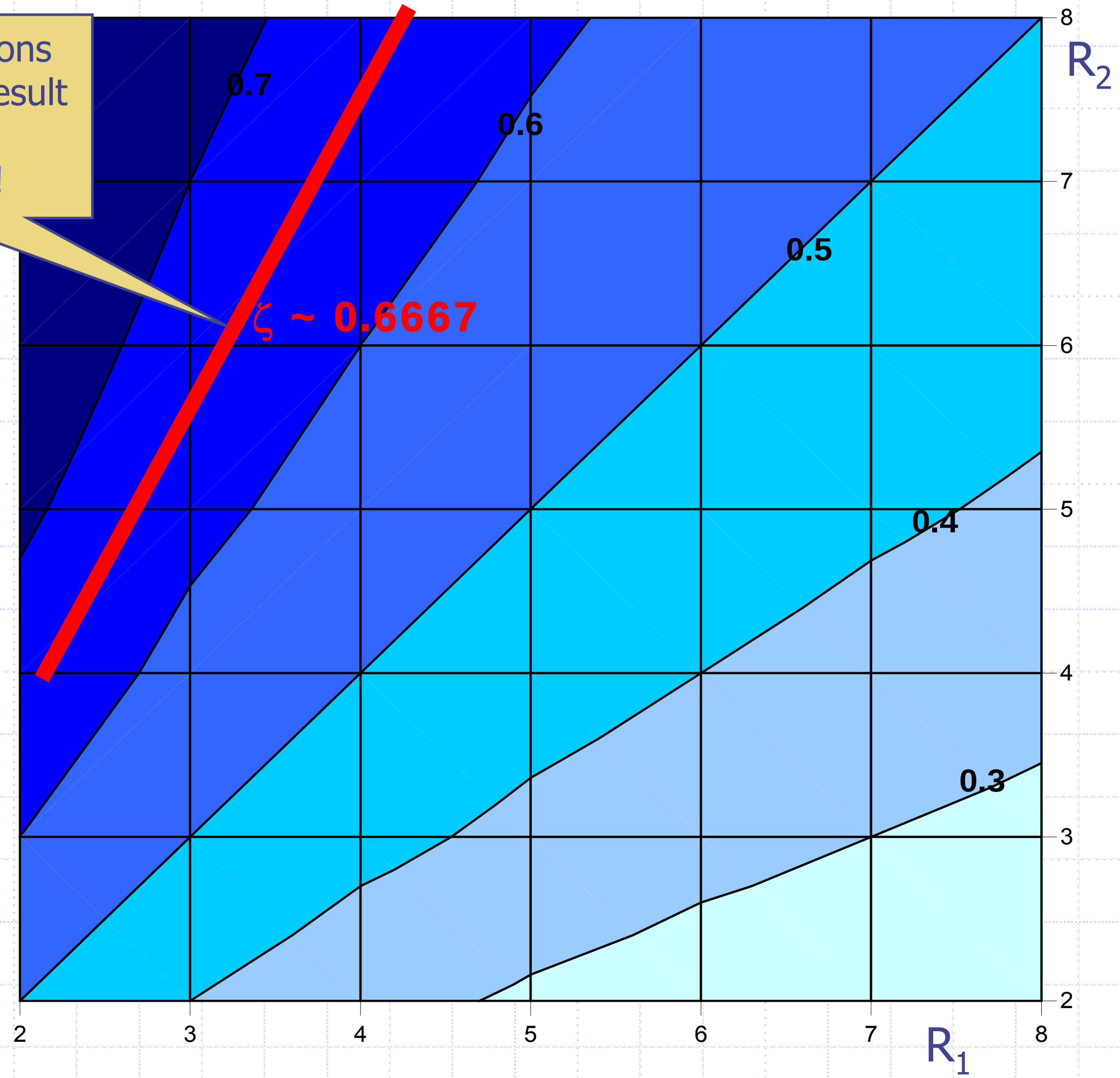
Performance Distribution

- Examine behavior of distribution of ζ.
  - Use Monte-Carlo to estimate…



Performance vs. Parameters

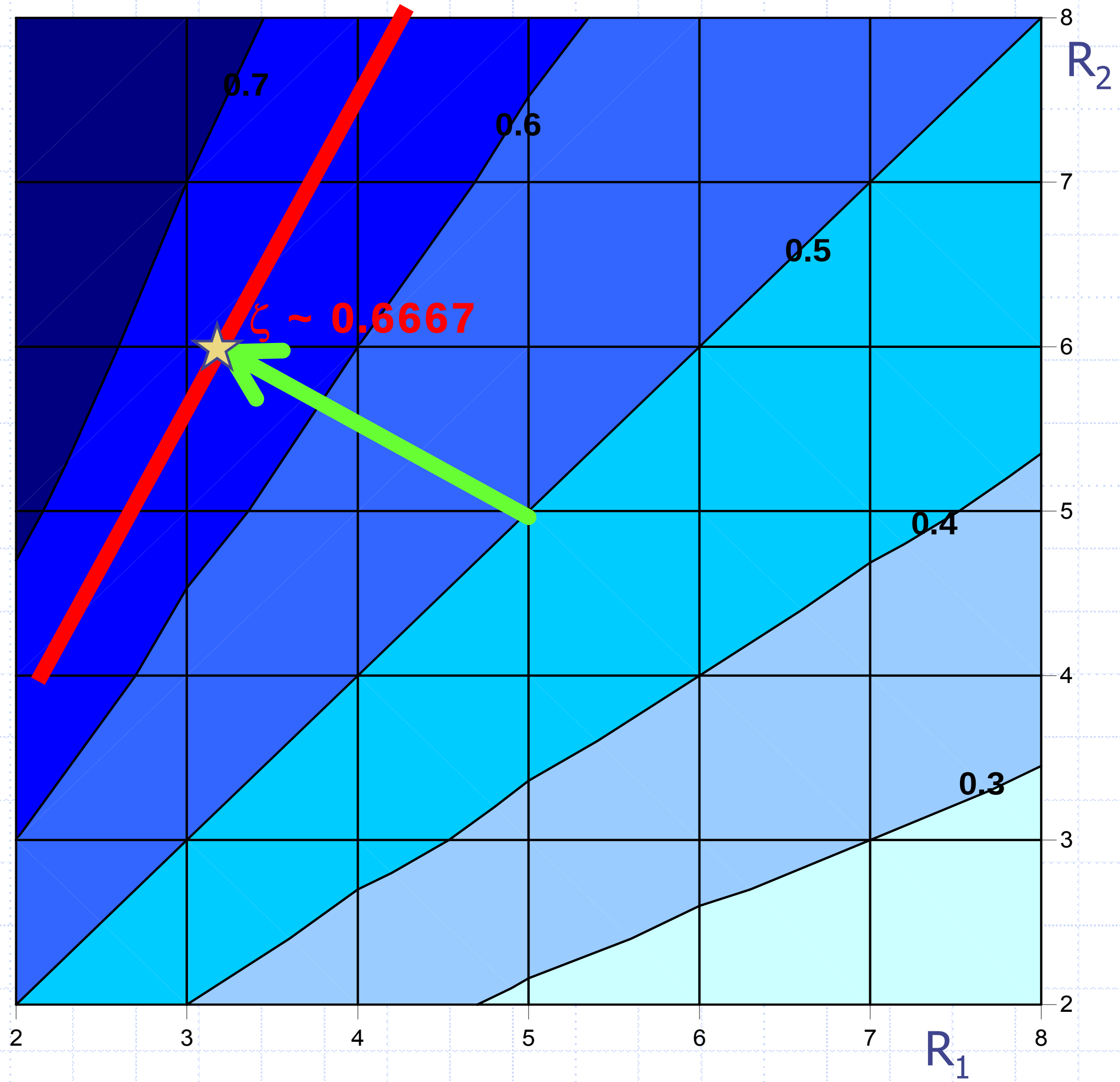
Many combinations of the resistors result in the same performance!



Worst Case Parameters

- We need an extra condition to define a unique set of worst-case parameters.
- Use the "Most Probable" set resulting in ζ_{WC}!
- For typical (Normal) distributions, most probable means closest to the center…

Worst Case Parameters



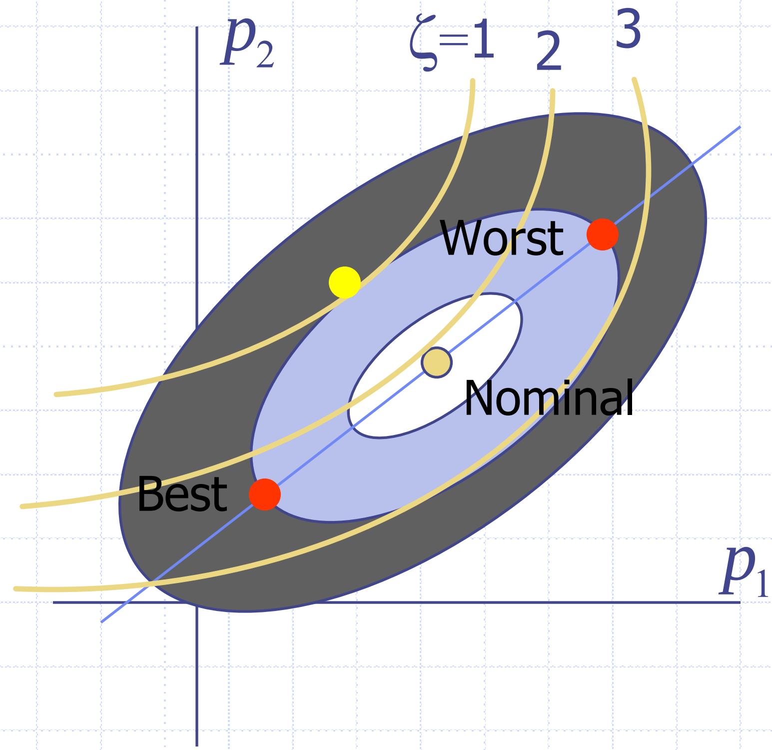
What is the Point?

- If we need to find the complete distribution of ζ in order to find the worst case, how is any less work?
- Because we use the worst case parameters to predict the extreme performance of "other" circuits!
- Example: find worst case delay of an inverter, and use it to predict the worst case of a NAND gate.

Problems with WC Analysis

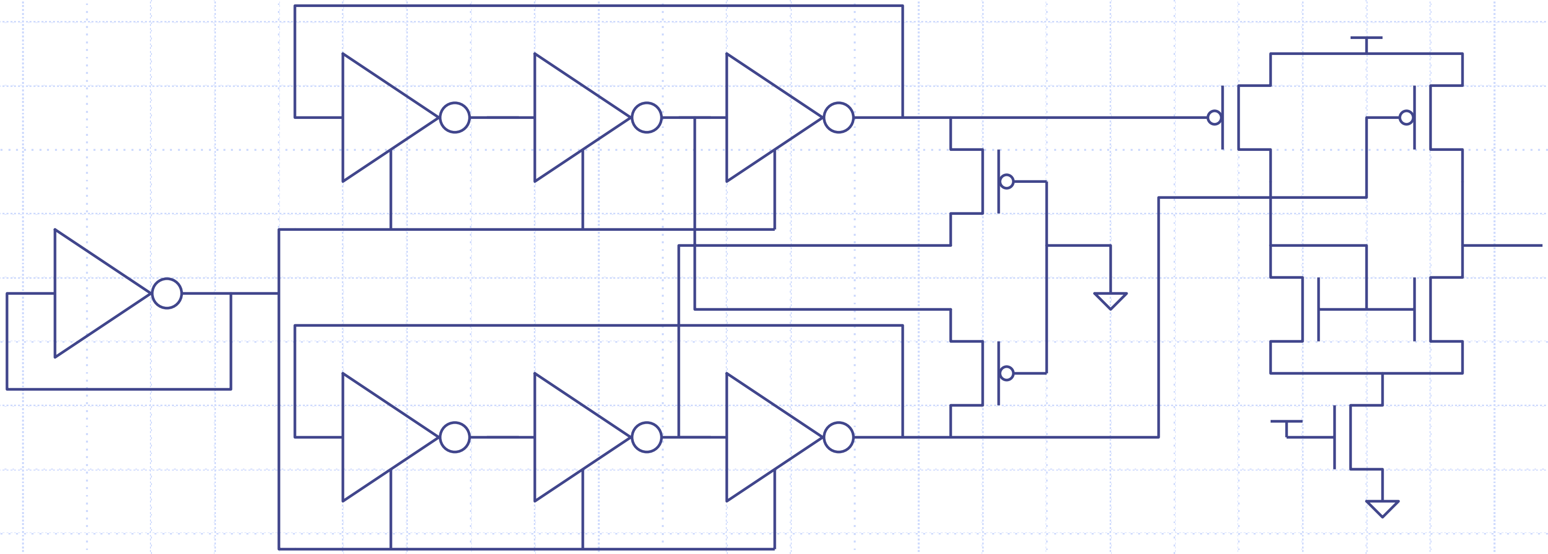
- Assumes *identical* sensitivities to parameter variations for *all* performances of *all* circuits.

- Performances which exhibit different sensitivities will produce inaccurate worst cases.

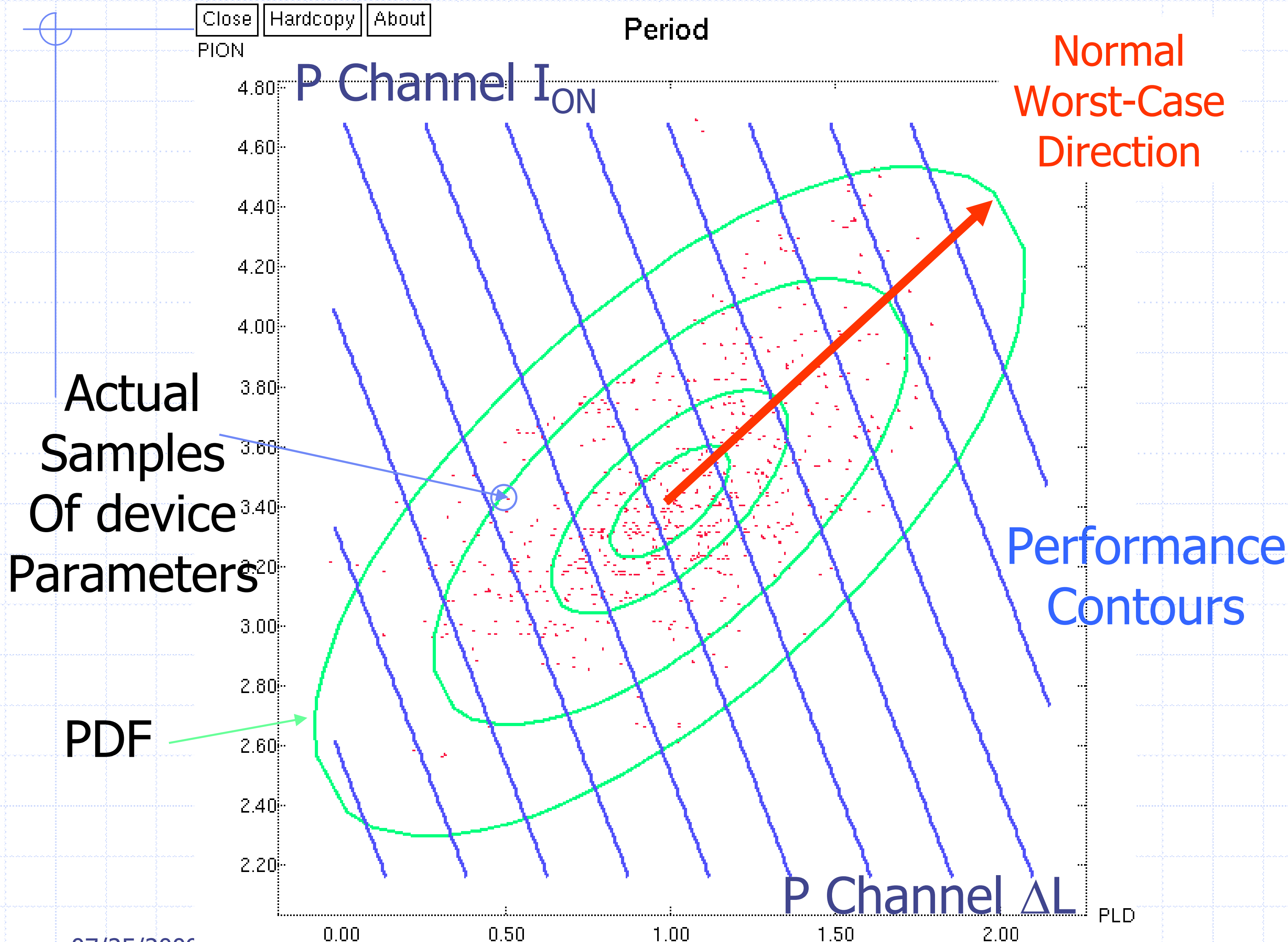


Problem Example: VCO

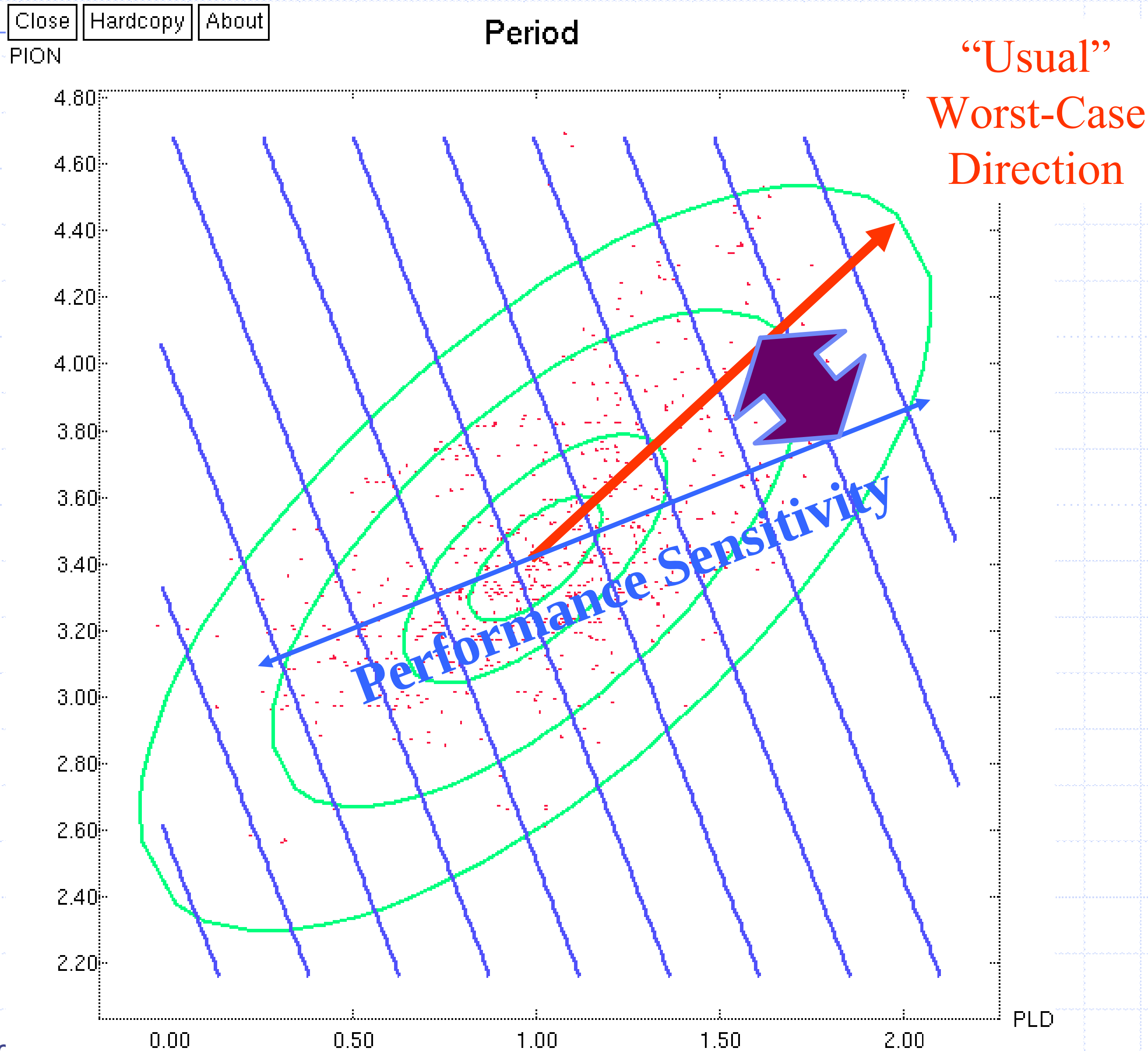
- Part of a PLL used in a PowerPC chip.
- Simulated with fixed voltage control input.



VCO Performance Statistics



VCO Performance Statistics

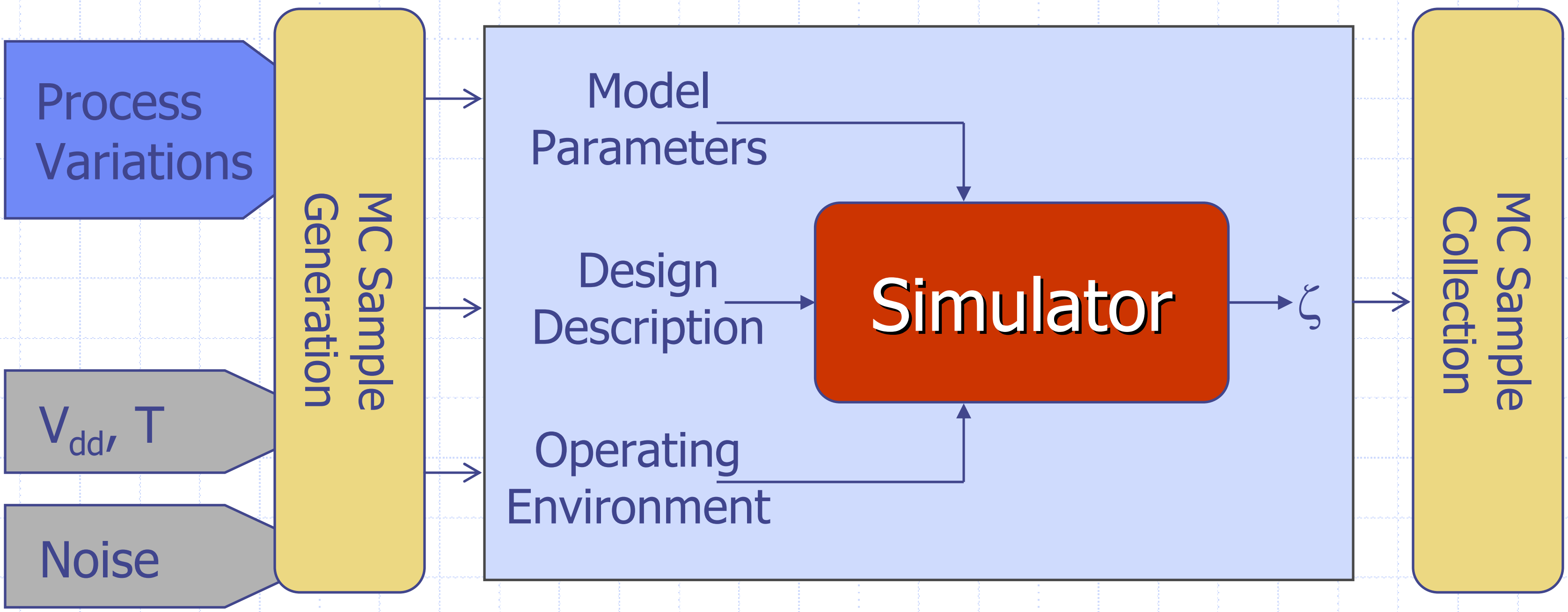


Yield Estimation

- In previous examples, we showed how we can use simple Monte-Carlo to estimate the distribution of performance.
- Given the distribution, yield (portion of distribution meeting specification) is easy to estimate.
- Can we do better?

Monte-Carlo Analysis

- Simple to use, implement, and –most importantly- understand the results of.
- Sample the parameters N times, predict the performance for each sample, estimate the performance distribution, then estimate the yield.



But, it can be Slow

- MC converges with ~ $1/N^{1/2}$
- So it can take many samples to get adequate accuracy.
  - My rule: 30 samples to estimate mean, 200 samples to estimate variance. YMMV.
  - Many more samples needed if yield is high!
- Why is this?
  - Because MC tends to have many samples around the mean, and few in the tails.

How Slow?

- Say we are estimating yield with a specification for ζ, ζ^*.

- If Prob($\zeta > \zeta^*$) is large, MC does well.
  - Since many samples will satisfy the criteria.

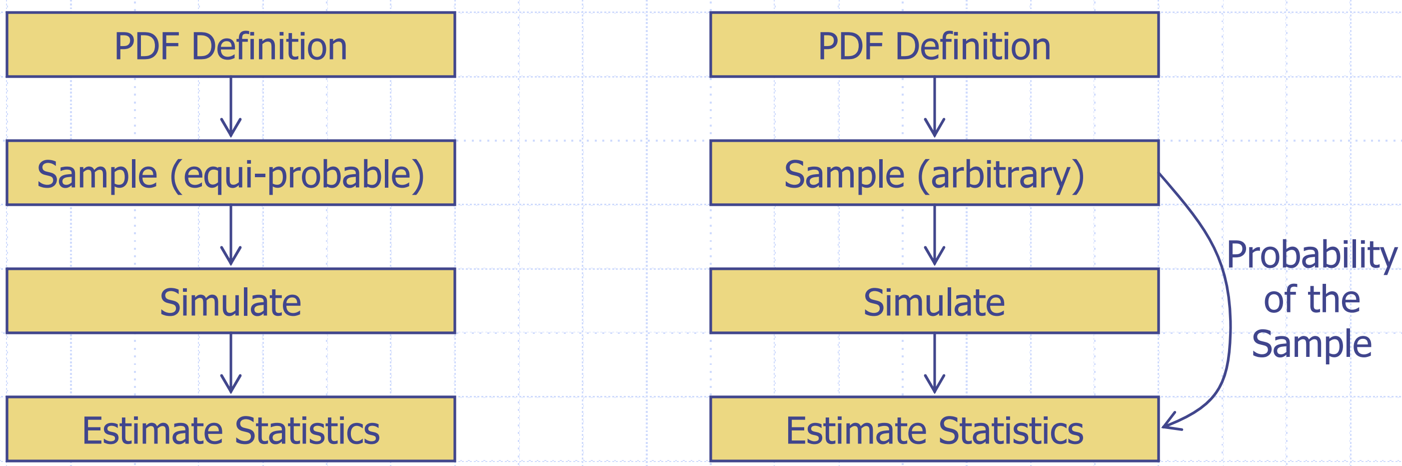
- If Prob($\zeta > \zeta^*$) is very small, MC does not do so well.
  - Too few samples fail, so resulting statistics will have a large error bound.

What can be done?

- We can attack this from two fronts:
- Make the samples better, or…
- Make the estimation of ζ faster.

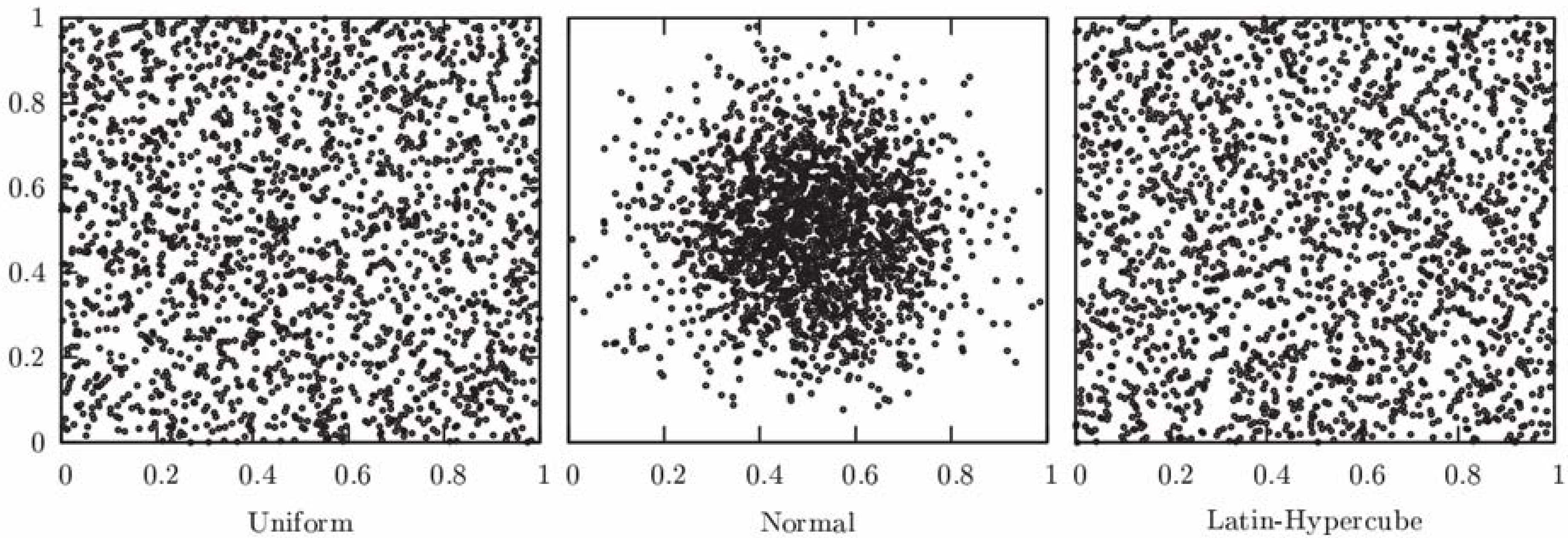
Better Sampling

- Since MC wastes a bunch of time sampling near the mean, a better sampling plan can provide us better accuracy.



Example Sampling Plans

- Alternative sample generation schemes can "explore the space" better than others.
  - Take a statistics course and learn about this!



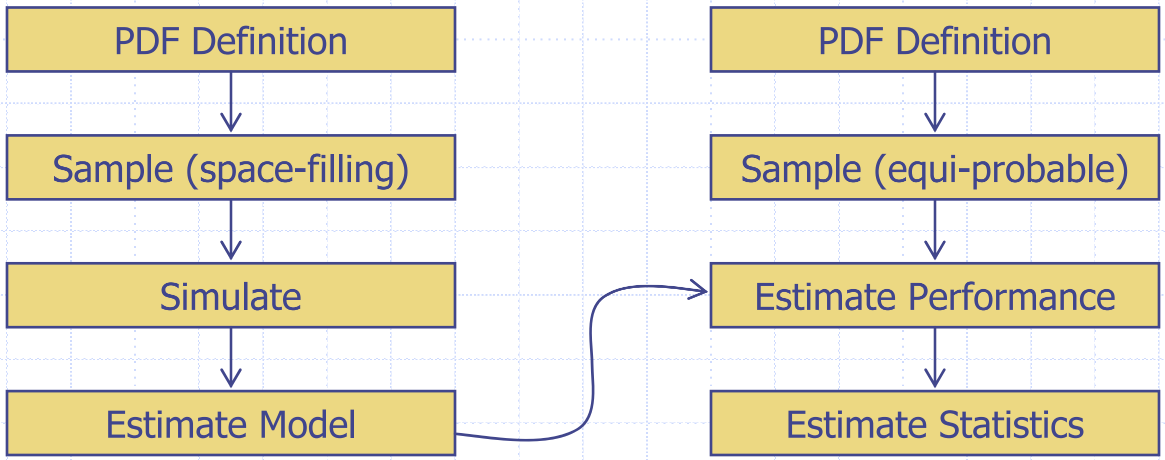
Response-Surface Modeling

- Tries to speed up MC in a different way.
  - Since simulation is slow, substitute the simulator with some type of approximation.

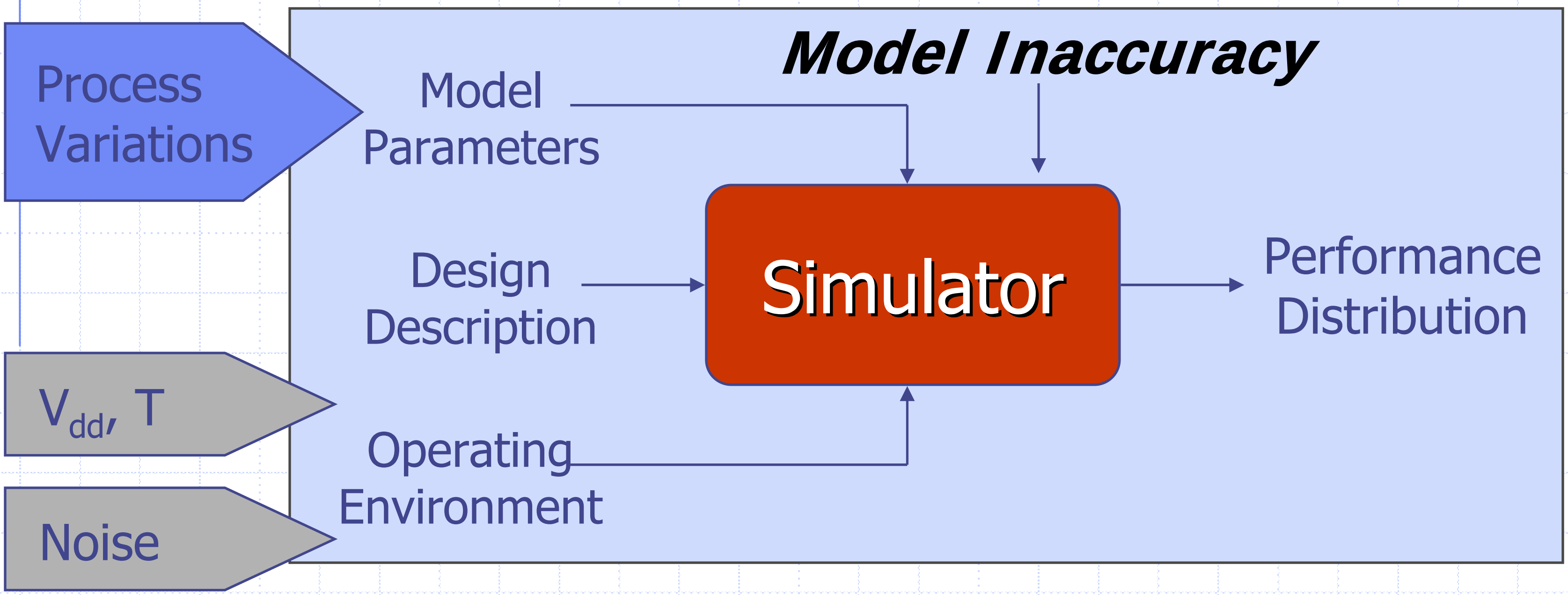
- Approximation can be a simpler model, or can be based on techniques like regression.
  - Given input x and output y, and a proposed model y = f(x, p), identify p to best fit the observations.
  - Recall "parameter extraction" has the same form!
  - But here, f() is not a physics-based model. Often it is a simple polynomial.

RSM Implementation

- Use same infrastructure to that of normal MC.
- RSM can be as simple as linear regression, and as complex as multivariate splines…
  - Take a statistics course and find out more.



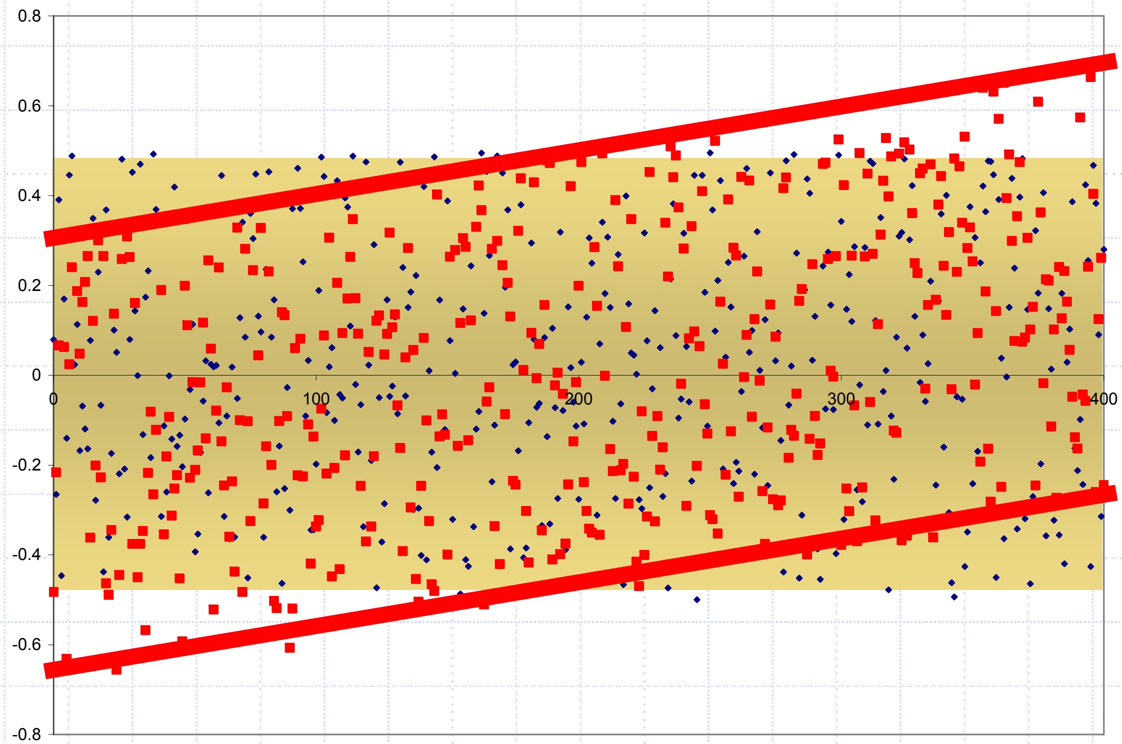
Simulation Error and Variability!



- Model inaccuracy need not be correlated with, and *cannot be distinguished* from variability.

What does this Mean?

- If you are using some type of response surface model, you need to be aware of the "error structure".



Analysis of Within-Chip Variability

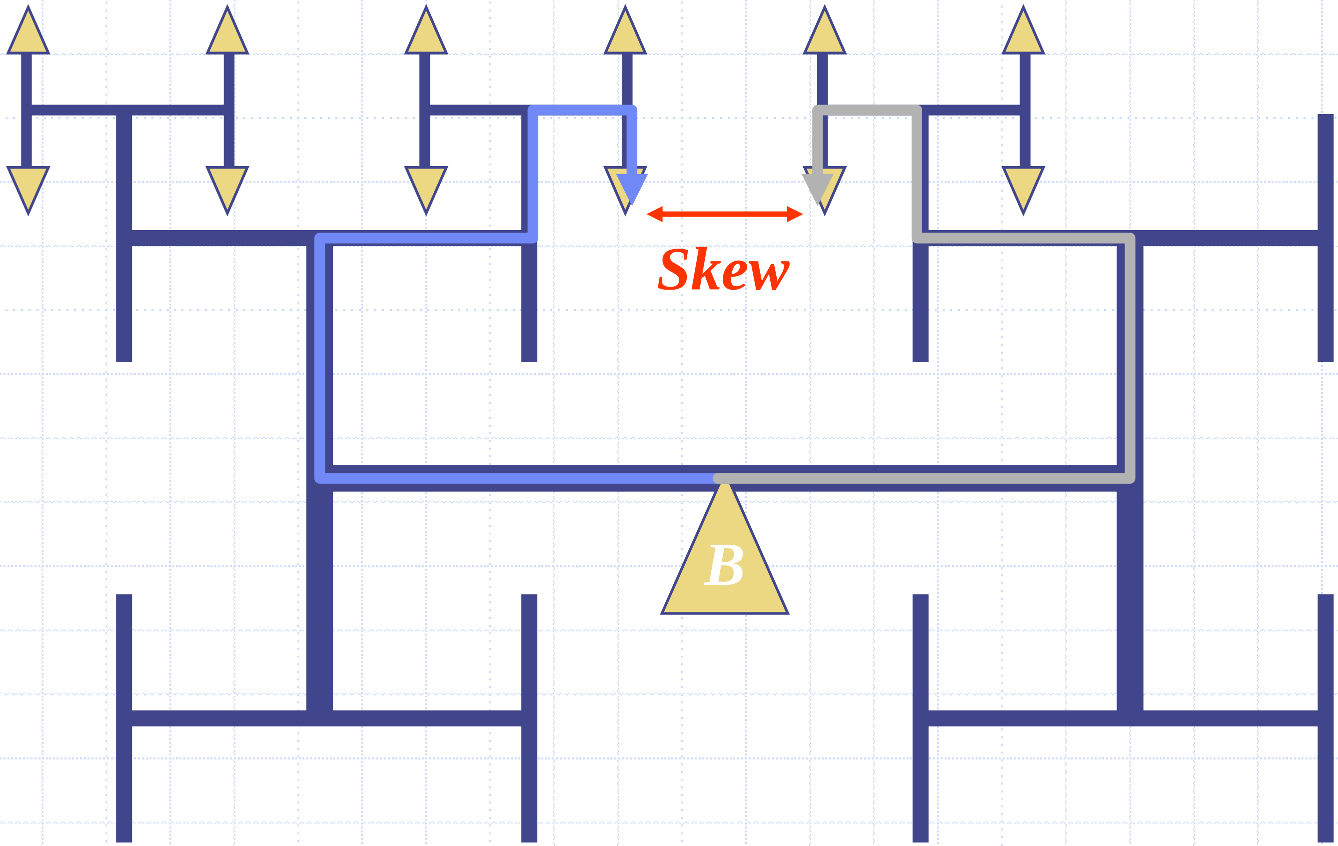
- After physical design (layout):
  - We can apply models for systematic spatial variations.
  - $P(x,y) = W(\omega,x,y) + N(0,\sigma^2)$
    - ω are the parameters of the spatial variation model.
    - Example: wire capacitance as a function of inter-dielectric thickness variations due to Chemical-Mechanical Polishing density dependence.
  - Then perform worst case analysis with respect to ω.

- Before physical design (or… *model not available*):
  - Spatial dependence not available.
  - $P(x,y) = N(\mu,\sigma^2)$
  - Max/Minimize performance subject to maintaining statistics.

  - This is the common case!

Within-Chip Worst Case Analysis

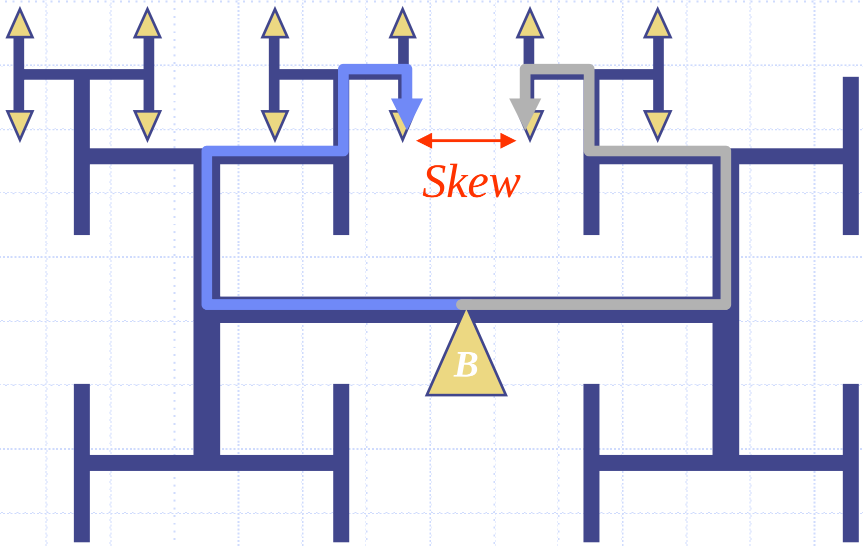
- Example: Skew in clock distribution network.



L_{EFF} Variations

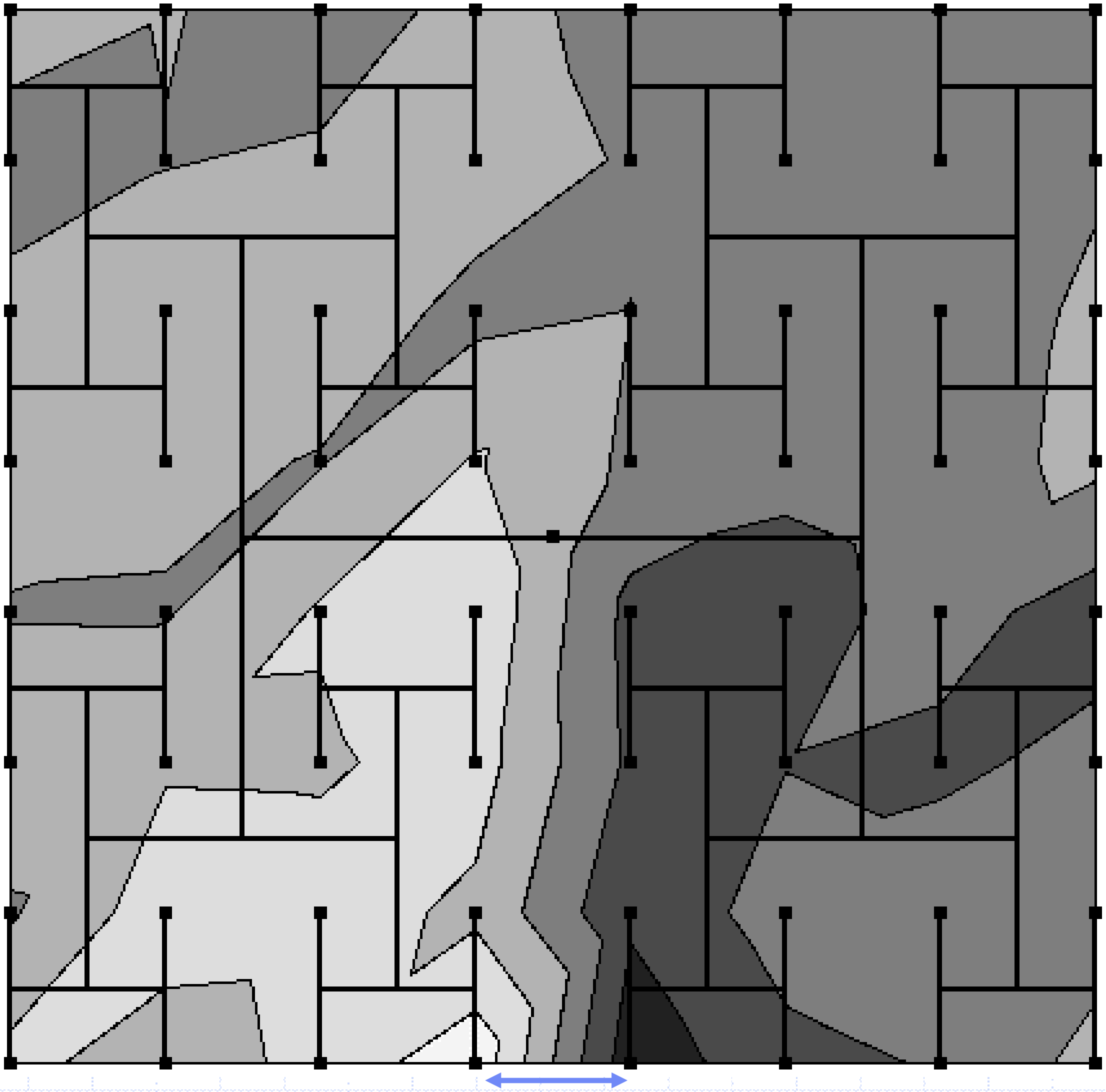
- Impact of Poly-Silicon mask, lithography and etch at the chip level.
- Each buffer (total of 65) has unique L_{EFF}.
- Values of L_{EFF} obey a normal distribution.

min Skew(L_{EFF})
s.t. mean(L_{EFF}) = μ
and stdv(L_{EFF}) = σ



Results for L_{EFF}

- Dark: short.
- Skew insensitive to top half of H-Tree.
- Sensitivity increases closer to the *leaves* of the H-Tree.
- Non-statistical worst case is 23% more pessimistic.
  - Change L_{EFF} by $\pm 3\sigma$ depending on sign of sensitivity.



Analysis for Variability: Perspective

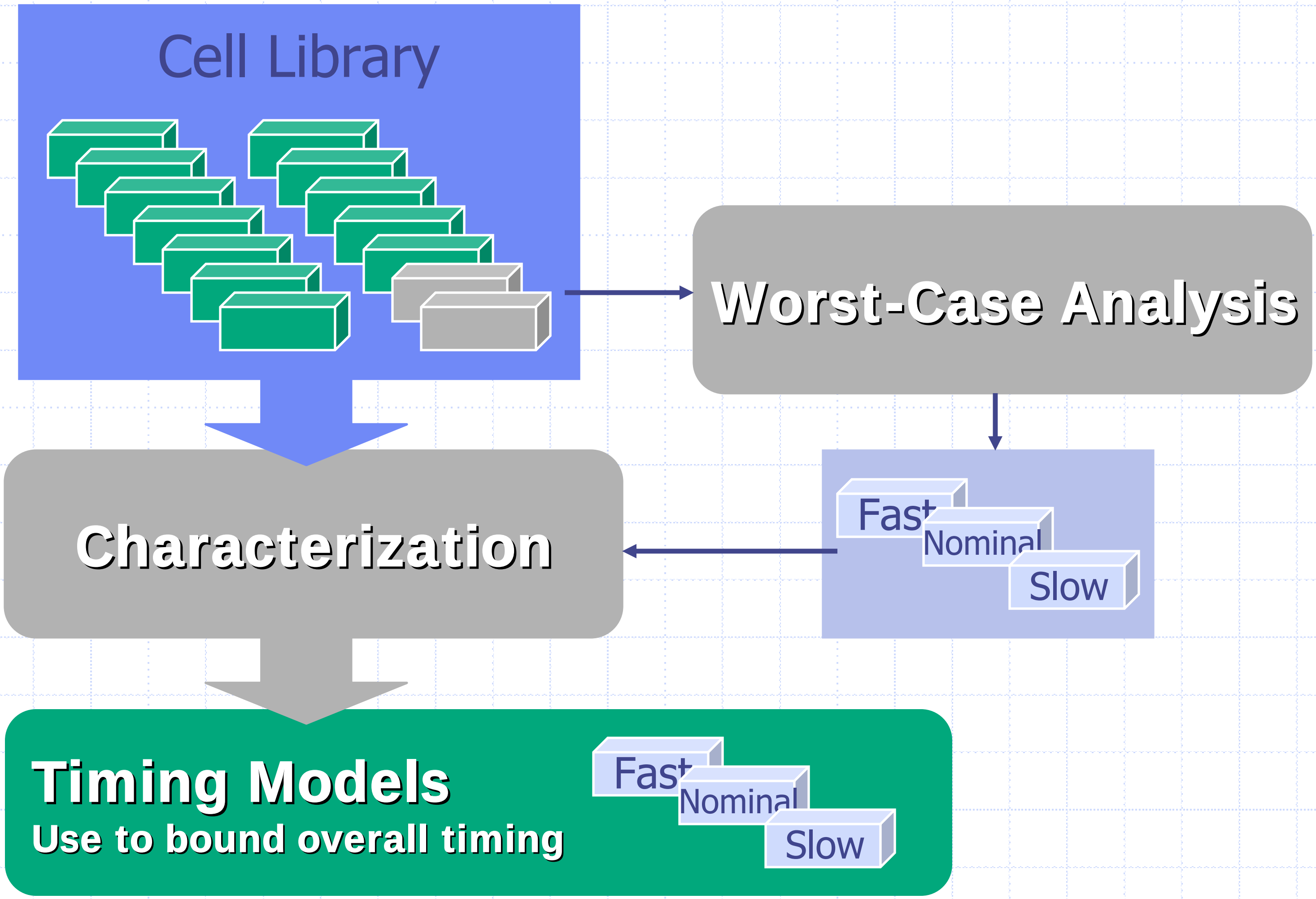
- Existing analysis methodologies rely on detailed device models and expensive circuit simulation.
- But… capacity constraints limit the size of analyzable designs.
- Answer: Static Timing Analysis (STA).
  - Reality is that STA is often the only viable sign-off tool.

STA for Variability

- Much recent work in academia and industry…
  - Emphasis has been on algorithms, less on models.

- Proposed some time back as a solution to the simulation time/capacity problem.
  - It is not possible to "spice" a whole design.
  - STA is the tool of choice for timing closure on digital designs.
  - Infrastructure exists to couple STA to "corner" models.

Variability Analysis using STA



STA for Variability

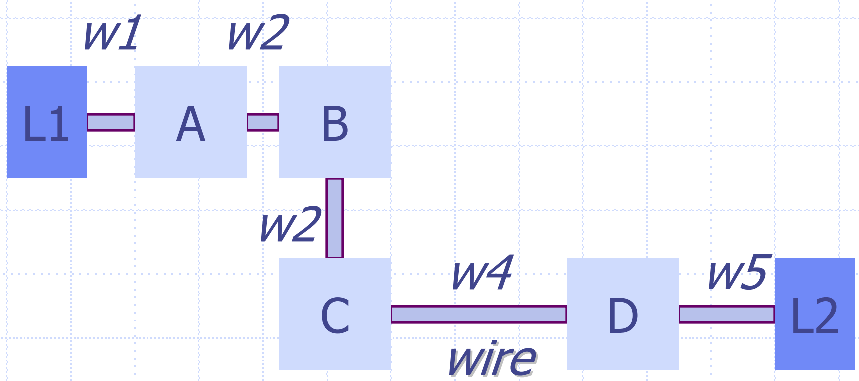
Given:

- Results of performing static timing analysis.
  - Detailed delay breakdown (cell/wire) for critical paths.
- *Derating* coefficients for cell and wire delay for each source of variation.

Estimate:

- Parametric (circuit-limited) yield.
  - Delay variability for each path.
- Probability of failure for each path.
- Performance (e.g. clock period) statistics.

Derating Coefficients...



Slack Report:
Path N:

#	cell	arrival	delay	wire	*d/DL*	*d/Vt*	*d/RC*
	L1	0	120p	20p	400	133	10
	A	140p	80p	20p	200	67	10
	B	240p	230p	35p	575	190	18
	C	505p	175p	125p	438	146	63
	D	805p	200p	80p	500	165	40
	L2	1085p					

From Sensitivity to Variability

- Aggregated path delay component sensitivities allow us to express total path delay as:
  - delay = $D_0 (1 + D_1\Delta L + D_2V_T + D_3RC \ldots)$
  - *Linearized model of delay for a specific path.*
- Given the statistics of ΔL, V_T, RC, we compute the distribution of delay:
  - delay = $N(D_0, (D_1\sigma_{\Delta L}^2 + D_2\sigma_{VT}^2 + D_3\sigma_{RC}^2 \ldots)^{1/2})$
  - Can be done because of the linearity assumption.
- Delay *bounds* lead to failure probability:
  - P_{fail} = Prob(delay > d_{MAX})

- But… Ignores correlations!

More Recent Work

- Much effort has been invested in moving from path-based to block-based SSTA.

- Not enough effort in:
  - Modeling of variability for SSTA (due mostly to lack of data).
  - Modeling the inaccuracy of STA and how it impacts the resulting statistics.

Outline

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- A Taxonomy of Variability
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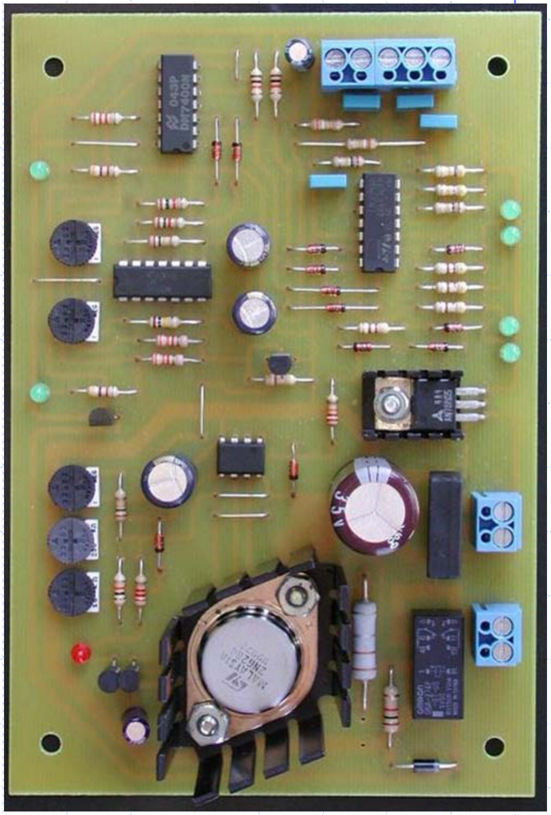
- Impact on Circuit Operation
- Variability Analysis
- Yield Optimization/Improvement
- DFM Trends and Outlook

- Homework Assignment

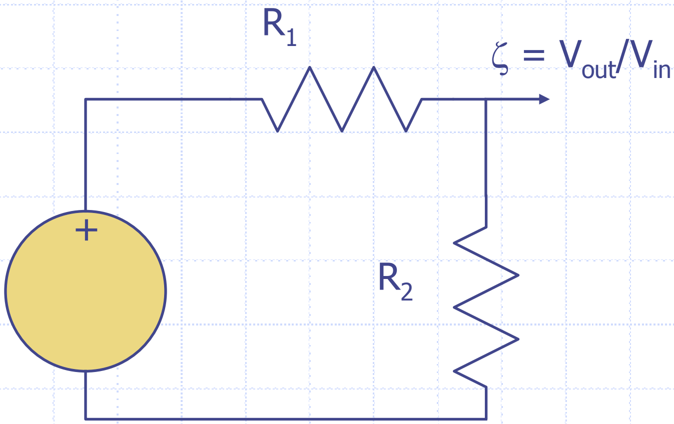
Yield Optimization/Improvement

- This is an "old" problem…
- Back in the days of discrete circuits, designers had to deal with component "tolerances".
  - A resistor would be ±10%.
  - An expensive resistor might be ±1%.
  - So using the cheapest components was important to profitability.
- Tolerance Design is the area in which this work was done.

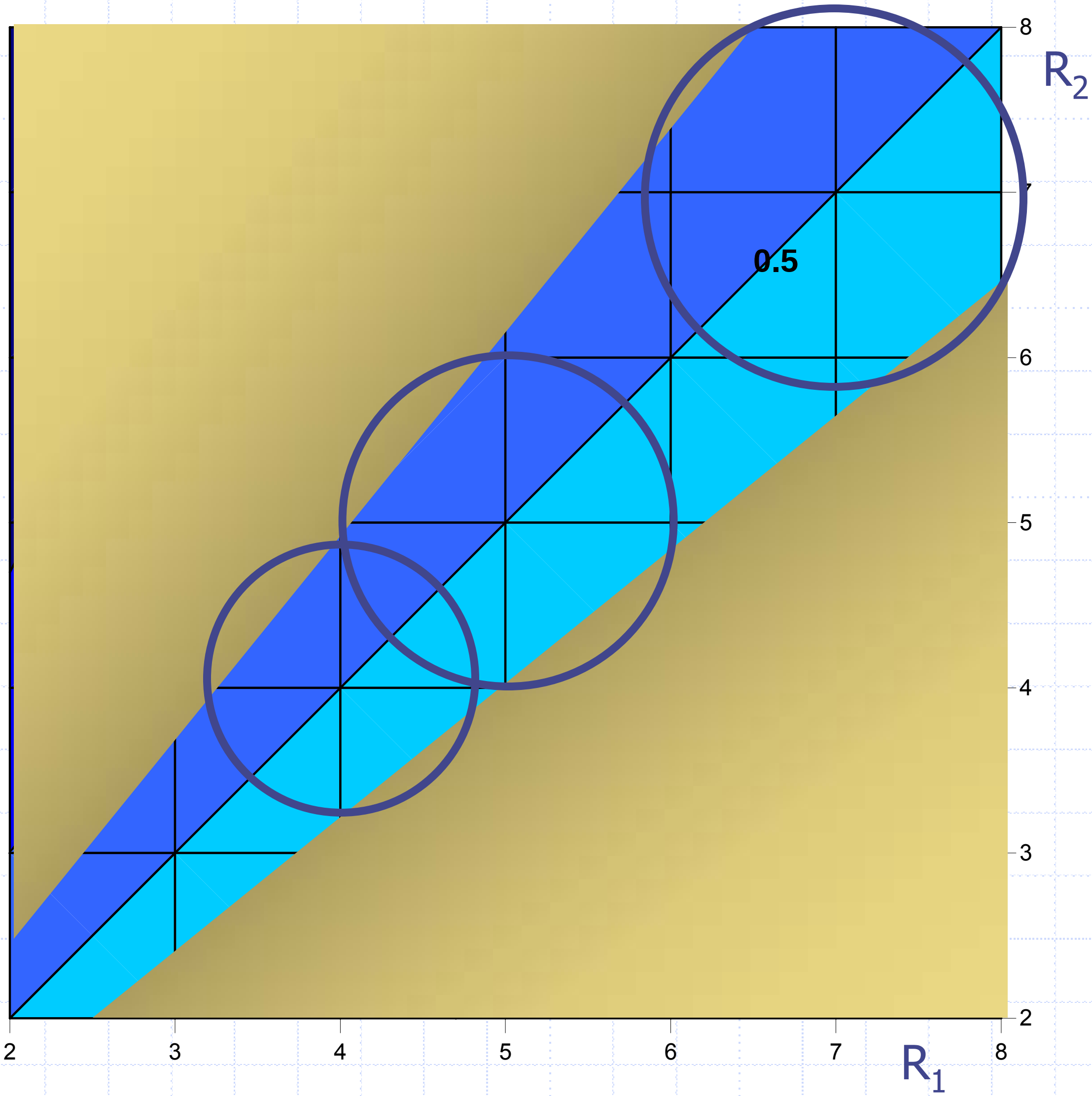


Design Centering

- Adjust nominal value of parameters to maximize number of working circuits.
- Example using our voltage divider:
  - Assume resistors have a 20% tolerance.
  - Assume we want ζ to have a 10% tolerance.
  - What is the best value of R_1 and R_2?
  - To make it more interesting, what are the best values that also minimize power?



Graphical Solution



Yield Optimization

- A number of academic papers exist on various forms of direct yield maximization.
- More work on analog than on digital.
  - Analog designers frequently make empirical models which make this work easier.
  - Analog design tends to be more sensitive to process variations.
- None appear to have "caught on".
  - Few CAD tools.
  - Spice + Matlab etc…

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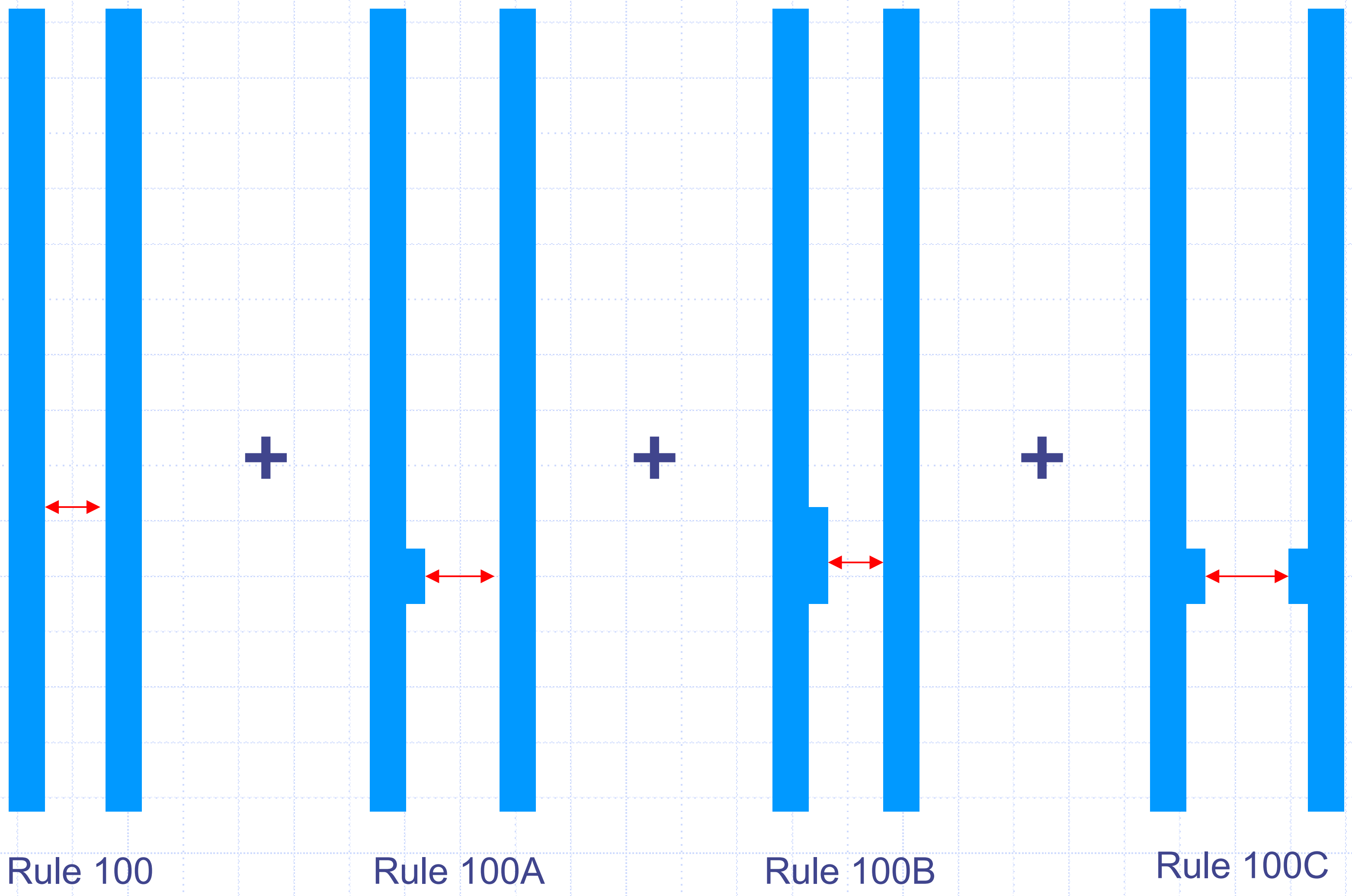
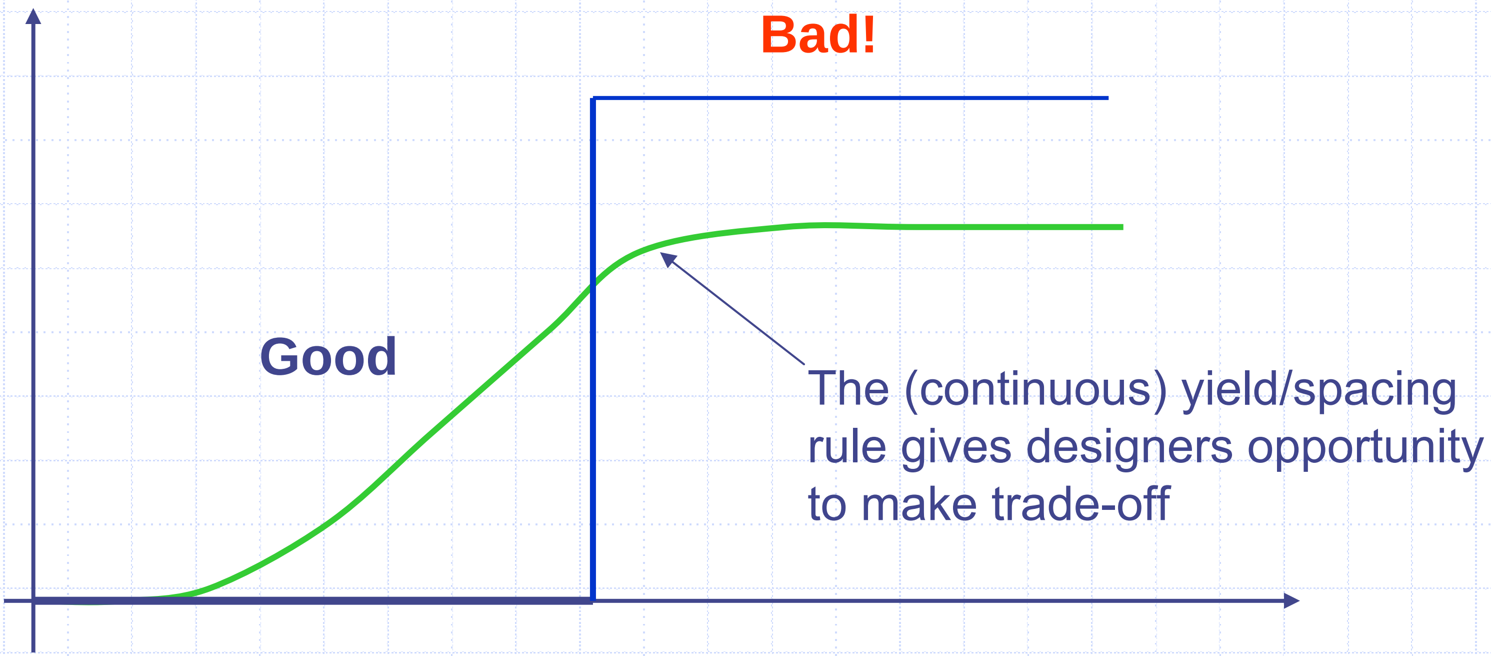
CAD/DFM Problems and Issues

- Inadequate information flow between design and manufacturing activities.
  - Example from IBM:
    - Chip design methodology document 10cm thick.
    - Technology description document 1cm thick.
- Limited facilities in design tools for the representation of the process.
  - Process often abstracted to **rules** which are not capable of generating design *improvement*, just design *correctness*!
  - This is doubly true of process variability!

Reactive Nature of Design Rules



"Hard" Rules?



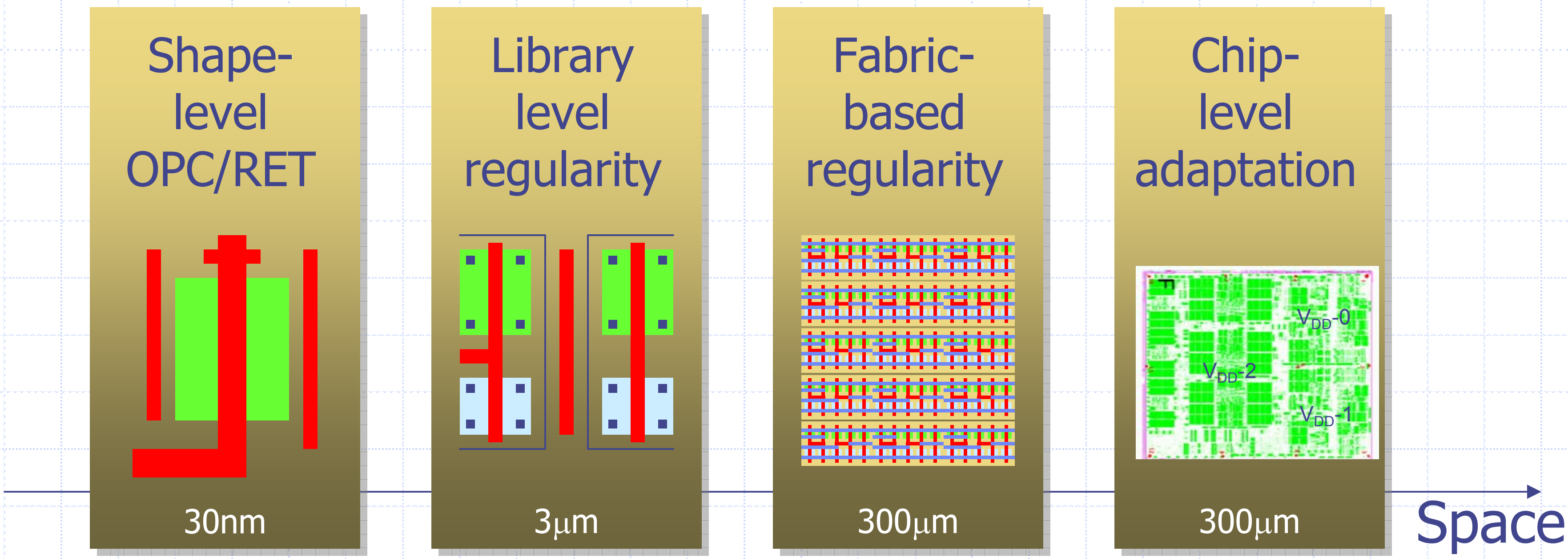
- The step-function like design rules are rigid. Unable to provide designers density/robustness trade-off
- A coherent and comprehensive representation for complex structures is hard

CAD/DFM Opportunities

- It is known that the interaction between design and implementation is increasing.
  - How you build has as much impact as how you designed it.
  - Sizing a schematic no longer guarantees a working design.
- New design methodologies are going to be needed.
  - General push for "regularity" (e.g., Restricted Design Rules)
  - Need to balance the regularity and area/performance penalty

Response to Variability

- Responses to variability target different "spatial frequencies".
  - No one response is sufficient to tackle the full impact, but all responses require accurate estimates of magnitude and impact.



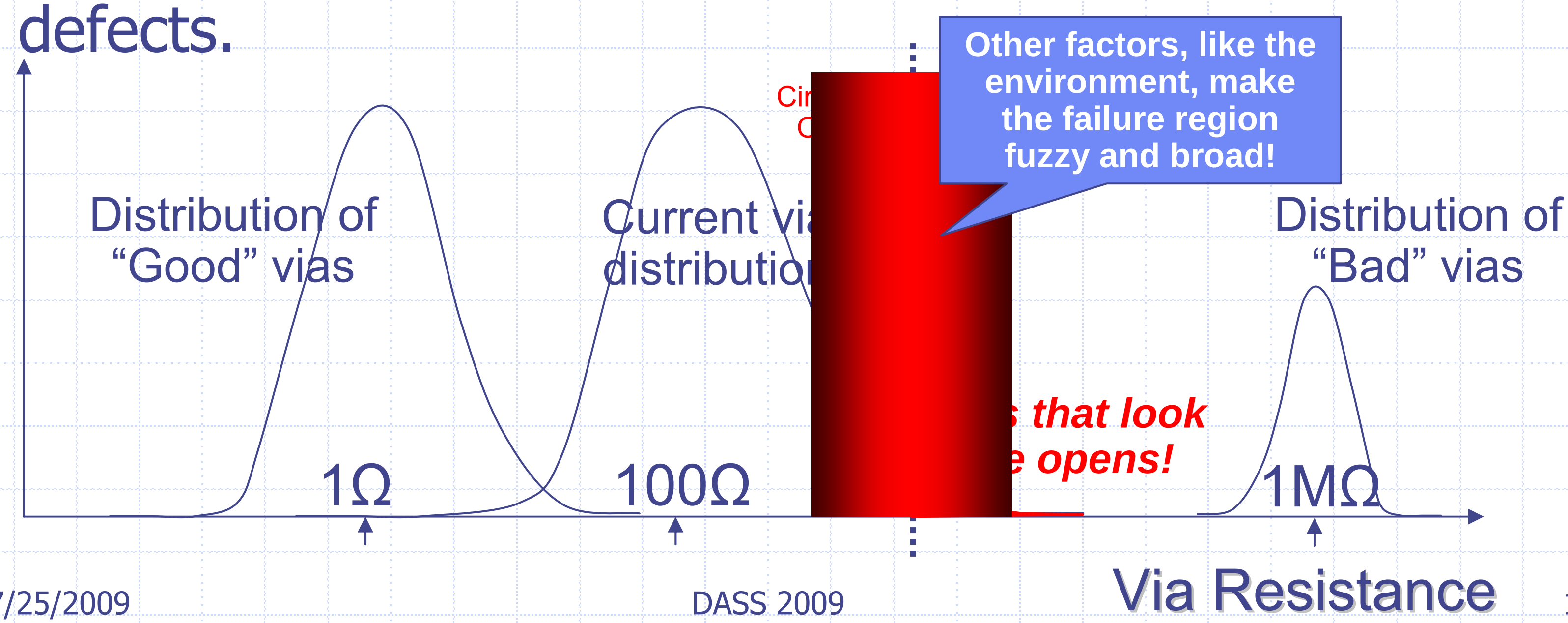
Linking Variability & Resilience

- Much current work is focused on the immediate and short term impact of variability.
  - Examples: statistical timing analysis, new approaches for function-based OPC etc…

- But increasing variability will change the character of the impact it has on circuits.

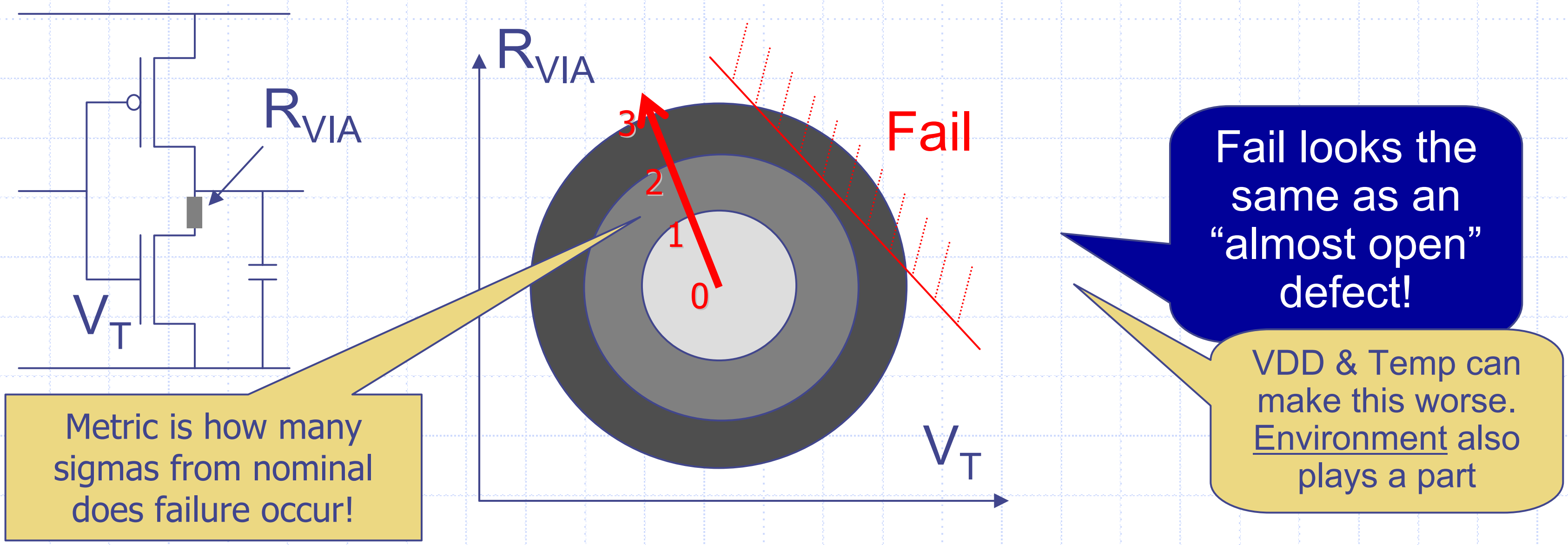
What changes with increased variability?

- Circuits can become permanently or intermittently defective.
- Failure dependence on operating environment makes test coverage very difficult to achieve.
- This can be viewed as the merger of failure modes due to structural (topological), and parametric (variability) defects.

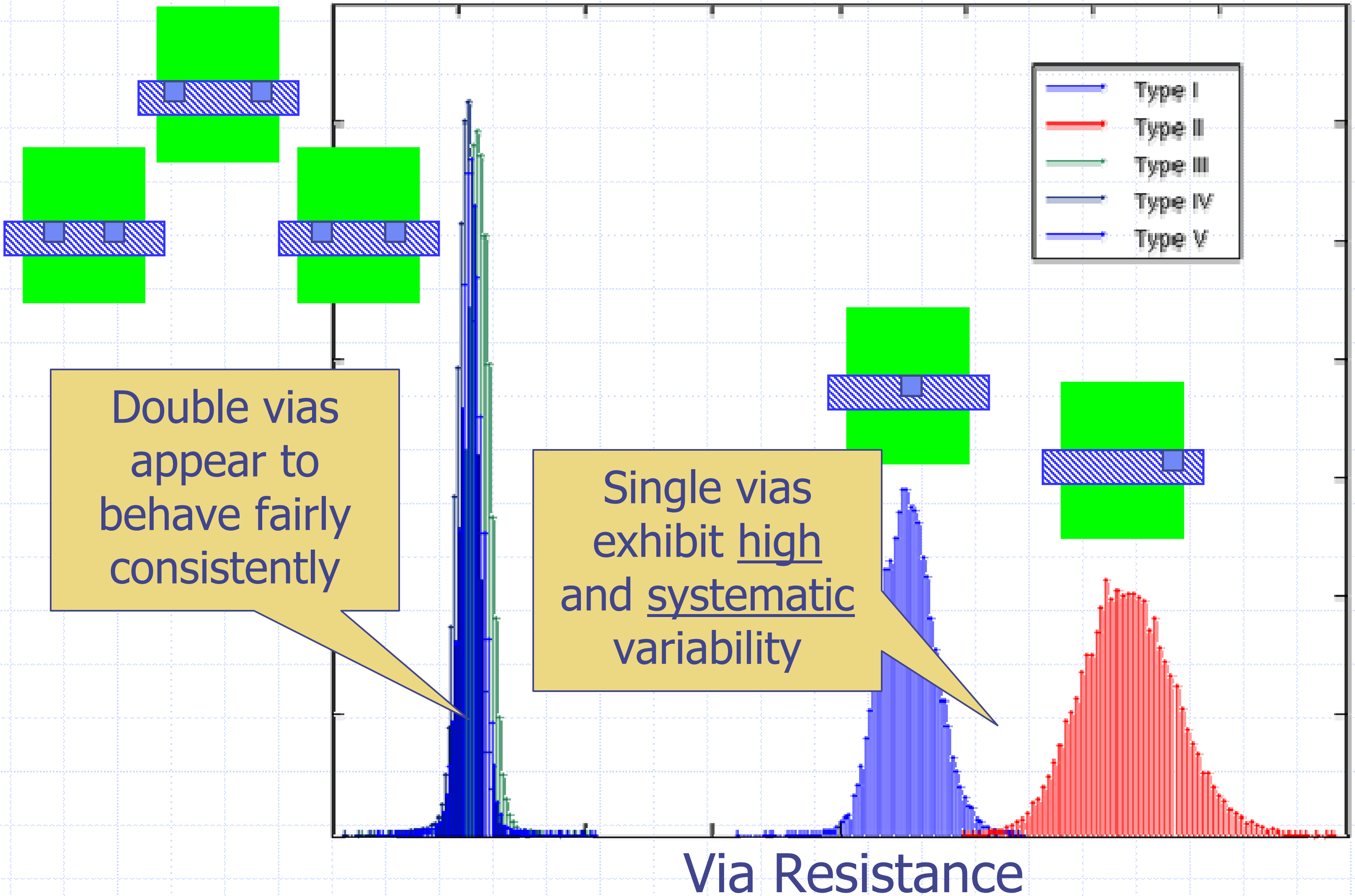


How Is This Happening?

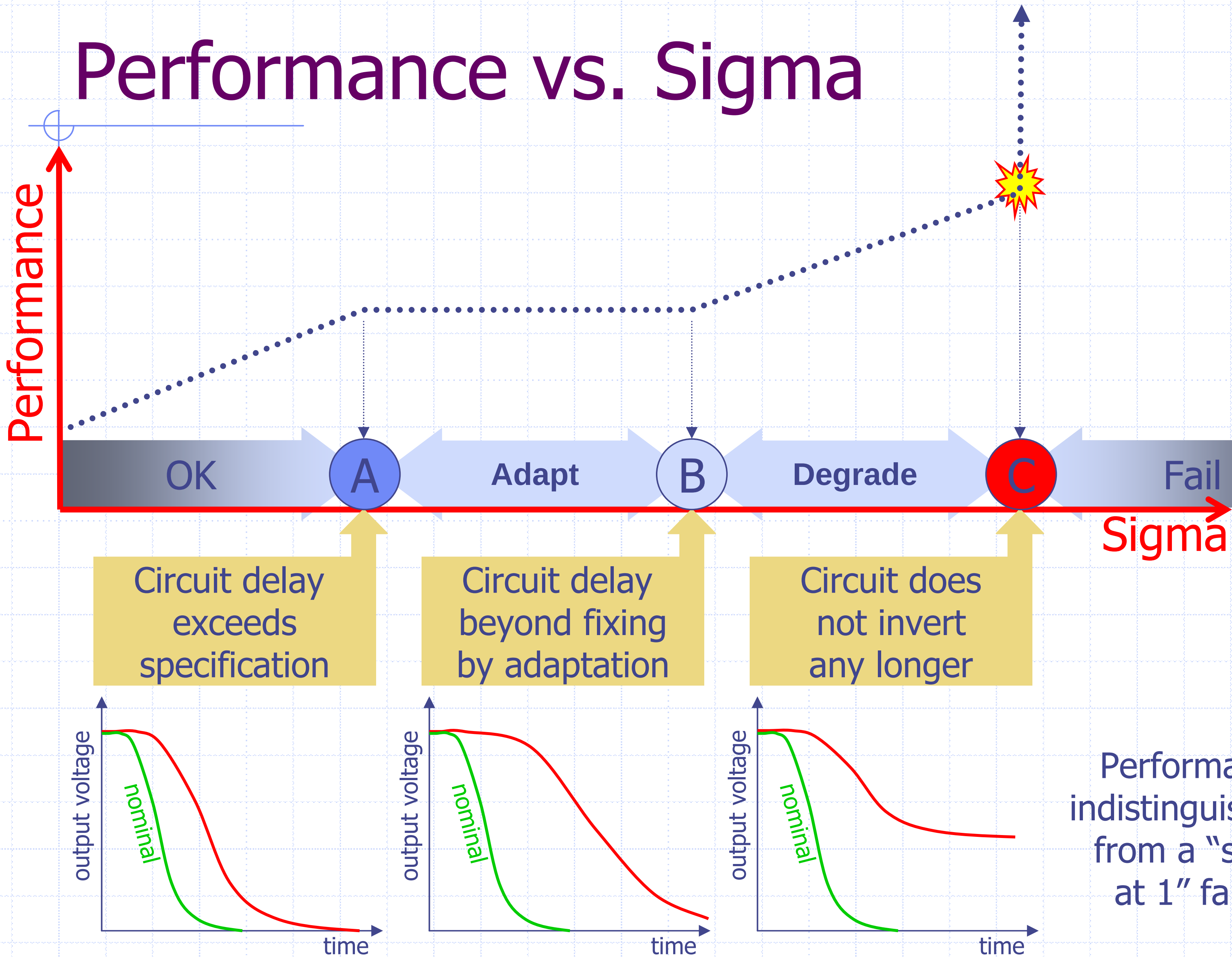
- Increased process complexity and systematic variability.
  - Example: a V_T of 0.25 ± 0.1, a via of $20 \ldots 200\Omega$.
  - Multidimensional: combination of multiple sources of variations.
- As variability increases, circuit performance passes from a degraded phase to a regime where failure becomes indistinguishable from hard (short/open) faults.



Random/Systematic Via Variability



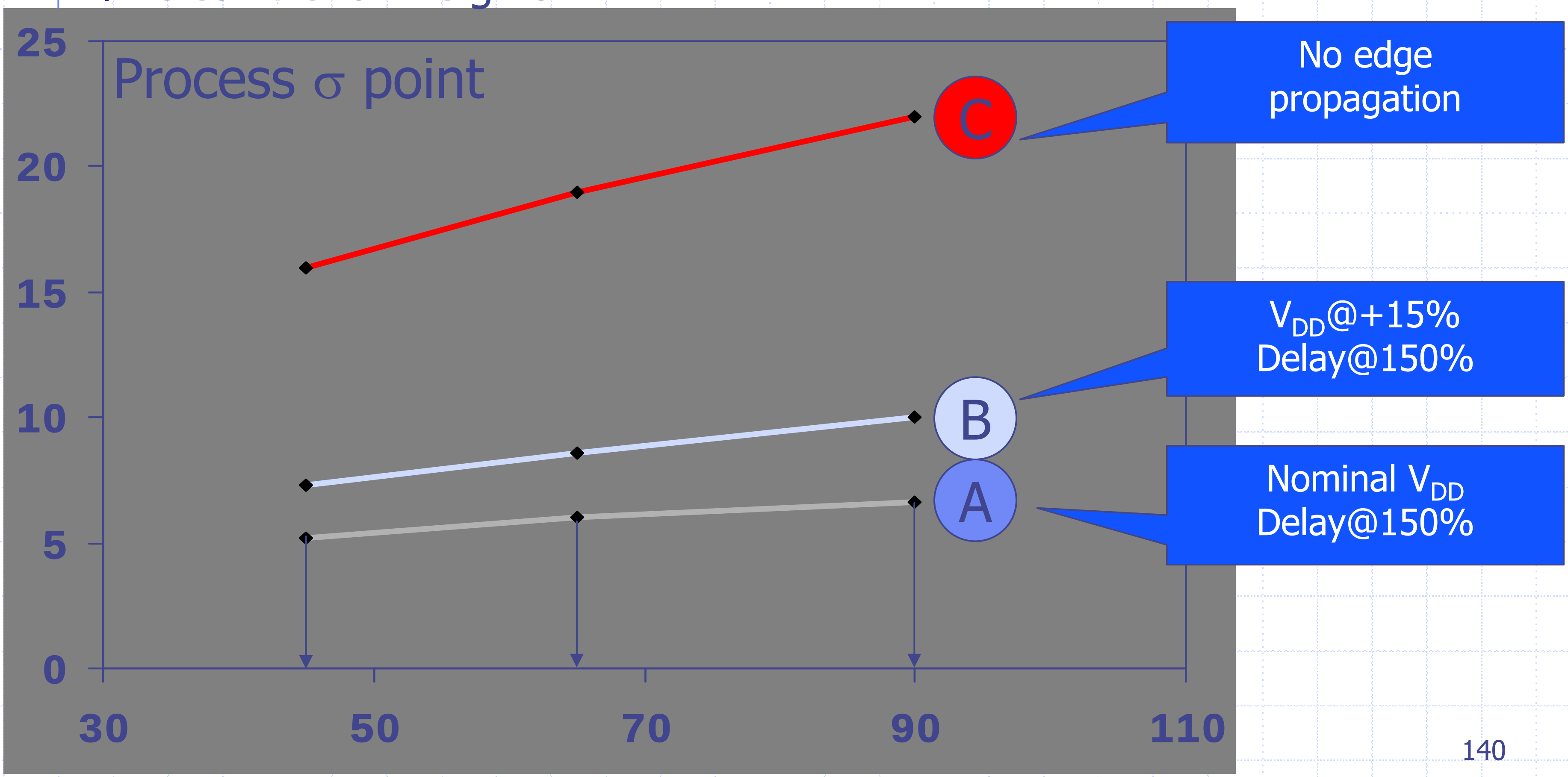
Performance vs. Sigma



Performance indistinguishable from a "stuck at 1" fault!

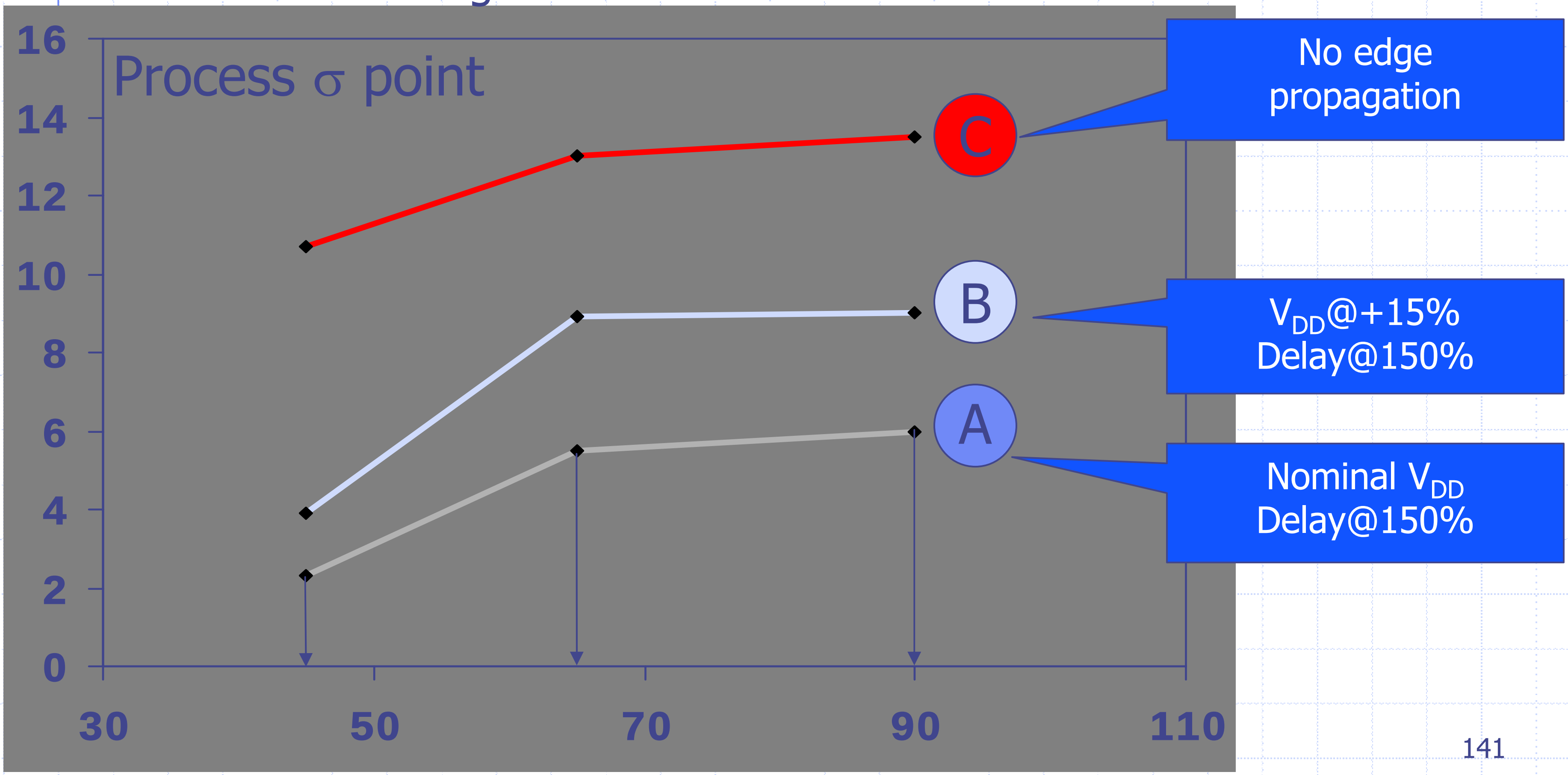
Trend For a Simple Buffer

- Simplest possible circuit (if this fails, everything else will).
- Performed analysis for 90nm, 65nm and 45nm.
- Clear trend in sigma!



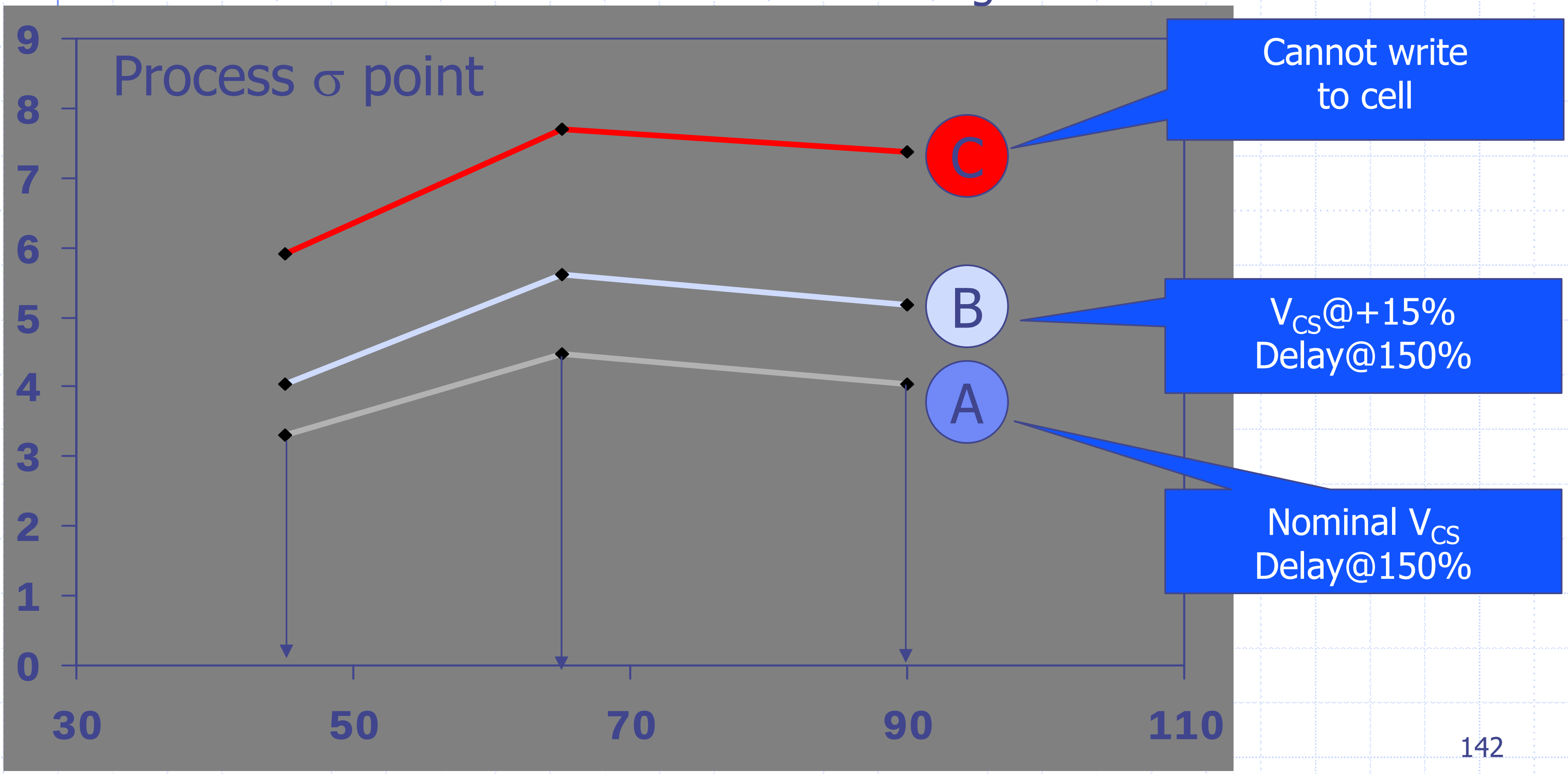
Technology Trend For a Simple Latch

- Pervasive circuit crucial for correct logic operation.
- Performed analysis for 90nm, 65nm and 45nm.
- Clear trend in sigma!



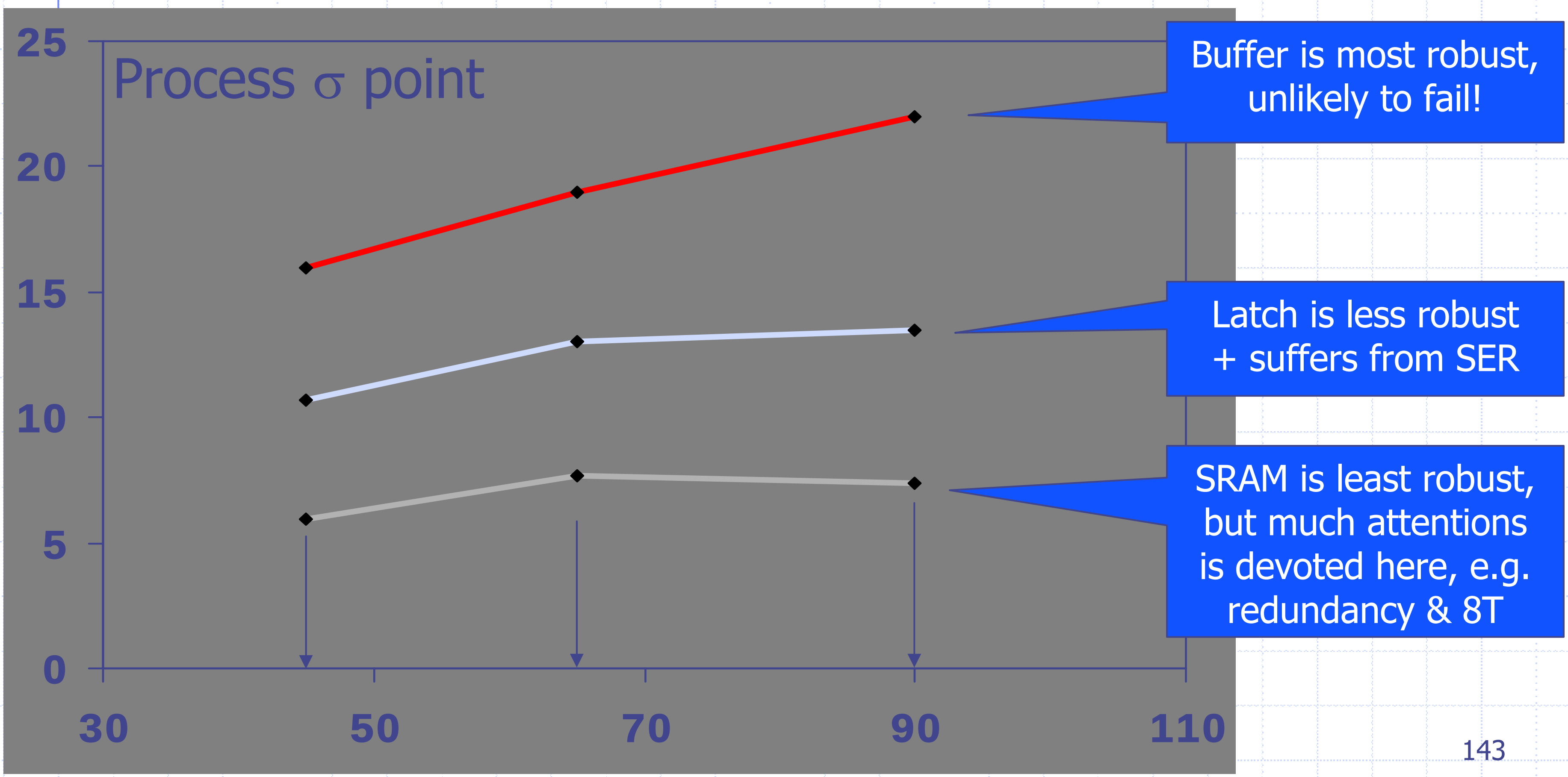
Technology Trend for an SRAM

- SRAM is known to be a more sensitive circuit… (lower σ).
- But, circuit heavily optimized for each technology.
- Much lower σ values + similar trend in sigma!



Comparison of Circuits (@Point C)

- Technology trend is modulated by circuit innovation and investment in analysis and optimization tools.
- Global trend remains clear!



Variability and Resilience

- We will need resilience at and beyond the 22nm technology node.

- How much resilience and/or adaptation will be determined by how well we understand the fabrication process.
  - Firm understanding of the sources and impact of systematic variation will be needed.
  - Magnitude of random or un-modeled variation will determine design margins (and design profit).

Implications

- As systematic and random defect levels rise, yield of large designs drops.
  - Fix for systematic defects: **regularity**.
  - Fix for random defects: **resilience**.
- Levels of defect distribution and variability will determine the smallest size of usefully redundant unit.
  - Future architectures for digital systems moving in the direction of large multi-core systems, but is this the right level?
- Measurement and assessment of technology variability magnitudes and trends is necessary.
  - Need to know how much redundancy will be needed.
  - Budget for potential surprises…

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Homework Assignment

- Explore the variability of a CMOS Ring Oscillator.
- Create an N stage RO, and simulate it in Spice to measure it's frequency.
- Assess impact on frequency of:
  - Power supply, Temperature NCH/PCH device L.
- Create a model:
  - Freq = $F(V_{DD}, T, L_N, L_P)$
- Sort the four sources of variability by impact.
  - Taking care to normalize things properly.

Ring Oscillator Circuit

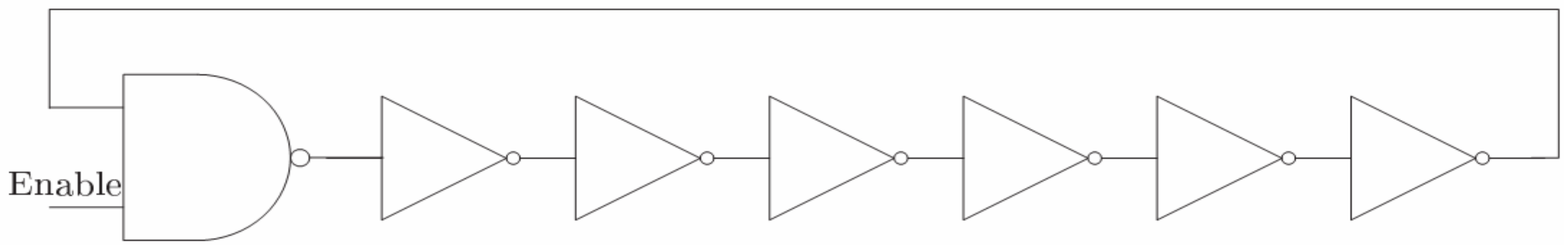

Fig. 4.1. A seven stage ring oscillator.

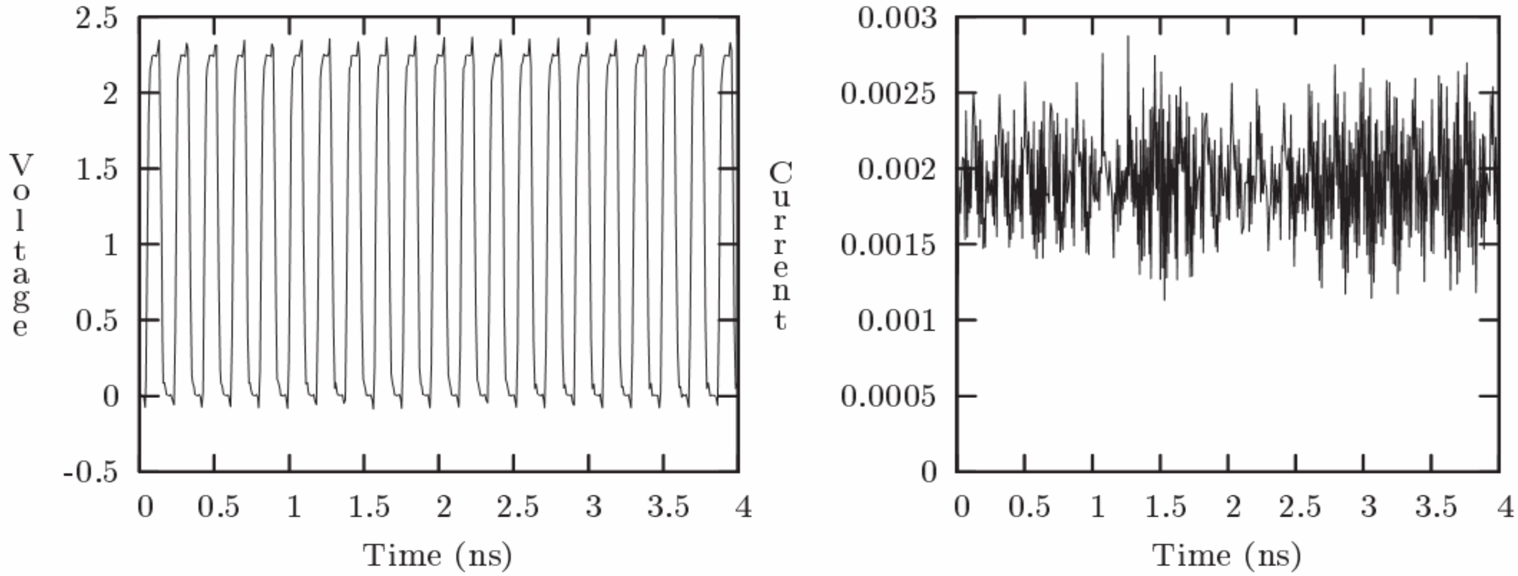

Fig. 4.2. Simulated voltage and current waveforms from seven stage ring oscillator..

An Example Result

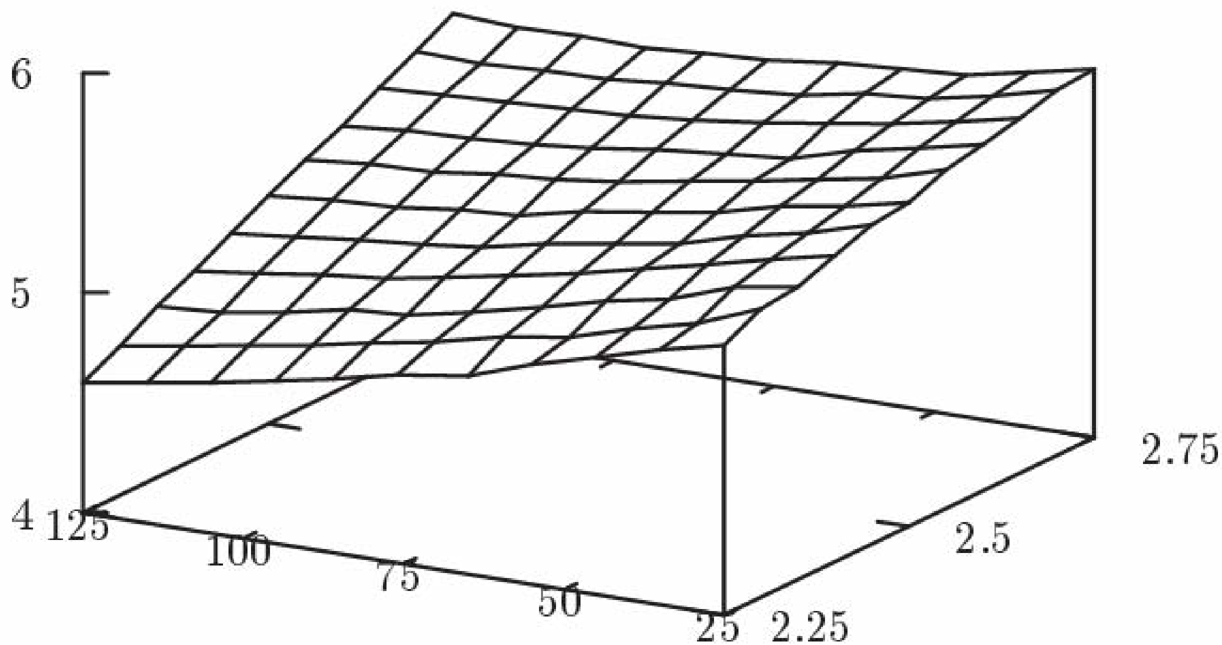

Fig. 4.3. Ring oscillator frequency vs. power supply voltage and temperature.

Assignment

- Select and document the amount of variation you would expect in the parameters.
  - Power supply, Temperature, NFET/PFET device L, NFET/PFET Vth
- Justify the amount of variation you chose.
- Perform simulations over the range of variation you select.
- Verify that the RO "worked" over the range…
- Make plots of frequency vs. parameters.

Assignment

- Propose and justify a model for frequency as a function of the parameters.
  - Justification can be based on first order modeling, or on empirical observation.
- Show the fit of the model to the data.
  - Plot predicted vs. measured frequency.
  - Calculate error statistics (μ, σ).
  - Calculate correlation between measured and predicted frequency.
- Based on the model, rank the parameters in terms of impact. Justify.