Embedded System Design and Synthesis

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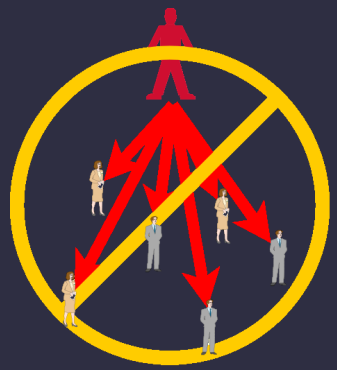


Status

- Specification, languages, and modeling
- Computational complexity, synthesis and optimization
- Real-time systems
- Scheduling
- Embedded operating systems
- Today: Power, temperature, and reliability
- Next: Wireless distributed sensing applications

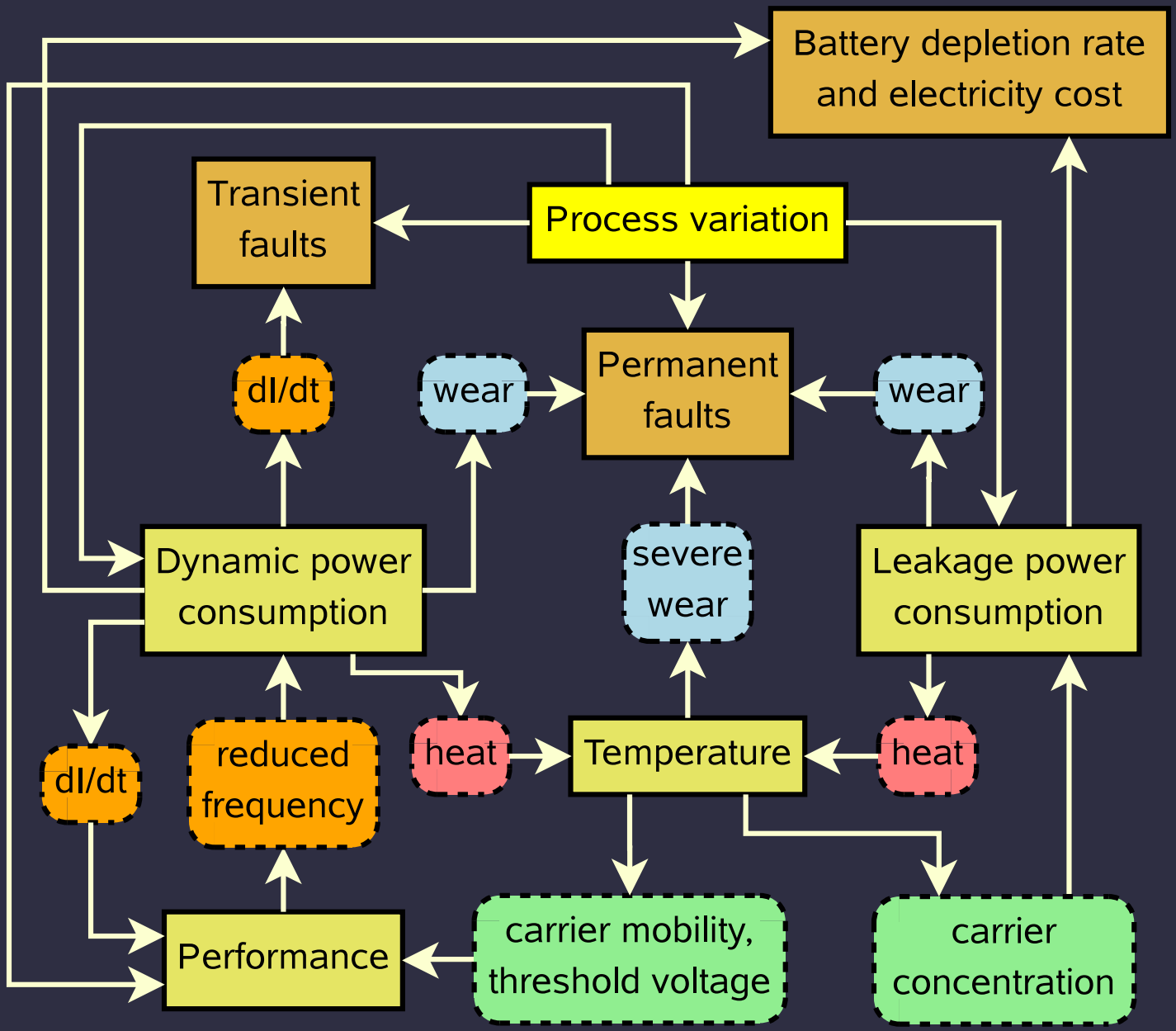
Outline

1. Power consumption
2. Homework

Section outline

1. Power consumption
   - Power and temperature
   - Power consumption modeling
   - Embedded system power consumption optimization

Power and temperature



Definitions

- Temperature: Average kinetic energy of particle
- Heat: Transfer of this energy
- Heat always flows from regions of higher temperature to regions of lower temperature
- Particles move
- What happens to a moving particle in a lattice?

Acoustic phonons

- Lattice structure
- Transverse and longitudinal waves
- Electron–phonon interactions

Optic phonons

- Minimum frequency, regardless of wavelength
- Only occur in lattices with more than one atom per unit cell
- Optic phonons out of phase from primitive cell to primitive cell
- Positive and negative ions swing against each other
- Low group velocity
- Interact with electrons
- Importance in nanoscale structure modeling?
- Boundary scattering and superlattices

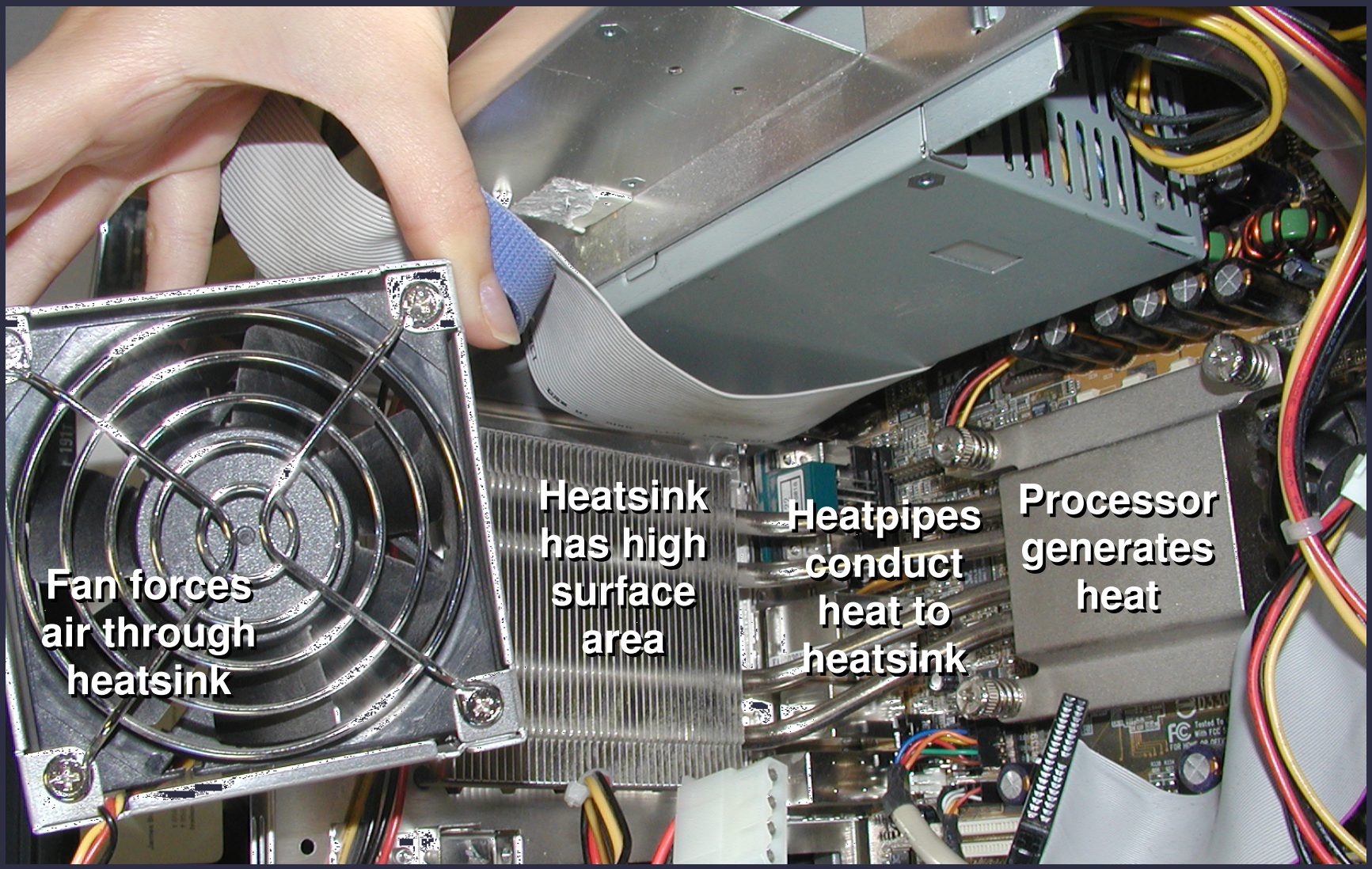
Why do wires get hot?

- Scattering of electrons due to destructive interference with waves in the lattice.
- What are these waves?
- What happens to the energy of these electrons?
- What happens when wires start very, very cool?
- What is electrical resistance?
- What is thermal resistance?

Why do transistors get hot?

- Scattering of electrons due to destructive interference with waves in the lattice
- Where do these waves come from?
- Where do the electrons come from?
  - Intrinsic carriers
  - Dopants
- What happens as the semiconductor heats up?
  - Carrier concentration increases
  - Carrier mobility decreases
  - Threshold voltage decreases

Cooling


Fan forces air through heatsink
Heatsink has high surface area
Heatpipes conduct heat to heatsink
Processor generates heat

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Power consumption trends

- Initial optimization at transistor level
- Further research-driven gains at this level difficult
- Research moved to higher levels, e.g., RTL
- Trade area for performance and performance for power
- Clock frequency gains linear
- Voltage scaling $V_{DD}{}^2$ – very important

Power consumption in synchronous CMOS

$$P = P_{SWITCH} + P_{SHORT} + P_{LEAK}$$

$$P_{SWITCH} = C \cdot {V_{DD}}^2 \cdot f \cdot A$$

$$\dagger\ P_{SHORT} = \frac{b}{12}(V_{DD} - 2 \cdot V_T)^3 \cdot f \cdot A \cdot t$$

$$P_{LEAK} = V_{DD} \cdot (I_{SUB} + I_{GATE} + I_{JUNCTION} + I_{GIDL})$$

C : total switched capacitance

V_{DD} : operating voltage

f : switching frequency

A : switching activity

b : MOS transistor gain

V_T : threshold voltage

t : rise/fall time of inputs

† P_{SHORT} usually $\leq 10\%$ of P_{SWITCH}

Smaller as $V_{DD} \to V_T$

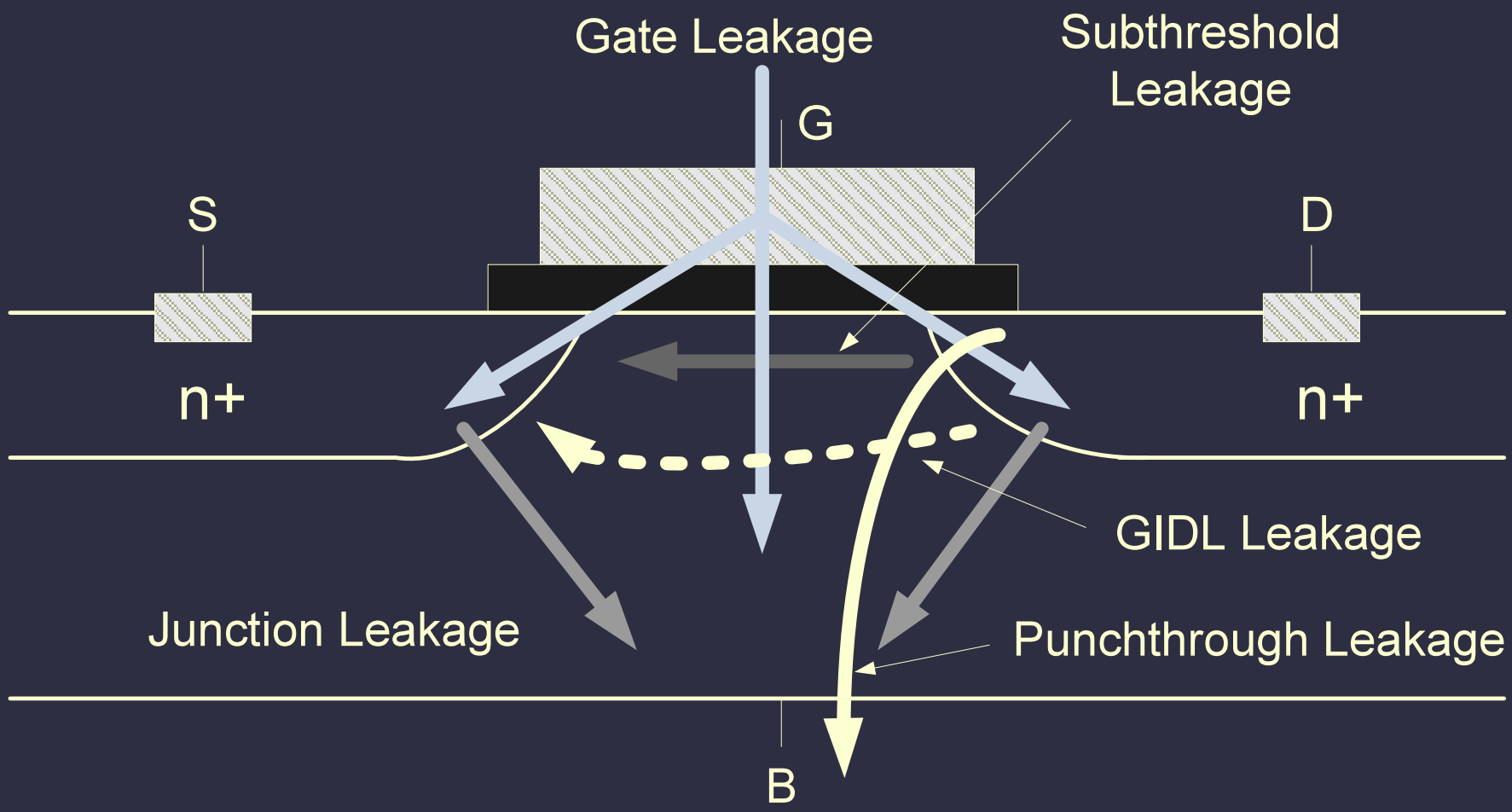
Adiabatic charging

- Voltage step function implies $E = C{V_{CAP}}^2/2$
- Instead, vary voltage to hold current constant: $E = C{V_{CAP}}^2 \cdot RC/t$
- Lower energy if $T > 2RC$
- Impractical when leakage significant

Wiring power consumption

- In the past, transistor power $\gg$ wiring power
- Process scaling $\Rightarrow$ ratio changing
- Conventional CAD tools neglect wiring power
- Indicate promising areas of future research

Leakage


Gate Leakage
Subthreshold Leakage
G
S
D
n+
n+
GIDL Leakage
Junction Leakage
Punchthrough Leakage
B

Subthreshold leakage current

$$I_{subthreshold} = A_s \frac{W}{L} {v_T}^2 \left(1 - e^{\frac{-V_{DS}}{v_T}}\right) e^{\frac{(V_{GS} - V_{th})}{n v_T}}$$

- where A_s is a technology-dependent constant,
- V_{th} is the threshold voltage,
- L and W are the device effective channel length and width,
- V_{GS} is the gate-to-source voltage,
- n is the subthreshold swing coefficient for the transistor,
- V_{DS} is the drain-to-source voltage, and
- v_T is the thermal voltage.

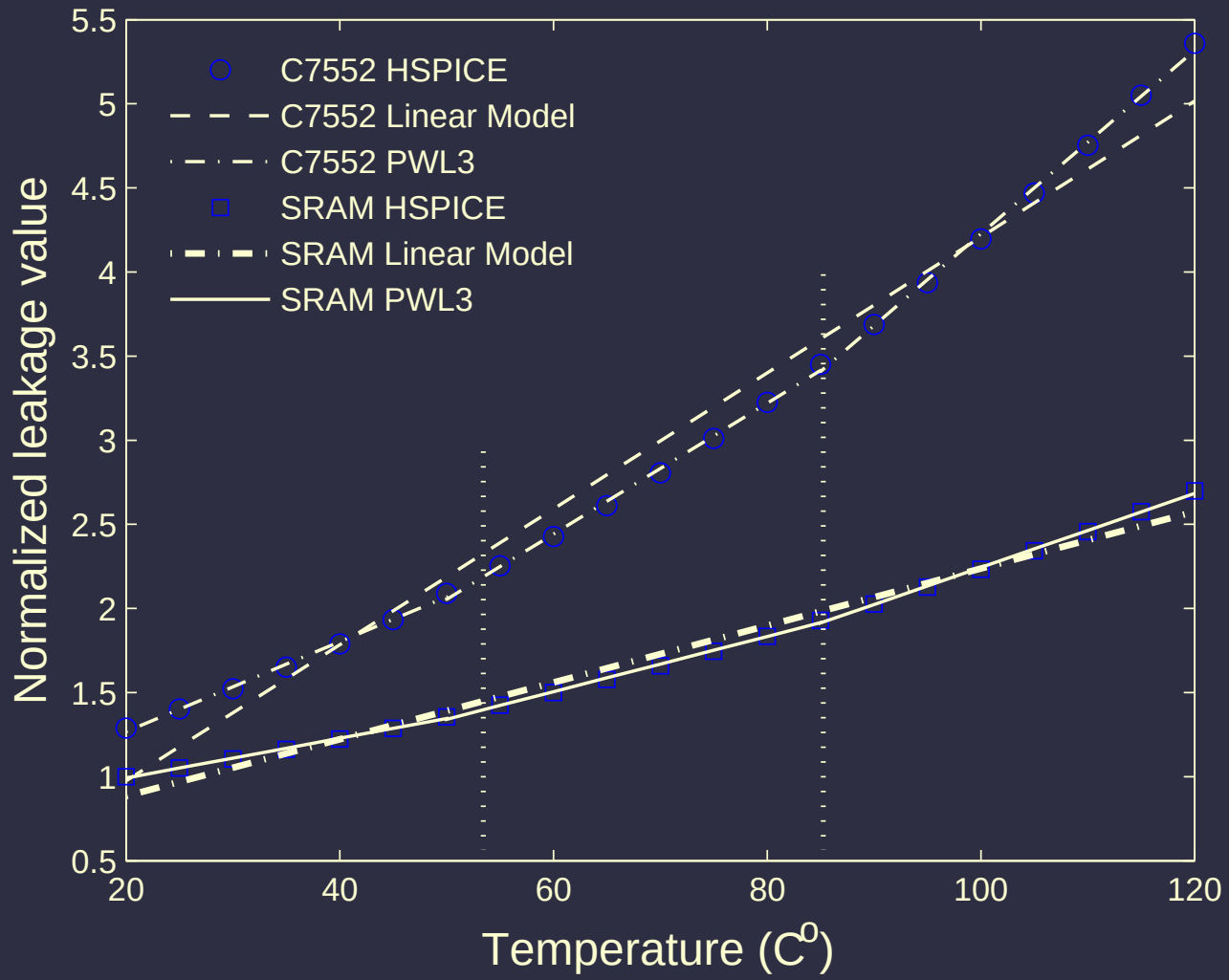
A. Chandrakasan, W.J. Bowhill, and F. Fox. *Design of High-Performance Microprocessor Circuits*. IEEE Press, 2001

Simplified subthreshold leakage current

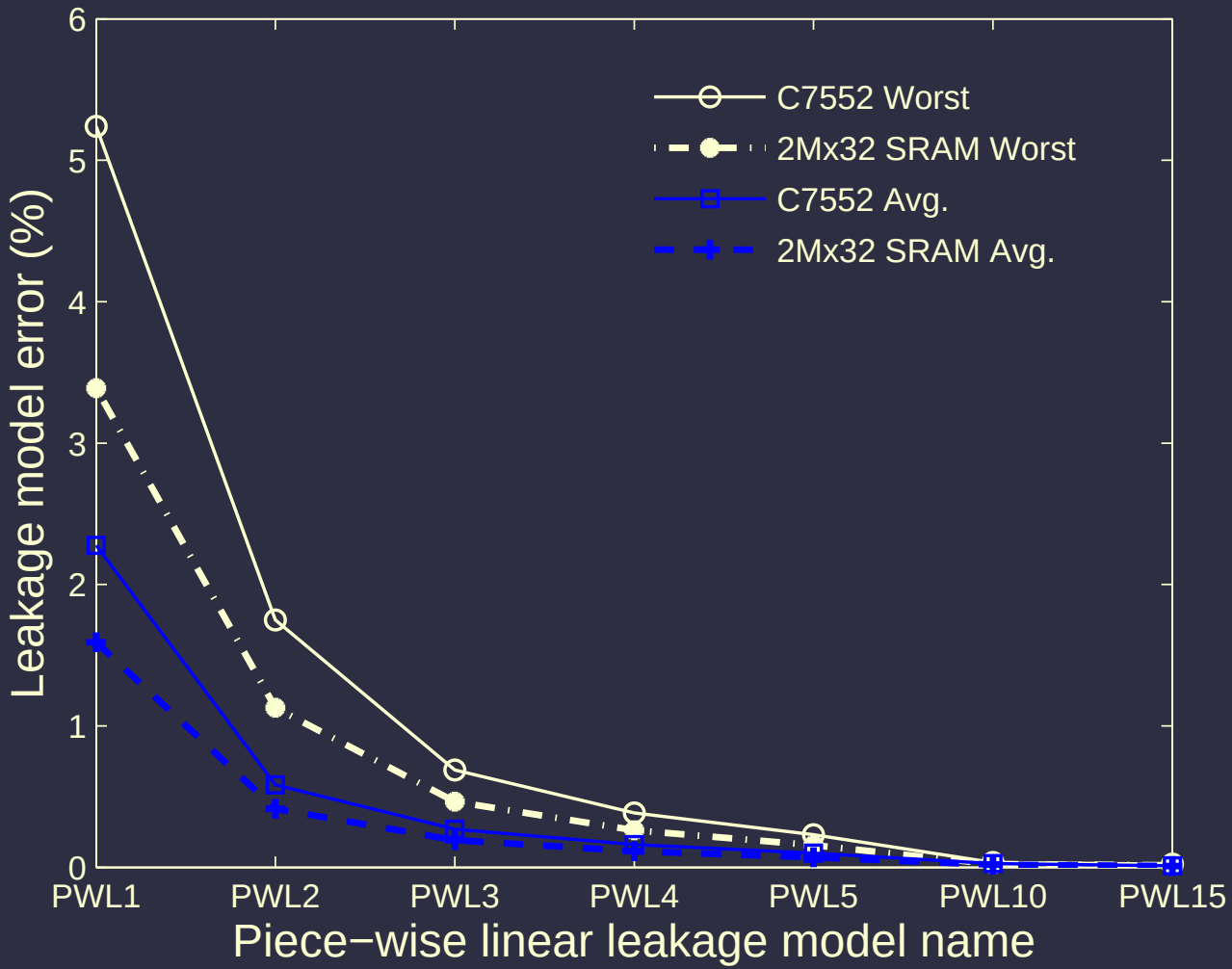
$V_{DS} \gg v_T$ and $v_T = \frac{kT}{q}$. q is the charge of an electron. Therefore, equation can be simplified to

$$I_{subthreshold} = A_s \frac{W}{L} \left(\frac{kT}{q} \right)^2 e^{\frac{q(V_{GS} - V_{th})}{nkT}} \quad (1)$$

Exponential?



Piece-wise linear error



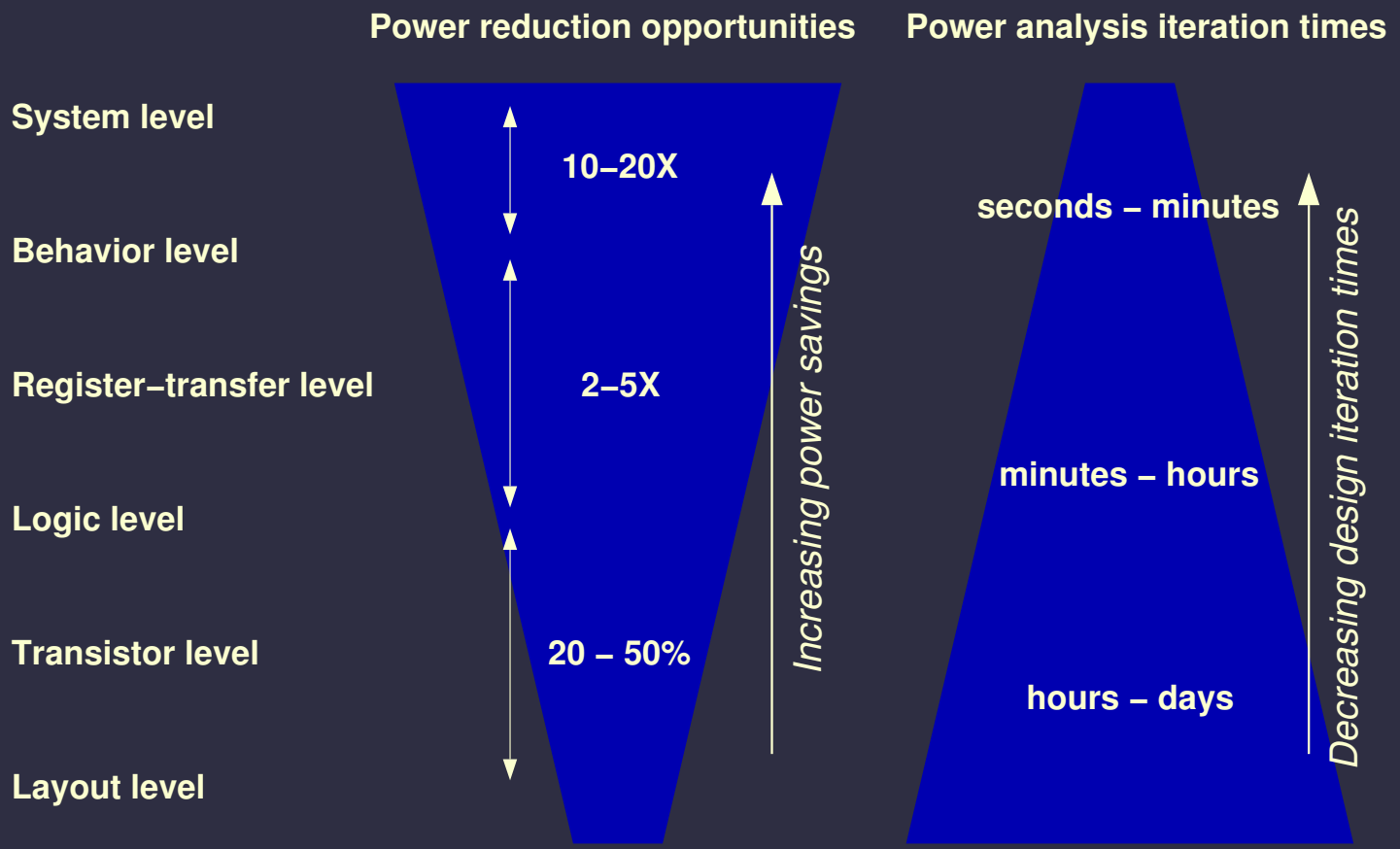
Gate leakage

$$I_{gate} = WLA_J \left(\frac{T_{oxr}}{T_{ox}} \right)^{nt} \frac{V_g V_{aux}}{T_{ox}^2} e^{-BT_{ox}(a-b|V_{ox}|)(1+c|V_{ox}|)}$$

- where A_J, B, a, b, and c are technology-dependent constants,
- nt is a fitting parameter with a default value of one,
- V_{ox} is the voltage across gate dielectric,
- T_{ox} is gate dielectric thickness,
- T_{oxr} is the reference oxide thickness,
- V_{aux} is an auxiliary function that approximates the density of tunneling carriers and available states, and
- V_g is the gate voltage.

K. M. Cao, W. C. Lee, W. Liu, X. Jin, P. Su, S. K. H. Fung, J. X. An, B. Yu, and C. Hu. BSIM4 gate leakage model including source-drain partition. In *IEDM Technology Dig.*, pages 815–818, December 2000

Design level power savings



From Anand Raghunathan

Power consumption conclusions

- Voltage scaling is currently the most promising low-level power-reduction method: V^2 dependence.
- As V_{DD} reduced, V_T must also be reduced.
- Sub-threshold leakage becomes significant.
- What happens if $P_{LEAK} > P_{SWITCH}$?
- Options to reduce leakage (both expensive):
  - Liquid nitrogen – diode leakage
  - Silicon-on-insulator (SOI) – I_{SUB}

Reference

G. Chen, R. Yang, and X. Chen. Nanoscale heat transfer and thermal-electric energy conversion. *J. Phys. IV France*, 125:499–504, 2005

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What can be done to reduce power consumption in embedded systems?

Please take/refer to your notes for this portion of the lecture.
It is meant to be interactive.

Power minimization techniques

- Reduce switching activity/clock frequency, glitching
- Reduce voltage (quadratic)
- Reduce capacitance
- Reduce temperature or increase threshold to reduce leakage
- Power/clock gating
- System-level power management, prediction

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Embedded operating system assignments I

- Due 6 October: L. Yang, Robert P. Dick, Haris Lekatsas, and Srimat Chakradhar. High-performance operating system controlled on-line memory compression. *ACM Trans. Embedded Computing Systems*, 9(4):30:1–30:28, March 2010.
- Due 11 October: Preeti Ranjan Panda, Nikil D. Dutt, and Alexandru Nicolau. On-chip vs. off-chip memory: the data partitioning problem in embeddeed processor-based systems. *ACM Trans. Embedded Computing Systems*, 5(3):682–704, July 2000.
- Due 13 October: Mini-project presentation.
- Due 14 October (emailing the summary is fine): M. Tim Jones. Anatomy of real-time Linux architectures. Technical report, April 2008 (this is fun and light reading).

Embedded operating system assignments II

- Due 20 October: Mini-project report.
- Due 25 October: Main project selection.
- Due date for main project presentation to be announced.
- Due 13 December: Main project report.

Example mini-project report format

1. Introduction and Motivation: Overview of what you are trying to accomplish, and reason why it is important.
2. Past Work and Contributions: Survey of related work. Most reports will find at least five relevant prior publications. Summarize them, and contrast your work with past work.
3. Problem Statement: Give a formal definition for the problem you are trying to solve.
4. Proposed Solution: Explain how you have solved the problem.
5. Experimental Evaluation: Give any experimental, simulation, or analytical parameters studies here.
6. Conclusions: Did you reach your goal? If not, why not? What new knowledge have your efforts yielded?

Upcoming topics

- Wireless distributed sensing applications.
- Human-centered computer design.
- Energy supply in embedded systems.