3D ICs

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Overview

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2. 3D ICs vs. 3D Packaging
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7. Challenges with 3D
8. Notable 3D chips
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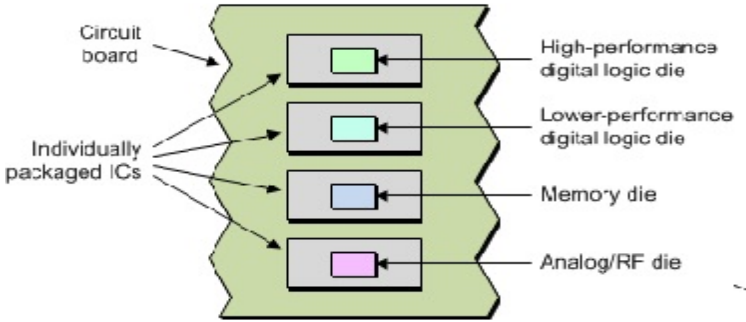
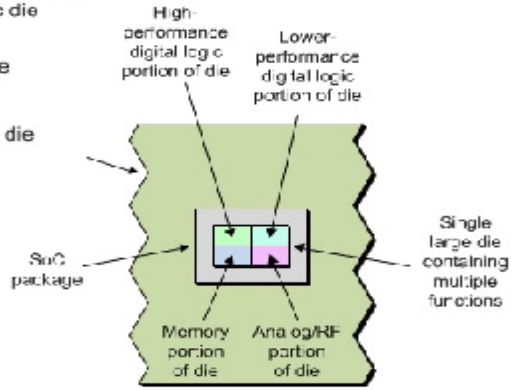
2D and 2.5D ICs

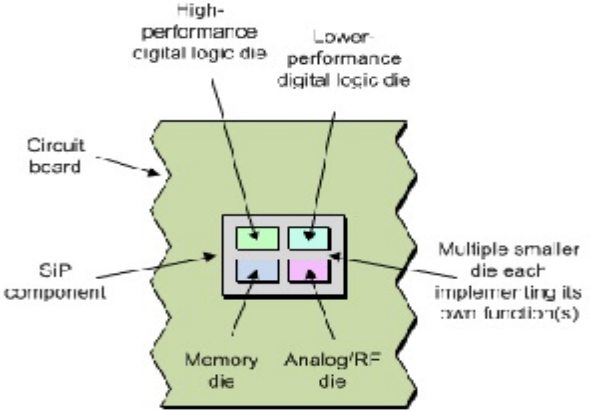
2D IC's



Circuit Board With individually Packed Chips

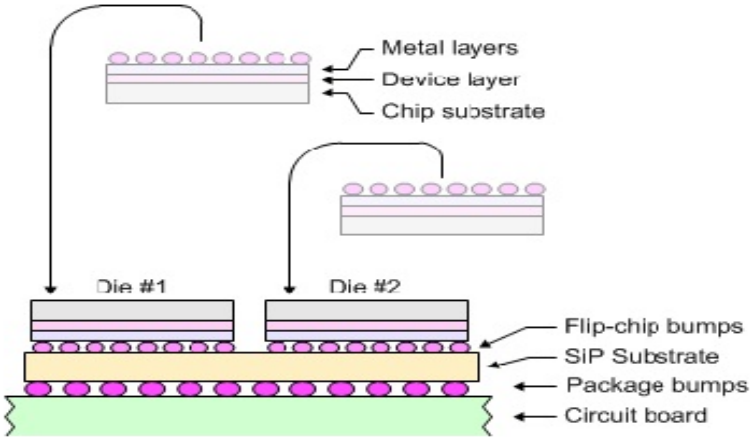


Birds-eye view of circuit board with a System-on-Chip (SoC) device

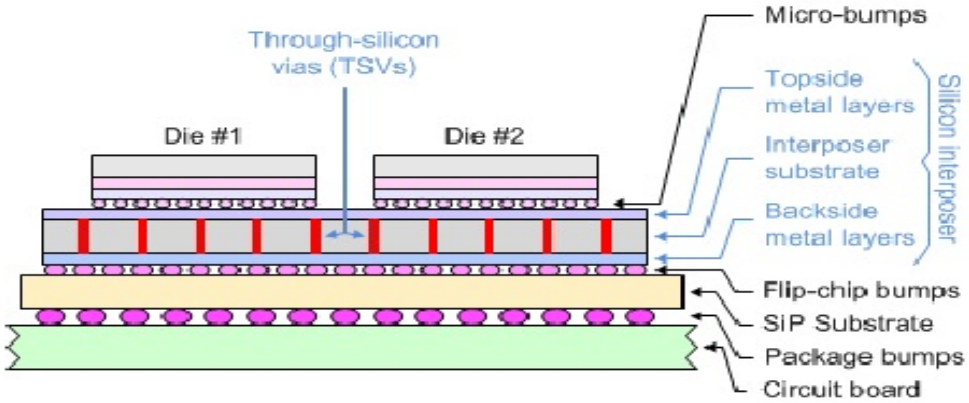


Birds-eye view of circuit board with a System-in-Package (SiP) device

2.5D Integrated Circuits



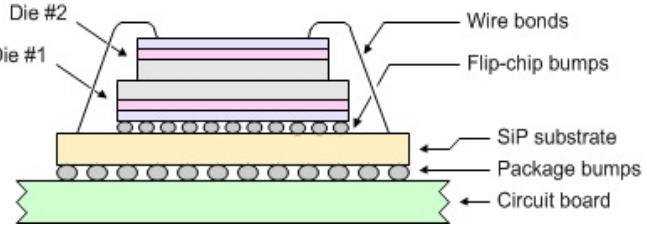
A traditional 2D IC/SiP



A 2.5D IC/SiP using a silicon interposer and through-silicon vias (TSVs)

3D ICs vs. 3D Packaging

Wait isn't 3D Packaging and 3DIC's the same?



Are today's '3D' chips really 3D?

- In a 3D package, separate chips are stacked in a single package. They may be stacked one above the other or side-by-side. The chips are merely stacked and connected using interconnects but not integrated into a single chip.

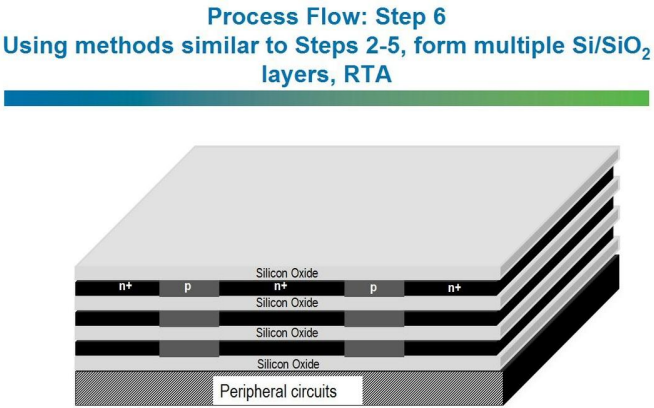
- In contrast, a 3D IC is a single chip. Multiple dice are stacked, connected using through-silicon vias (TSVs), and multiple groups of dice again connected together using a silicon interposer—and all of this is mounted on a single SiP.

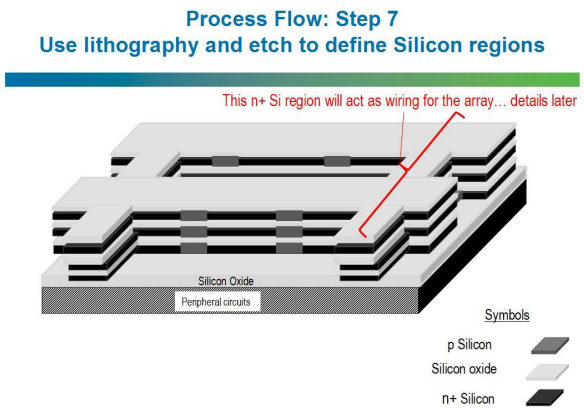
- 3D chips are in development stage, and any chip touted as 3D today is essentially a 2.5D chip or a 3D package.

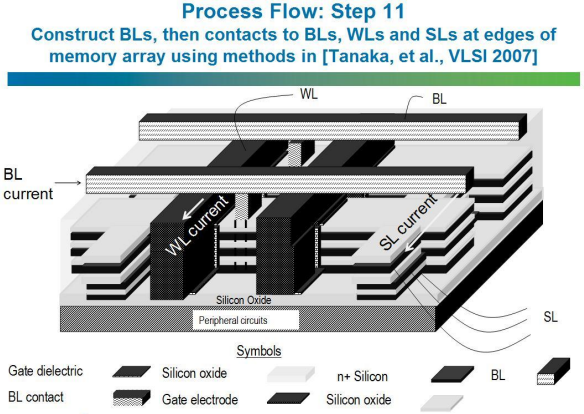
Manufacturing Technologies

Manufacturing Technologies

- Currently 4 ways to make 3D ICs



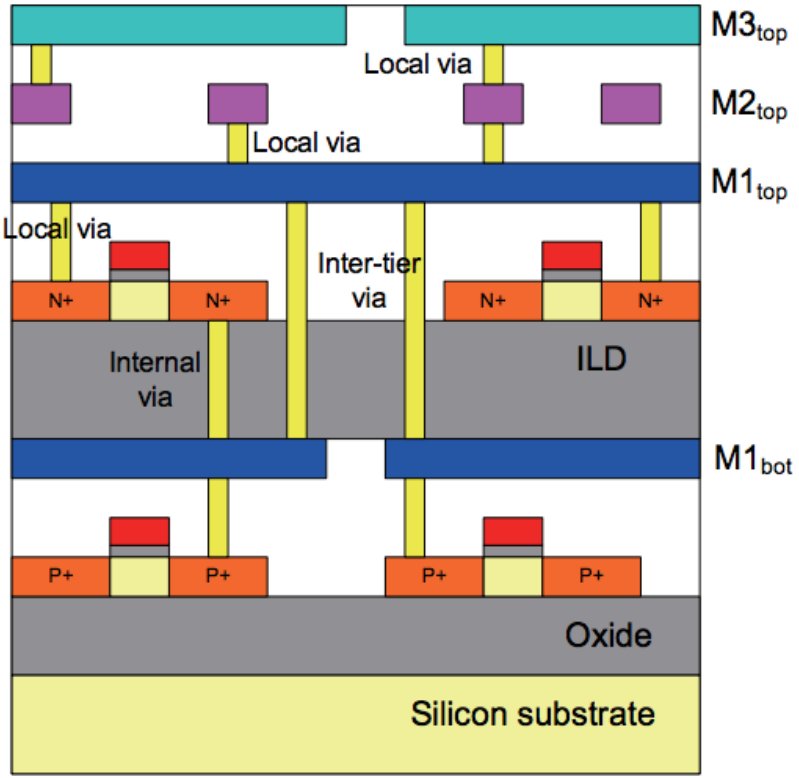




http://www.monolithic3d.com/3d-ic-edge.html

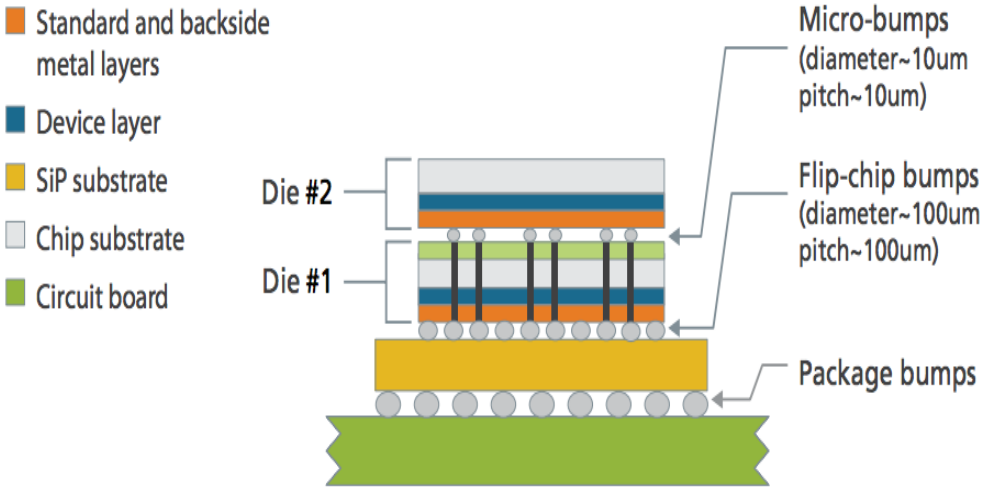
1. Monolithic

- Components and wiring built in layers on single wafer, then diced into 3D ICs
- (+) Only one substrate
  - No need for aligning, thinning, bonding, or “through-silicon vias” (TSVs)



http://www.gtcad.gatech.edu/www/papers/isqed12-1.pdf

2. Wafer-on-Wafer



- Components built on 2+ wafers, which are then aligned, bonded, diced into 3D ICs
- (–) Can reduce yields (if any chip in a 3D IC is defective, entire 3D IC is defective)
- (–) Wafers must be the same size, but many materials manufactured on smaller wafers than CMOS/DRAM

http://www.cadence.com/rl/resources/white_papers/3dic_wp.pdf

3. Die-on-Wafer

- Components built on 2 wafers
- One wafer diced, then aligned and bonded onto die sites of second wafer
- Additional dice may be added to stacks before dicing

4. Die-on-Die

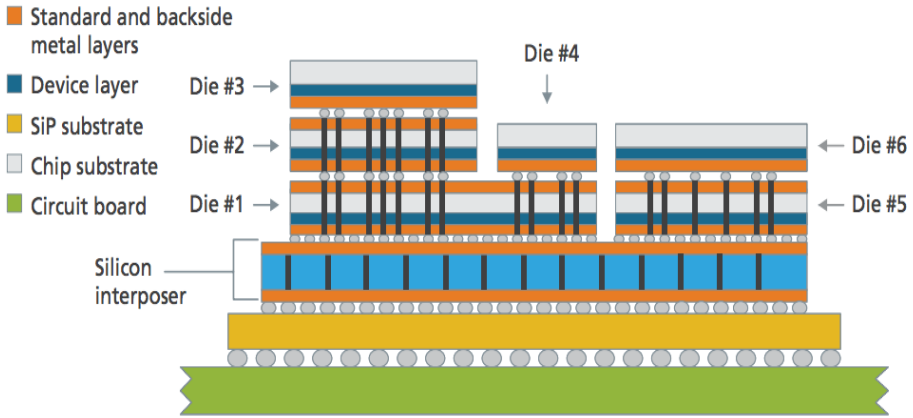


Figure 4: A more complex 3D IC using TSVs and 6 die

- Components built on multiple dice, then aligned, bonded
- (+) Each component die can be tested first
- (+) Each die can be “binned” beforehand, to mix and match process corners to optimize power/performance

http://www.cadence.com/rl/resources/white_papers/3dic_wp.pdf

Design Styles

Design Styles

- Gate level vs. board level integration

Gate-Level Integration

- Separates “cells” between multiple dies
- (+) Wire length reduction, flexibility
- (–) Many TSVs required
- (–) Requires 3D place-and-route software
- (–) Can’t test “blocks” before die stacking
- (–) Amplifies die variation

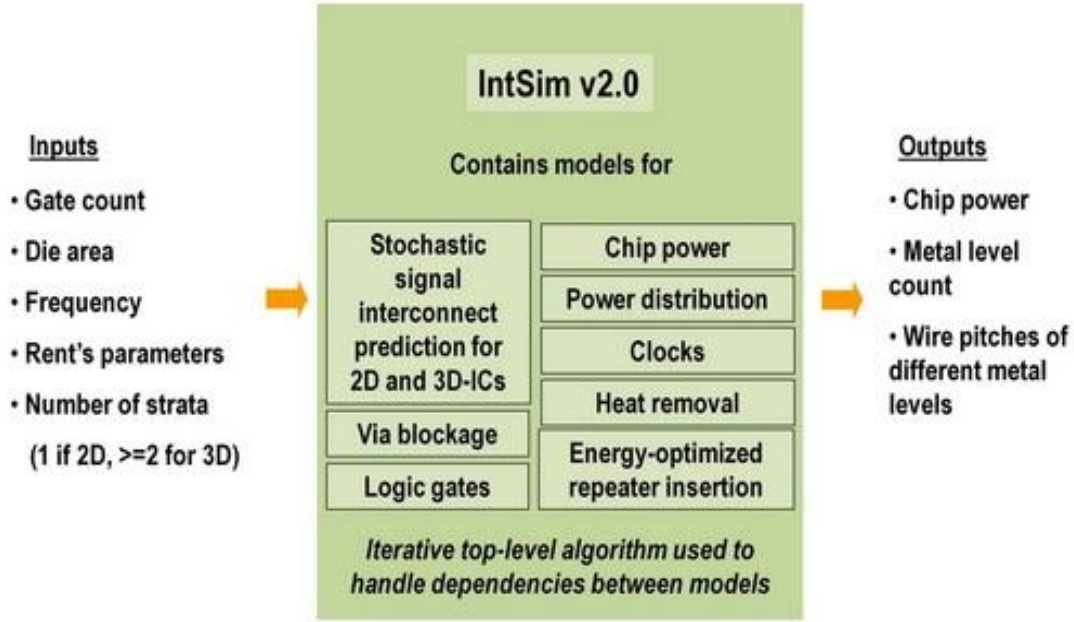
Board-Level Integration

- Assigns whole “blocks” to different dies
- (+) Reduces TSVs
- (+) Allows separate optimized processes
- (+) Only requires 3D tools for analysis/thermal sim
- (+) Easier to adapt 2D “blocks”

Simulators

IntSim

- Free, open source
- Java-based



Download: http://www.monolithic3d.com/simulators.html

Uses of IntSim v2.0

Simulate and optimize 2D and 3D-ICs

Students can play with the tool and interactively learn how a 2D or 3D-IC works.

Pre-silicon estimates for die size, number of metal levels, size of each metal level and chip power

Architectural decisions such as clock frequency, gate count, number of 3D stacked layers

Study scaling trends and make predictions about future technologies

Should I built a 3D-IC with 2 stacked device layers or 4 stacked device layers?

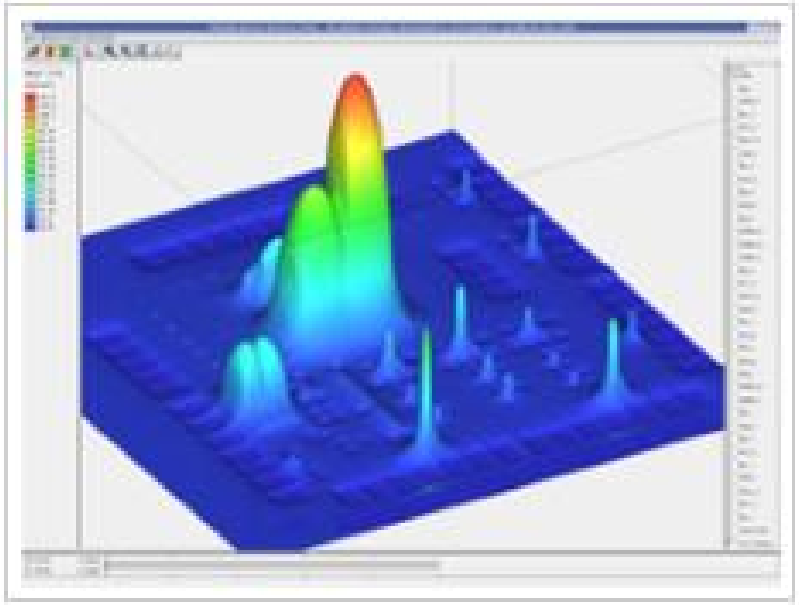
Will exponential wire resistivity increases at smaller nodes limit the benefits of scaling?

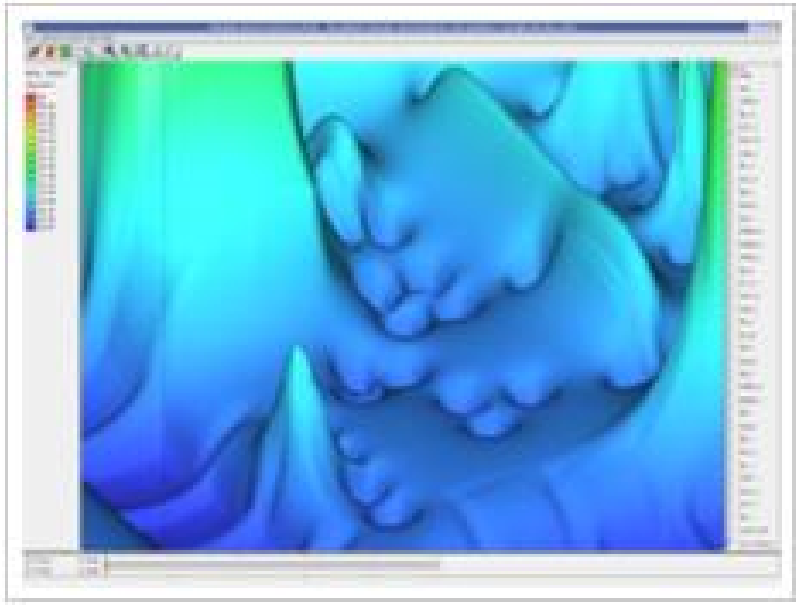
How will a graphene-based transistor impact chip performance and power?

How much chip power will I save if I develop a new low-k interconnect dielectric with 10% lower dielectric constant?

HeatWave

- Proprietary software from Gradient
- Creates temp profiles for 2D & 3D ICs





http://www.gradient-da.com/products/heatwave.php

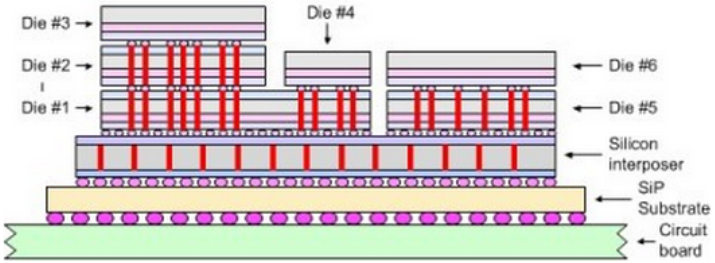
Synopsis 3D-IC EDA Suite

- Full EDA suite for 3D ICs
- Proprietary software
- Testing, layout, verification, simulation

http://www.synopsys.com/Solutions/EndSolutions/3D-IC-Solutions/Pages/default.aspx

Benefits

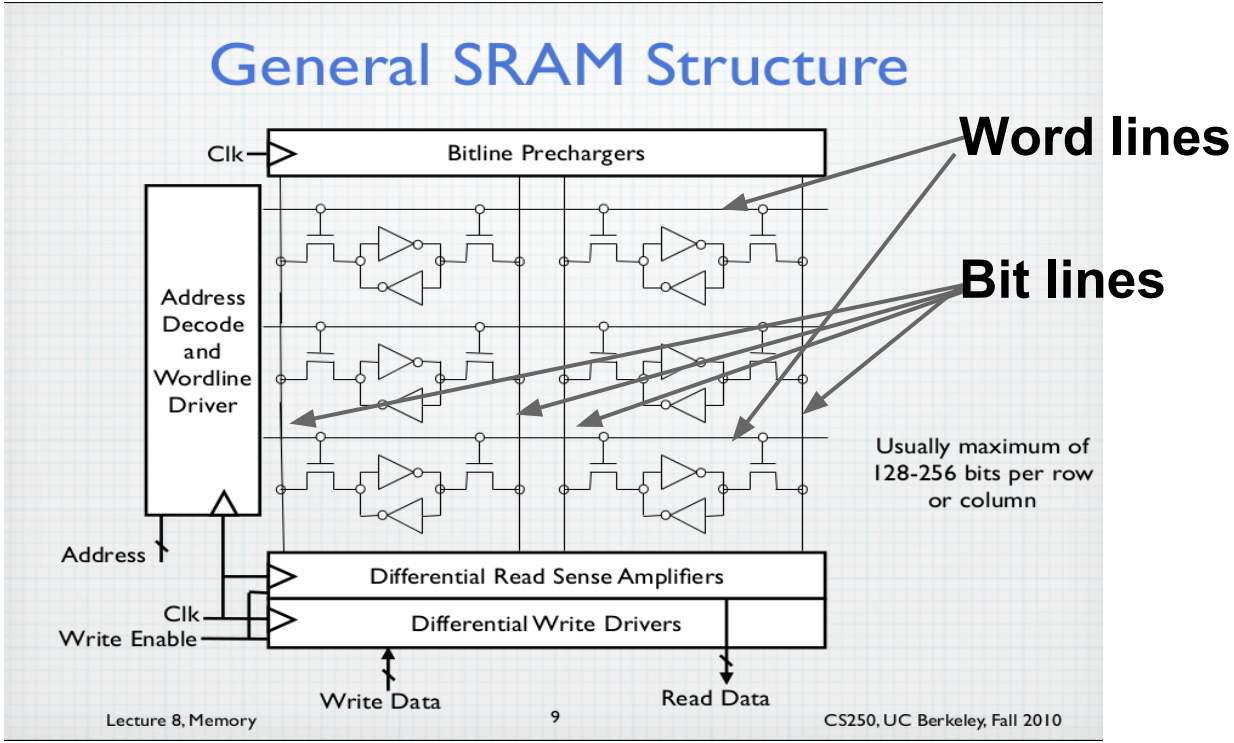
Benefits of 3D-IC



A more complex "True 3D IC/SiP"

- More than "Moore" integration
- Advantages over conventional 2D-IC
  - alleviating the communication bottleneck
  - integration of heterogenous materials
  - enabling novel architectures

Example - 3D-SRAM



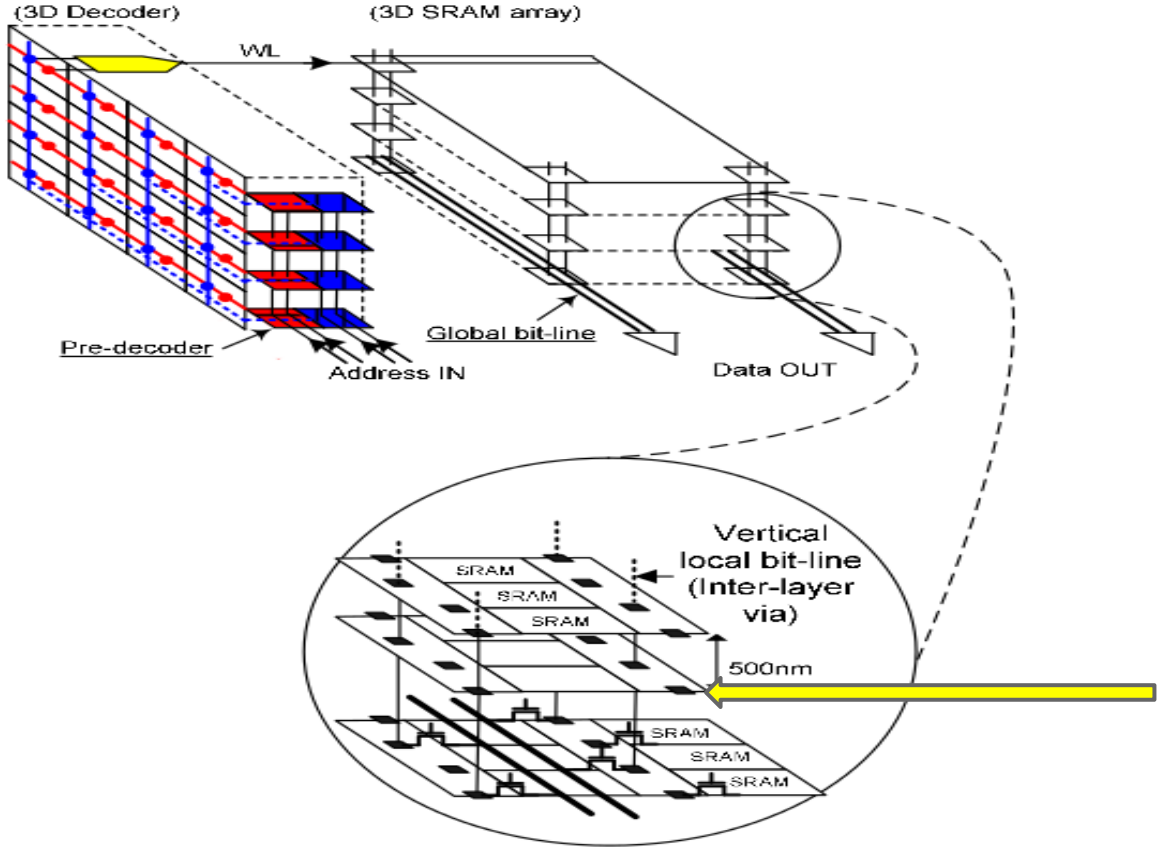
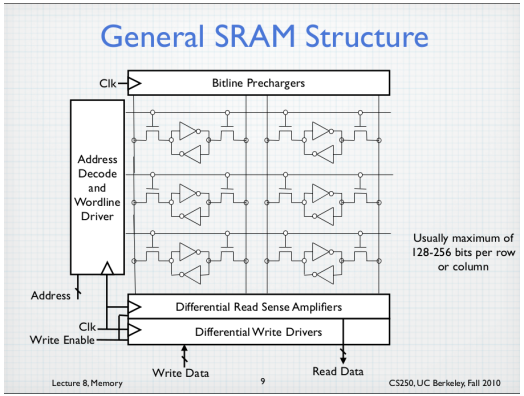
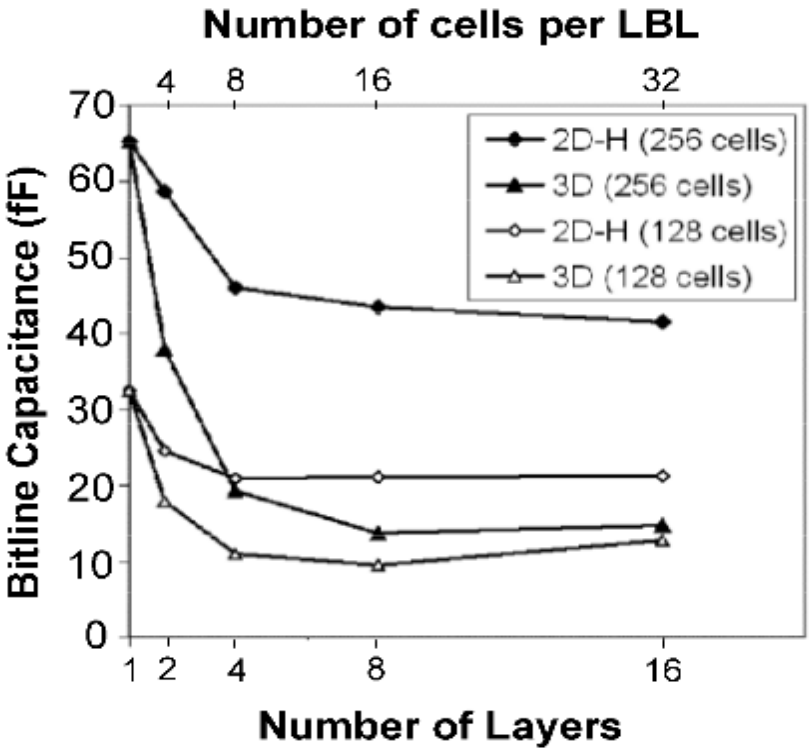
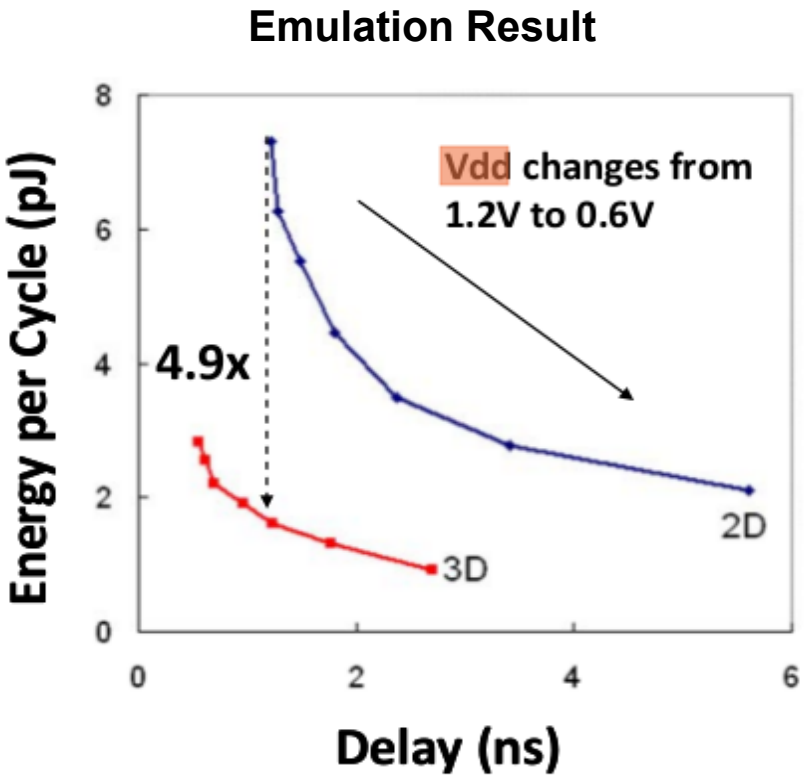


Fig. 3. 3D-SRAM architecture.

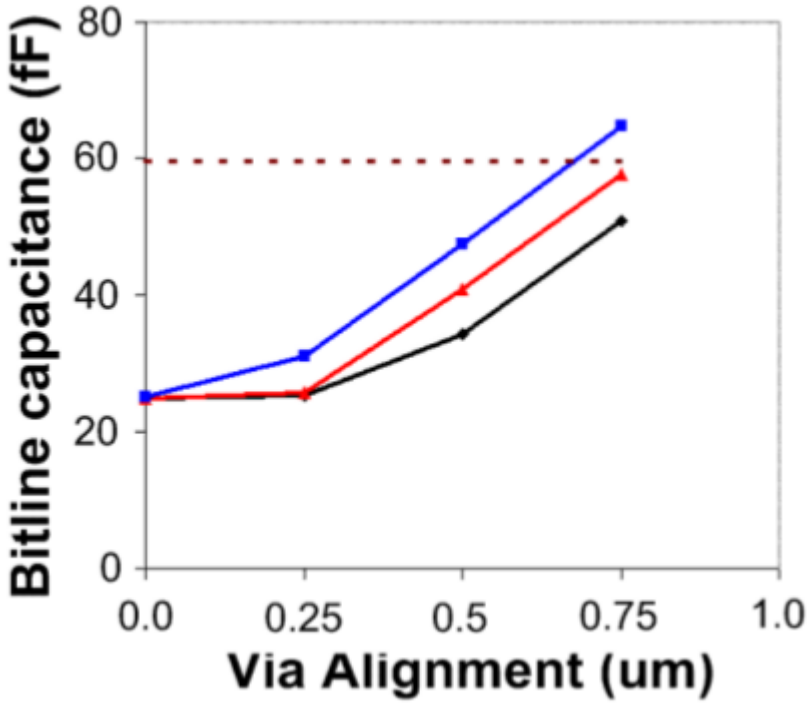



Number of cells per LBL
4
8
16
32
70
60
50
40
30
20
10
0
Bitline Capacitance (fF)
2D-H (256 cells)
3D (256 cells)
2D-H (128 cells)
3D (128 cells)
1
2
4
8
16
Number of Layers


Emulation Result
8
6
4
2
0
Energy per Cycle (pJ)
Vdd changes from
1.2V to 0.6V
4.9x
2D
3D
0
2
4
6
Delay (ns)

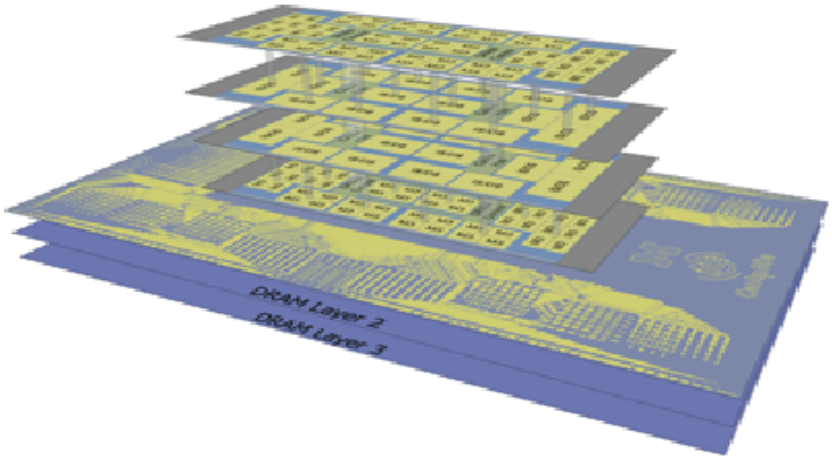
Challenges

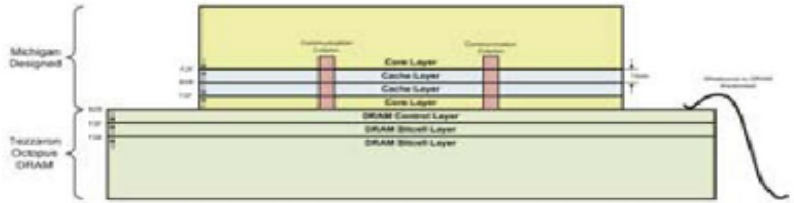
Challenges



- Misalignment
- Heat control
(overall speaking)

Centip3De: Near-Threshold 3D Stacked System





Centip3De is a near-threshold 7-layer 3D system that contains 128 ARM Cortex-M3 cores and 256MB of stacked DRAM. Centip3De uses the unique aspects of near-threshold computing to create highly energy efficient compute clusters. Centip3De uses Tezzaron's through-silicon via based 3D stacking and stacked DRAM.


Future

Near Future

- Three-dimensional integrated circuits or 3D chips are believed to be the best way to keep Moore's Law ticking.

- Semiconductor Manufacturing International Corp.
  - "consolidates and strengthens SMIC's R&D and manufacturing capabilities for silicon-based sensors, thru-silicon-via (TSV) technology ...The move is in line with a longstanding differentiation strategy promoted by its CEO, T.Y.Chiu. "
- Austriamicrosystems"
  - Invested more than 25 million euros in creating 3D IC production capacity at its wafer fab near Graz, Austria.
  - At the time of its announcement, AMS said it made the investment because of "soaring demand" for stacked-die services based on TSV integration it has developed. The AMS 3D IC production line will be fully operational by the end of 2013 and initially will produce devices for medical imaging and mobile phones.

- Total system cost, IC cost, development costs and their amortization over production volumes, risk of failure, time to market, and, last but not least, the technical requirements of increasingly complex solutions.

References

https://www.google.com/url?sa=t&rct=j&q=&esrc=s&source=web&cd=6&ved=0CDcQFjAF&url=http%3A%2F%2Finst.eecs.berkeley.edu%2F~cs250%2Ffa10%2Flectures%2Flec08.pdf&ei=P596UtaxKsmjrQGdrID4AQ&usg=AFQjCNFhxYqJBri5Q-BB4btnZ3gwQaWDIQ&sig2=FjNSGKT29dRexihpcQehOA Lecture 8, Memory, Berkeley.

https://www.google.com/url?sa=t&rct=j&q=&esrc=s&source=web&cd=4&ved=0CEsQFjAD&url=http%3A%2F%2Fwww-isl.stanford.edu%2F~abbas%2Fpapers%2Fconf%2520The%2520Prospect%2520of%25203D-IC.pdf&ei=PG96Ut62G4XPqQHD1YCYDw&usg=AFQjCNGVqAgc2gcWYrdzIv0U_dMs_xSf3g&sig2=-MgBx7nFg9MpvmqAfQ9hVA&cad=rja "The prospect of 3D-IC", Stanford University.

http://www.eetimes.com/document.asp?doc_id=1279540 "2D 2.5 VS 3D", EE Times


Questions?


Thank you.