Review

1. Explain each transistor operating region.
2. What is pinch-off?
3. How does body bias work?
4. What is velocity saturation?
5. What is sub-threshold operation?
Lecture plan

1. Device trends
2. Fabrication
3. Layout and design rules
4. Packaging and board-level integration
5. Homework
Process variation

Given our current knowledge of transistor operation, what impact will variation in
- dopant concentrations,
- oxide thickness,
- transistor width, and
- interconnect width
have?
FinFETs

From Freescale.
Carbon nanotubes and nanowires

From AIST.
Quantum cellular automata

- Binary information encoded in device configuration.
- Signals are propagated through nearest neighbor interaction.

From Professor Xiaobo Sharon Hu.
Quantum cellular automata arithmetic-logic unit

From Professor Xiaobo Sharon Hu.
Single-electron tunneling transistors

Source (S) | Optional second gate (G2) | Junctions | Island | Gate (G) | Drain (D) | Insulator

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Common problems

- Difficult to get high-quality devices where they are needed.
- High susceptibility to thermal noise.
- High susceptibility to charge trap offsets.
- Low gain.
What does the future hold

- CMOS for another decade or so, until devices consist of a small integer number of atoms.
- Nobody knows what comes next.
- Nothing? New device technology?
- Implications for information technology?
Lecture plan

1. Device trends
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Review

1. List a few different alternatives to CMOS for use in digital systems.
2. Indicate their advantages and disadvantages relative to CMOS.
NMOSFET

[Diagram of NMOSFET structure with labels for Polysilicon, Al, SiO₂, n⁺, n⁻, p⁻, n-well, p-substrate, and D⁺ symbols]
Insulator properties

- Low-$\kappa$: reduced capacitance, useful for isolating wires.
- High-$\kappa$: increased capacitance, useful for maintaining $k$ despite increased gate thickness.
High-level fabrication process overview

Dual-Well Trench-Isolated CMOS Process
Schematic of circuit to fabricate
Layout of circuit to fabricate
Overview of fabrication process

- **Device trends**
- **Fabrication**
- Layout and design rules
- Packaging and board-level integration

Homework

Overview of fabrication process:

1. **Oxidation**
2. **Photoresist coating**
3. **Stepper exposure**
4. **Photoresist development**
5. **Acid etch**
6. **Spin, rinse, dry**
7. **Process step**

Typical operations in a single photolithographic cycle (from [Fullman]).
FIGURE 1.37. General semiconductor production process.

SiO$_2$ patterning

(a) Silicon base material

(b) After oxidation and deposition of negative photoresist

(c) Stepper exposure

(d) After development and etching of resist, chemical or plasma etch of SiO$_2$

(e) After etching

(f) Final result after removal of resist
Etching

Fig. 2.5  Etching profiles obtained with (a) isotropic wet chemical etching and (b) dry anisotropic etching in a plasma or reactive-ion etching system.

Summary of processing steps

1. Define active areas.
2. Etch and fill trenches.
3. Implant well regions.
4. Deposit and pattern polysilicon/metal gate layer.
5. Implant source and drain regions, and substrate contacts.
6. Create contacts and via windows.
7. Deposit and pattern metal layers.
Step 1: epitaxial layer
Step 2: gate oxide and sacrificial nitride layer deposition
Step 3: plasma etching
Step 4: trench filling, CMP, etching, SiO$_2$ deposition
Step 5: n-well and $V_{Tn}$ adjustment implants
Step 6: p-well and $V_{Tp}$ adjustment implants
Step 7: polysilicon/metal deposition and etch
Step 8: $n^+$ and $p^+$ source, drain, and poly implantation
Step 9: SiO₂ deposition and contact etch
Step 10: deposit and pattern first interconnect layer
Step 11: deposit SiO$_2$, etch contacts, deposit and pattern second interconnect layer
Interconnect layers
Al vs. Cu

- For Al, can deposit and etch metal layers.
- Cu alloys with Si.
- Cannot safely deposit Cu directly on Si.
- Cu difficult to controllably etch.
- Instead, build SiO$_2$ shield and etch contact regions.
Damascene process

- Oxide deposition
  - Stud lithography and reactive ion etch
  - Wire lithography and reactive ion etch

- Stud and wire metal deposition
  - Metal chemical-mechanical polish

From IBM.
Interconnect layers

[1] IBM Corp.'s new CMOS 75 process for manufacturing ICs uses copper for its six levels of interconnections, and has effective transistor channel-lengths of only 0.12 µm. It is the first commercial fabrication process to use copper wires (see “The Damascus connection,” p. 25).
Lecture plan

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Layout production

- Must define 2-D structure for each mask/layer.
- Initial topology planning often done.
- Can be partially or fully automated.
- Must adhere to design rules.
Stick diagrams

Stick diagram of inverter
Faults and variation

- Clearly cannot have two wires crossing each other.
- Variation imposes further constraints.
Possible faults

![Circuit Diagram](image)
Possible faults

![Diagram showing possible fault types involving VDD and VSS connections with bridging fault annotated.](image)
Possible faults

\[ V_{DD} \]

\[ V_{SS} \]

\[ a \]

\[ b \]

\[ z \]

\[ V_{DD} \]

\[ a \]

\[ b \]

\[ z \]
Possible faults

- Stuck-open fault

Diagrams showing wiring and connections.
Possible faults
Possible faults

\[ V_{DD} \]

\[ V_{SS} \]

\[ a \]

\[ b \]

\[ z \]

stuck-at fault

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Possible faults

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Design rules

Summary

- Automatically-checked layout rules.
- Reduce fault probabilities.
- Generally regarded as necessary.

Caveats

- Recent studies show many rules are not beneficial.
- Interaction range is increasing relative to $\lambda$.
  - Complicates design rules, making manual comprehension difficult.
- Design rule checking can be slow.
### Meanings of colors in layouts

<table>
<thead>
<tr>
<th>Layer</th>
<th>Color</th>
<th>Representation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Well (p,n)</td>
<td>Yellow</td>
<td></td>
</tr>
<tr>
<td>Active Area (n+,p+)</td>
<td>Green</td>
<td></td>
</tr>
<tr>
<td>Select (p+,n+)</td>
<td>Green</td>
<td></td>
</tr>
<tr>
<td>Polysilicon</td>
<td>Red</td>
<td></td>
</tr>
<tr>
<td>Metal1</td>
<td>Blue</td>
<td></td>
</tr>
<tr>
<td>Metal2</td>
<td>Magenta</td>
<td></td>
</tr>
<tr>
<td>Contact To Poly</td>
<td>Black</td>
<td></td>
</tr>
<tr>
<td>Contact To Diffusion</td>
<td>Black</td>
<td></td>
</tr>
<tr>
<td>Via</td>
<td>Black</td>
<td></td>
</tr>
</tbody>
</table>
### Layout layers

<table>
<thead>
<tr>
<th>Layer Description</th>
<th>Representation</th>
</tr>
</thead>
<tbody>
<tr>
<td>metal</td>
<td>m1, m2, m3, m4, m5</td>
</tr>
<tr>
<td>well</td>
<td>nw</td>
</tr>
<tr>
<td>polysilicon</td>
<td>poly</td>
</tr>
<tr>
<td>contacts &amp; vias</td>
<td>ct, v12, v23, v34, v45</td>
</tr>
<tr>
<td>active area and FETs</td>
<td>ndif, pdif, nfct, pfct</td>
</tr>
<tr>
<td>select</td>
<td>nplus, pplus, prb</td>
</tr>
</tbody>
</table>

- **Homework:**

- **Digital Integrated Circuits**

- **Fabrication**

- **Device trends**

- **Layout and design rules**

- **Packaging and board-level integration**

- **Robert Dick**
Intra-layer design rules

- Same Potential
  - Well
    - 0 or 6
    - 10
  - Contact or Via Hole
    - 2
  - Select
    - 2

- Different Potential
  - Well
    - 9
  - Polysilicon
    - 2
  - Active
    - 3
  - Metal1
    - 3
  - Metal2
    - 4
Via design rules
Layout editor
Design rule checker

poly_not_fet to all_diff minimum spacing = 0.14 um.
Lecture plan

1. Device trends
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Packaging requirements

- **Electrical**: Good insulators and conductors.
- **Mechanical**: Reliable, doesn’t stress IC.
- **Thermal**: Low thermal resistance to ambient. In some cases, consistency more important.
- **Cost**.
Wire bonding
Tape automated bonding
Tape automated bonding die attachment

Diagram showing:
- Film + Pattern
- Solder Bump
- Die
- Substrate
Flip-chip bonding

![Flip-chip bonding diagram]

- Solder bumps
- Interconnect layers
- Substrate
- Die
Through-hole PCB mounting
Surface mount
Example package types
Chip cap

- Cooling medium (air or liquid)
- Chip cap
- Hierarchial branched channels
- Thermal interface material (paste)
- Chip
- Chip carrier
- Electrical contacts
Heat pipe
Heat pipe details

Heat pipe thermal cycle
1) Working fluid evaporates to vapour absorbing thermal energy.
2) Vapour migrates along cavity to lower temperature end.
3) Vapour condenses back to fluid and is absorbed by the wick, releasing thermal energy
4) Working fluid flows back to higher temperature end.
## Example of variation in package parameters

<table>
<thead>
<tr>
<th>Type</th>
<th>C (pF)</th>
<th>L (nH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>68-pin plastic DIP</td>
<td>4</td>
<td>35</td>
</tr>
<tr>
<td>68-pin ceramic DIP</td>
<td>7</td>
<td>20</td>
</tr>
<tr>
<td>256-pin PGA</td>
<td>5</td>
<td>15</td>
</tr>
<tr>
<td>Wire bond</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Solder bump</td>
<td>0.5</td>
<td>0.1</td>
</tr>
</tbody>
</table>
System-on-chip

- Instead of integrating more ICs, put more on an IC.
- Advantages: Lower cost per device, compact.
- Disadvantages: Requires integration of devices fabricated with different processes.
Move from lead solder

- Tin–lead solder was commonly used.
- Lead is toxic, accumulates in the body, and is difficult to dispose of.
- Pure tin works in the short term.
- May be acceptable as solder in the long term.
- Problems with plating.
Tin whiskers

Screw dislocations, primarily caused by plating.
Multi-chip modules

- Better than board-level integration.
- Integrate multiple processes.
- Somewhat compact.
- Expensive.
Multiple active layer 3-D integration

Potential for thermal problems.
Heterogeneous system 3-D integration

Integrate

- Logic.
- Memory.
- Analog.
- Research on discrete components (with soldering).
Microchannel cooling

Credit to David Atienza at EPFL.
Vapor-phase cooling

Credit to Michael J. Ellsworth, Jr. and Robert E. Simons at IBM.
Summary

- CMOS is the most economical way to build digital logic now, but potential alternatives being developed.
- Fabrication process is essentially repeated deposition, masking, etching, and polishing steps to dope and build material layers.
- Al → Cu.
- SiO$_2$ → High-κ and Low-κ.
- Cu interconnects use damascene process.
- Poly-Si → metal.
Upcoming topics

- MOSFET dynamic behavior.
- Wires.
- CMOS inverters.
Lecture plan

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Homework assignment

- 24 September: Homework 1.
- 3 October: Lab 2.