Digital Integrated Circuits – EECS 312

http://robertdick.org/eecs312/

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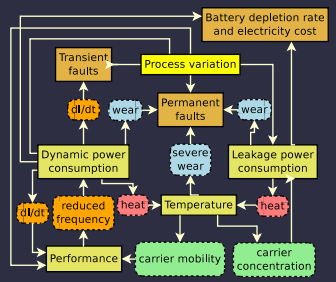
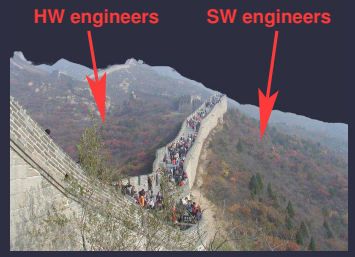
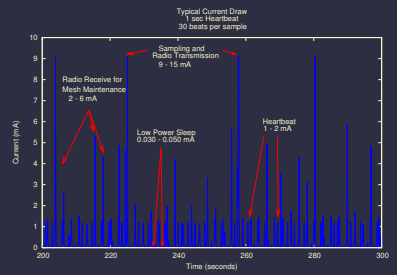
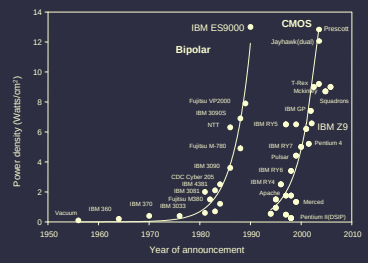








Lecture plan

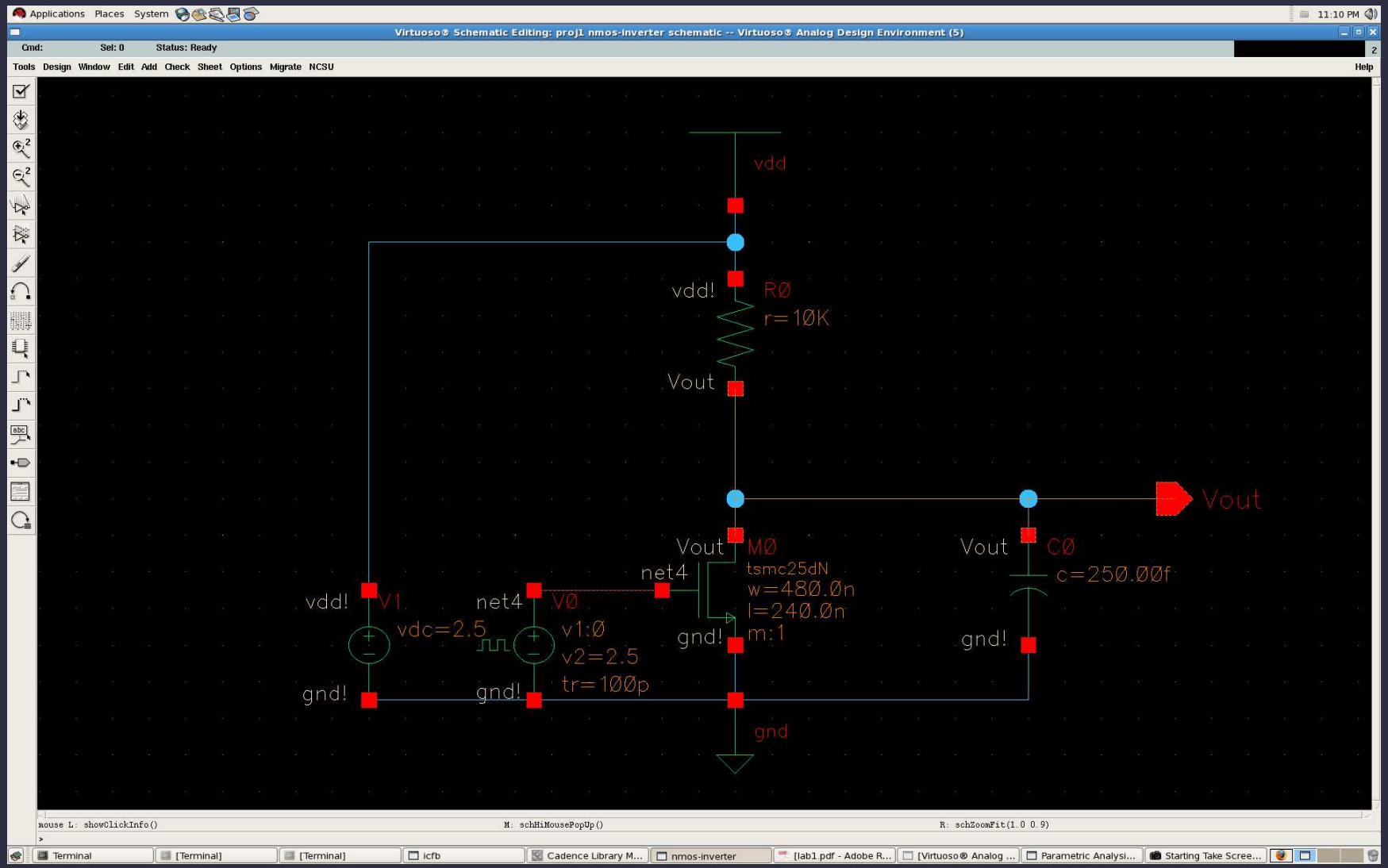
1. Lab one
2. Desired transistor behavior
3. Homework

Lab one challenges

- Learning to use the tools (last Friday).
- Understanding the circuits used in the lab (today).
- A note on the CAD tools market.

Derive and explain.

NMOS inverter schematic



Resistance

$$R = \rho \frac{L}{W} \quad (1)$$

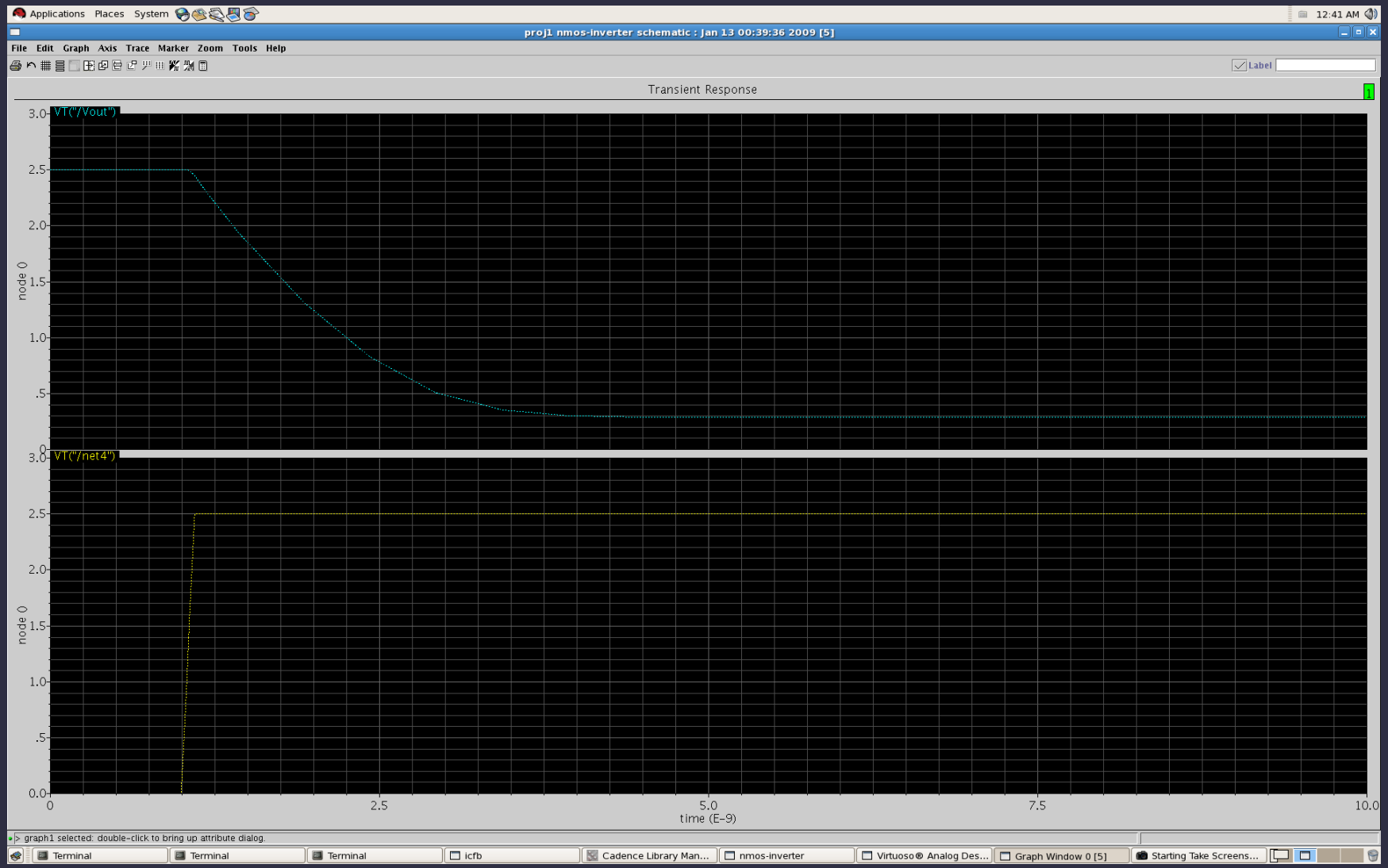
$$G = \sigma \frac{W}{L} \quad (2)$$

$$G = \frac{1}{R} \quad (3)$$

$$\sigma = \frac{1}{\rho} \quad (4)$$

- Assuming fixed height.
- R: resistance.
- ρ: resistivity.
- L: length.
- W: width.
- G: conductance.

NMOS inverter simulation results



RC network

$$V_c = V_{final} + (V_{init} - V_{final})\, e^{\frac{-t}{\tau}} \quad (5)$$

$$\tau = RC \quad (6)$$

NMOS→CMOS inverter

- How does structure change?
- What impact does transistor width have? Why different widths?
- How does response change?
- What are advantages?
- What are disadvantages?

Derive and explain.

Review questions and note

- What are digital systems built from?
- What gate properties are required for use in digital systems? Why?
- What have the major effects of process scaling been? What challenges does it face in the future?
- What are the physical structures and symbols of (N/P)MOSFETs? How do they work?

Lecture plan

1. Lab one
2. Desired transistor behavior
3. Homework

Desired and actual properties of transistors

Desired properties

- Perfect digital signal transfer.
- No parasitics.

Actual properties

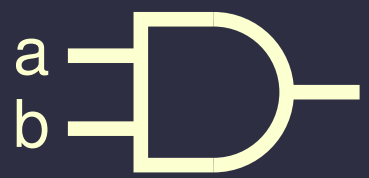
- Imperfect transfer function.
  - Fortunately, has gain and capable of signal regeneration (restoration).
- Parasitic resistance and capacitance.
- Leakage.

Brief introduction to Boolean algebra

- The only values are 0 (or false) and 1 (or true).
- One can define operations/functions/gates.
  - Boolean values as input and output.
- A truth table enumerates output values for all input value combinations.

AND

a	b	a $\wedge$ b
0	0	0
0	1	0
1	0	0
1	1	1



a *AND* b = a $\wedge$ b = a b

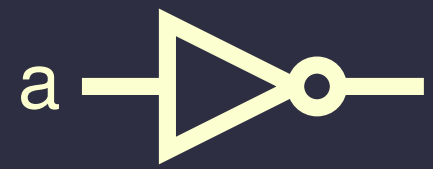
OR

a	b	a + b
0	0	0
0	1	1
1	0	1
1	1	1

$$a \; \textit{OR} \; b = a \vee b = a + b$$

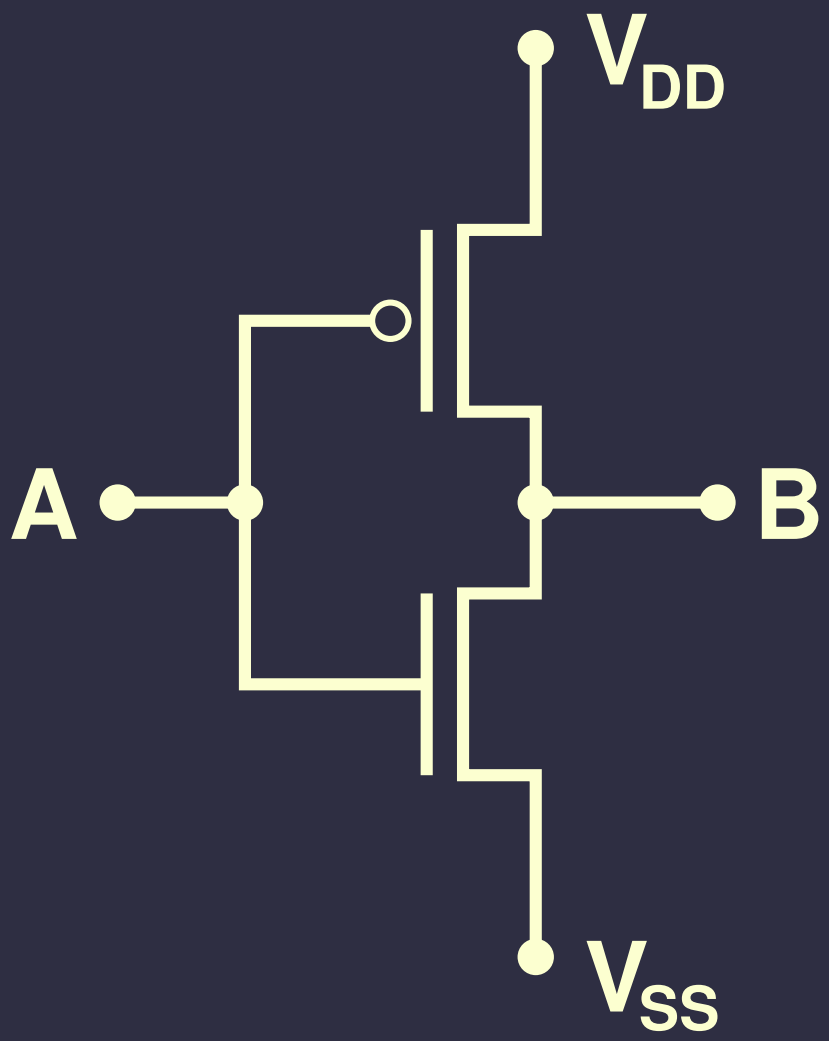
NOT

a	$\overline{a}$
0	1
1	0

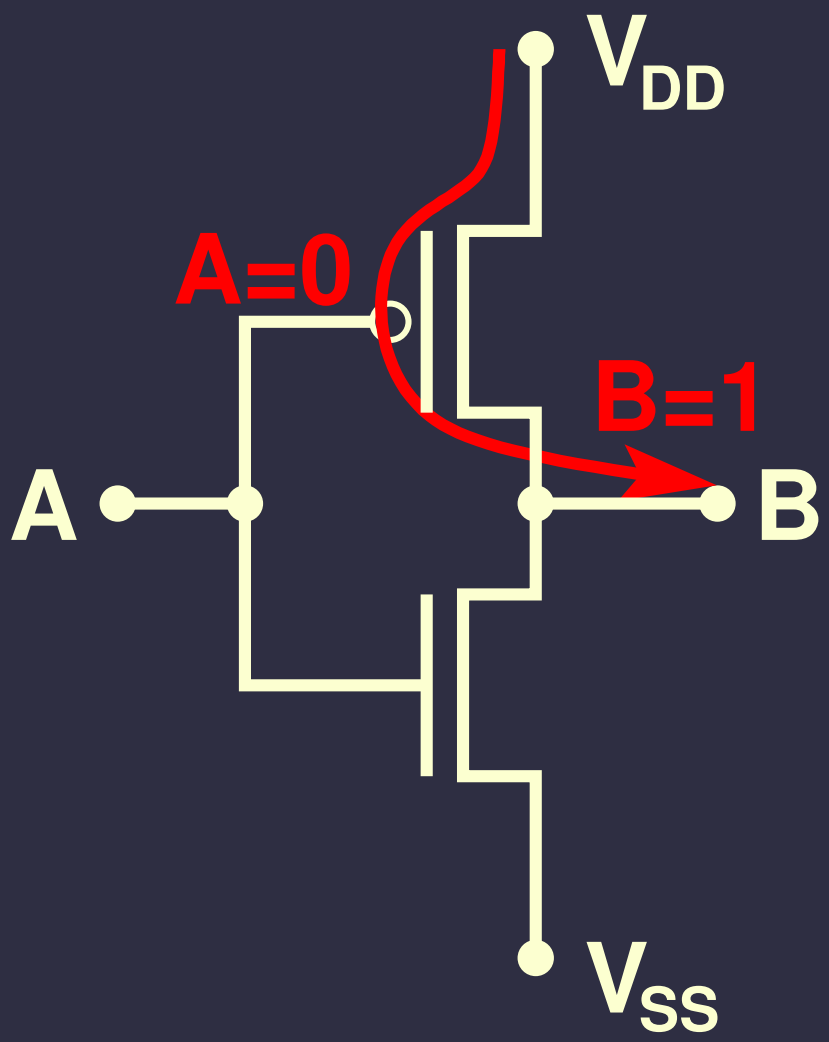


$$NOT\ \mathrm{a} = \overline{\mathrm{a}}$$

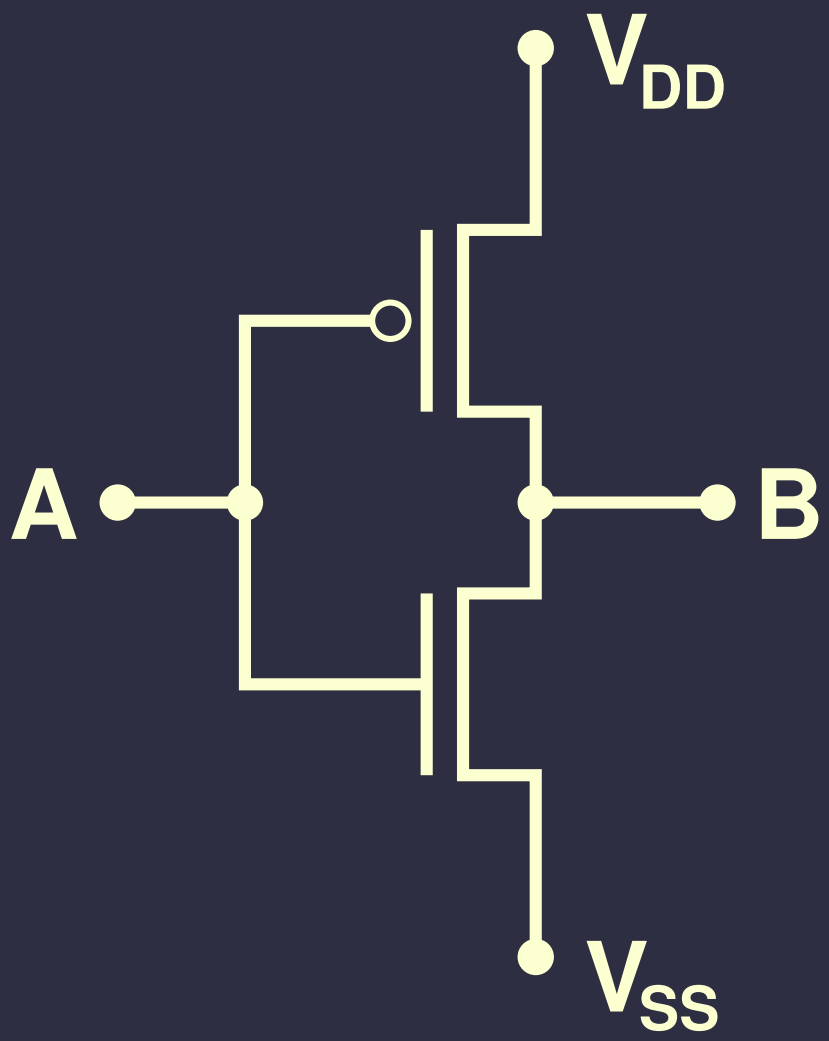
CMOS inverter operation



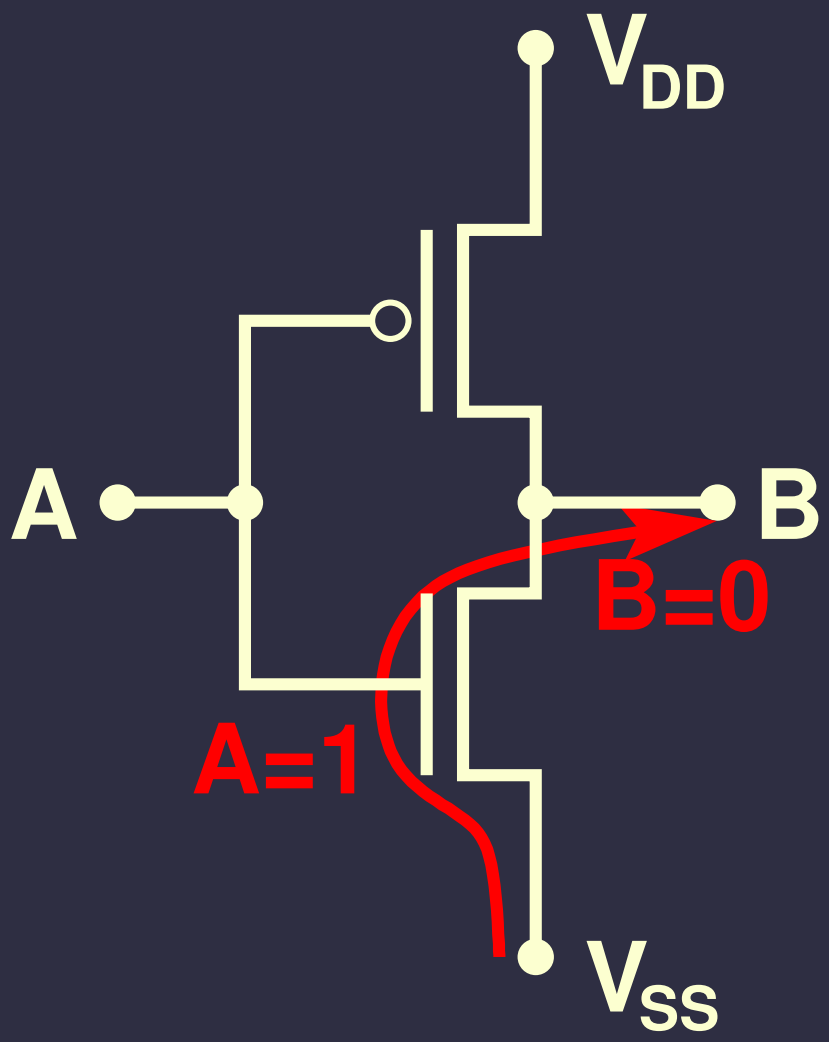
CMOS inverter operation



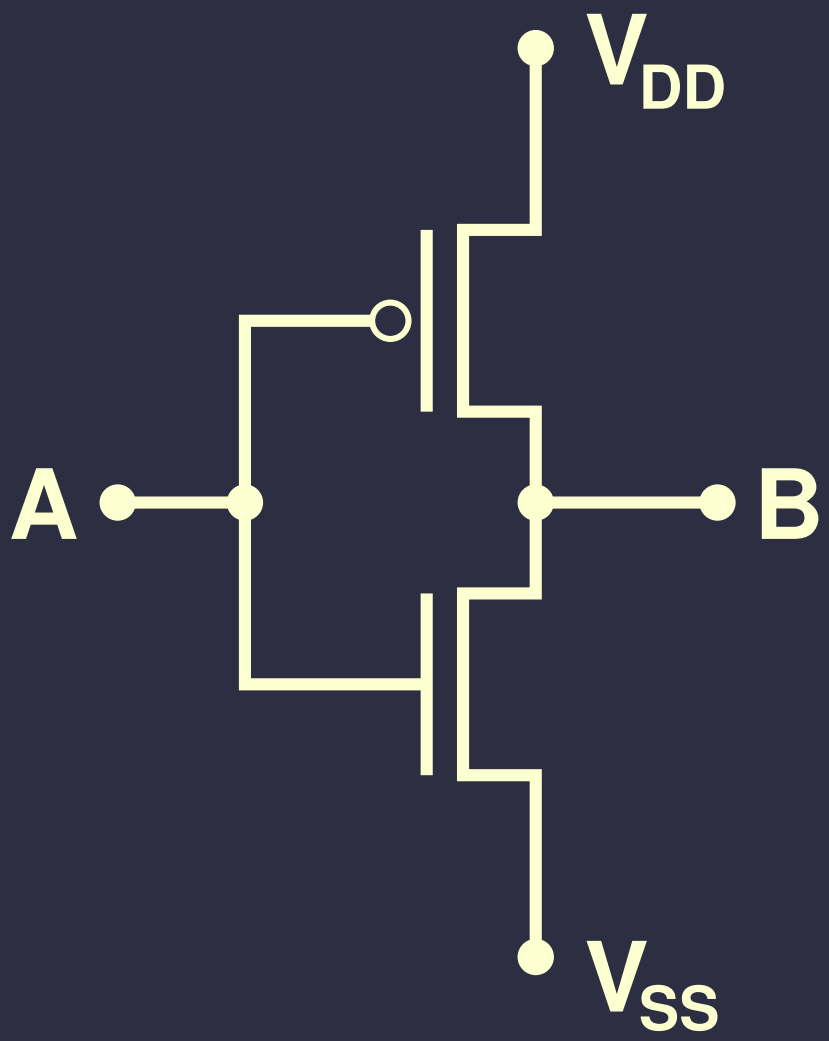
CMOS inverter operation



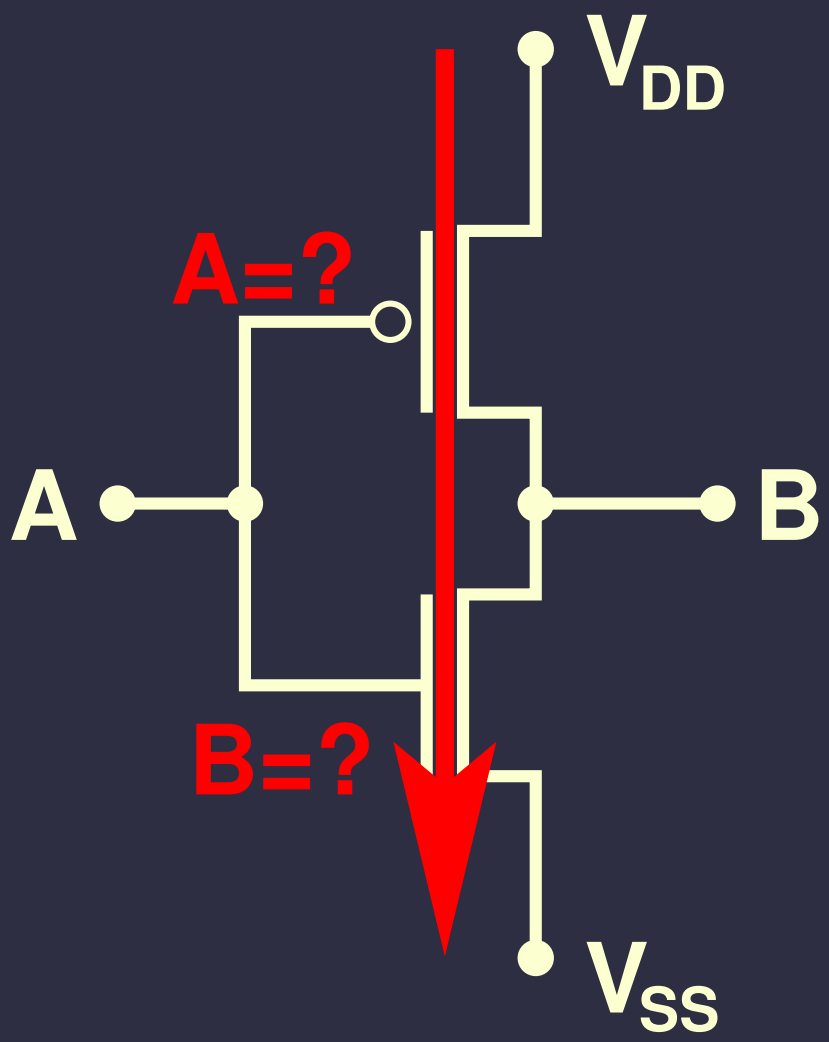
CMOS inverter operation



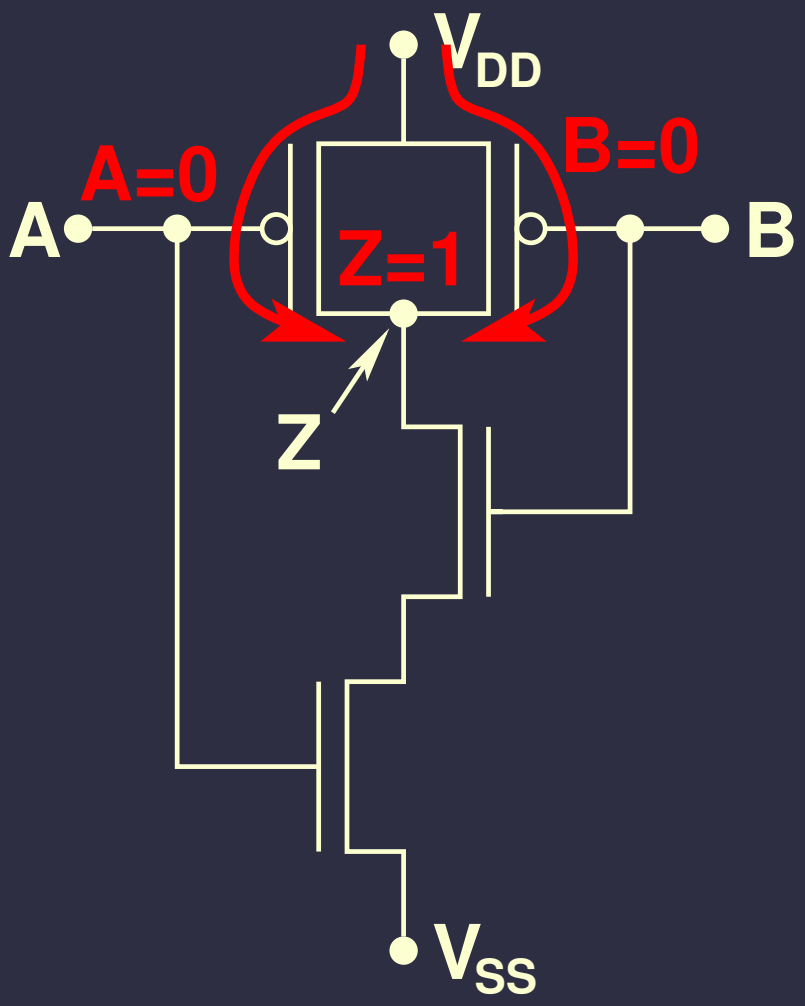
CMOS inverter operation



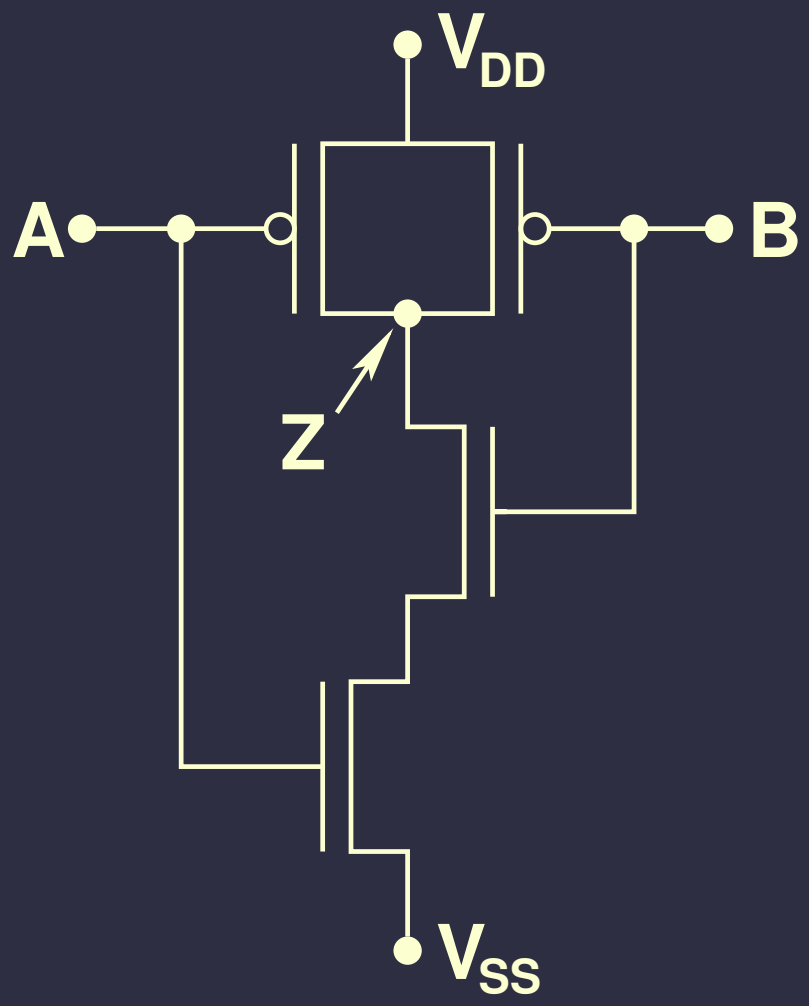
CMOS inverter operation



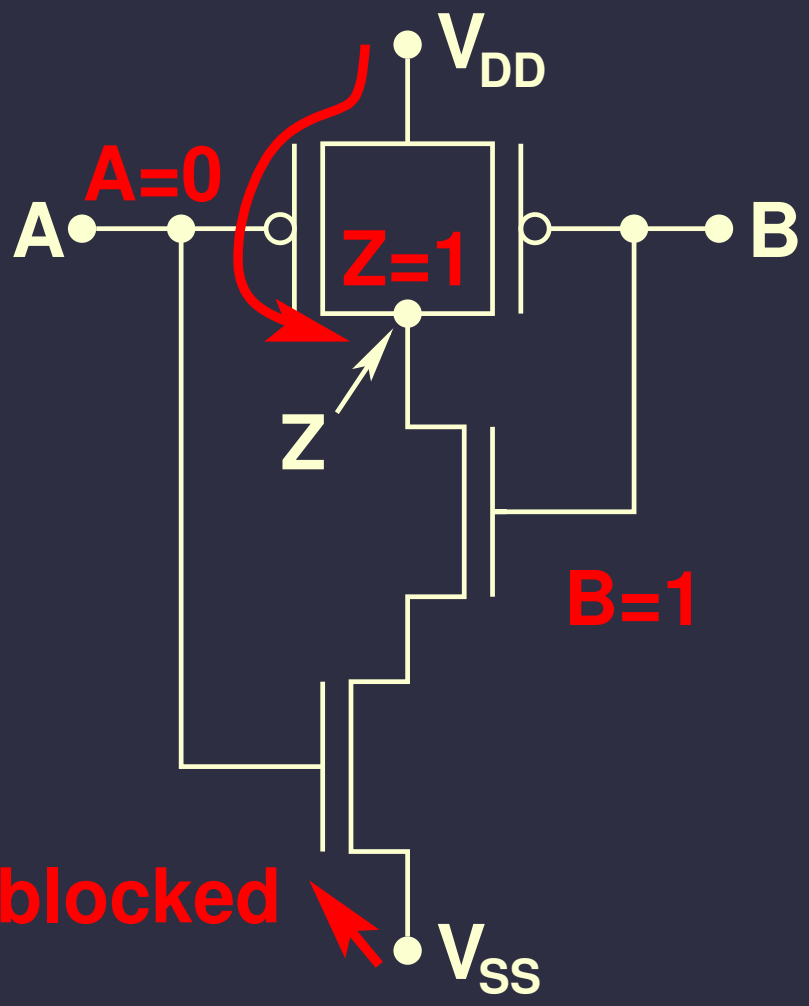
NAND operation



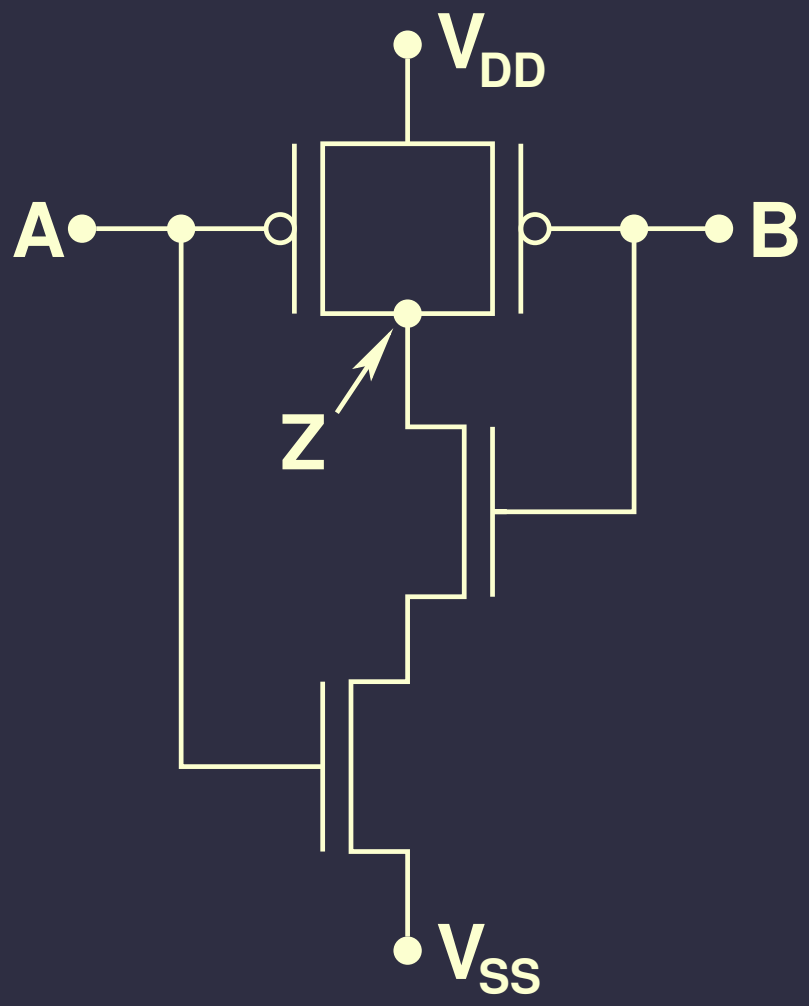
NAND operation



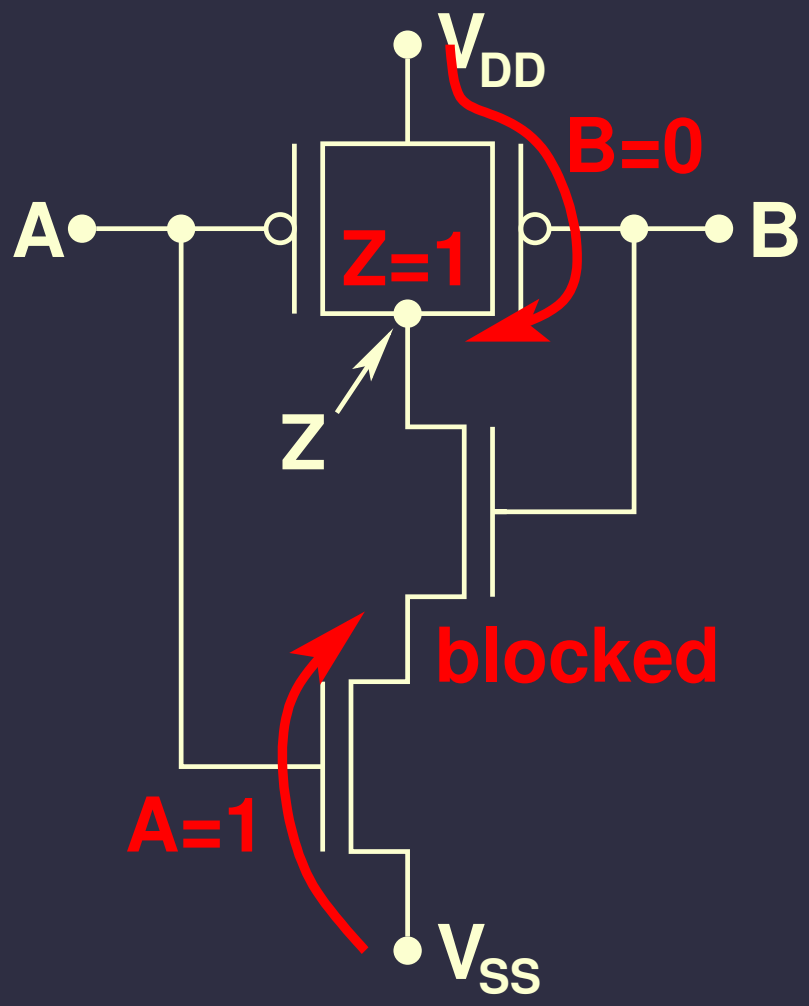
NAND operation



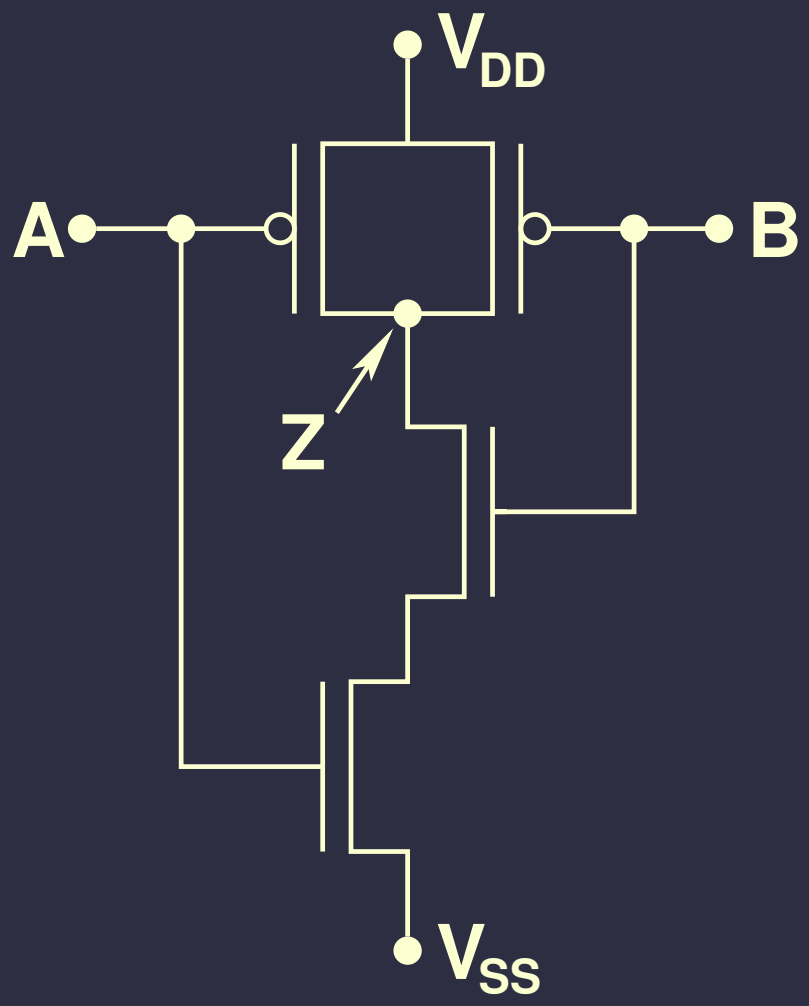
NAND operation



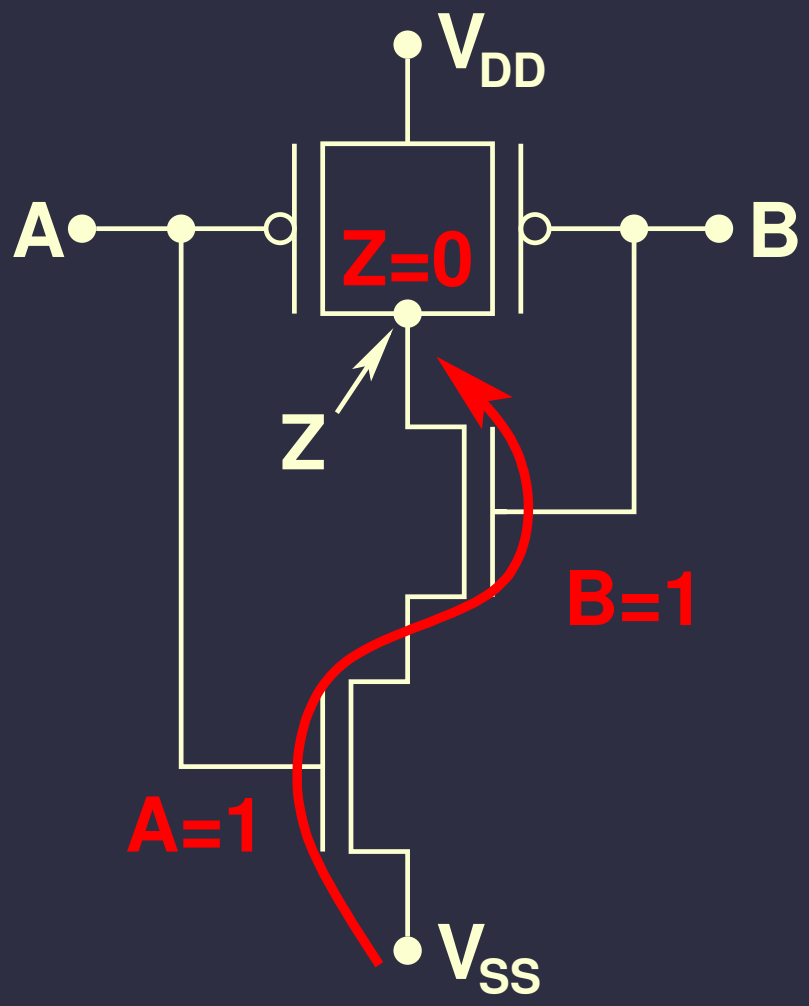
NAND operation



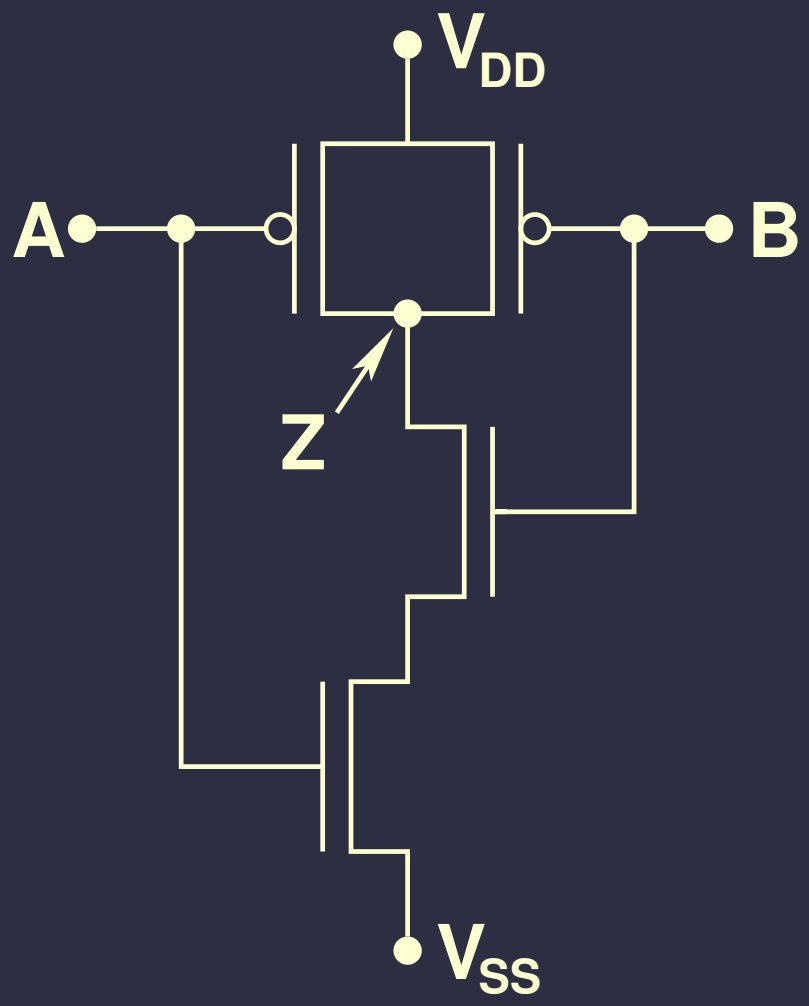
NAND operation



NAND operation

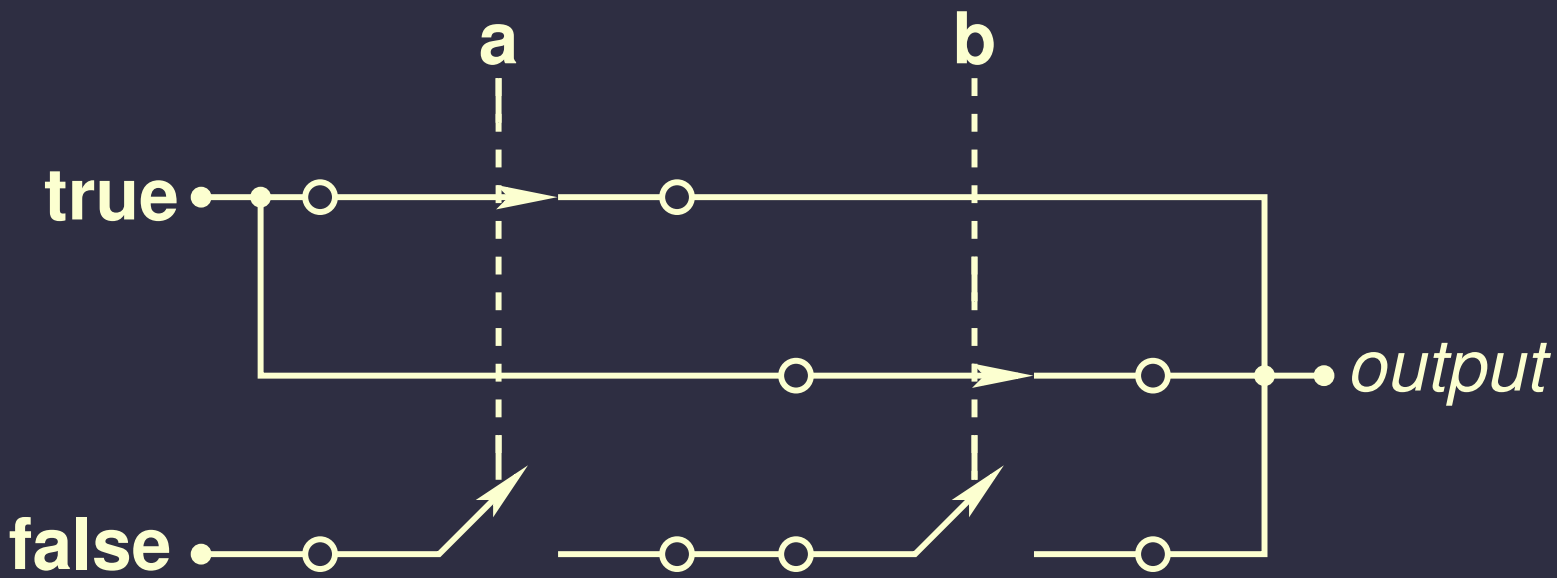


NAND operation



NAND gate

- Therefore, *NAND* and *NOR* gates are used in CMOS design instead of *AND* and *OR* gates



NAND gate

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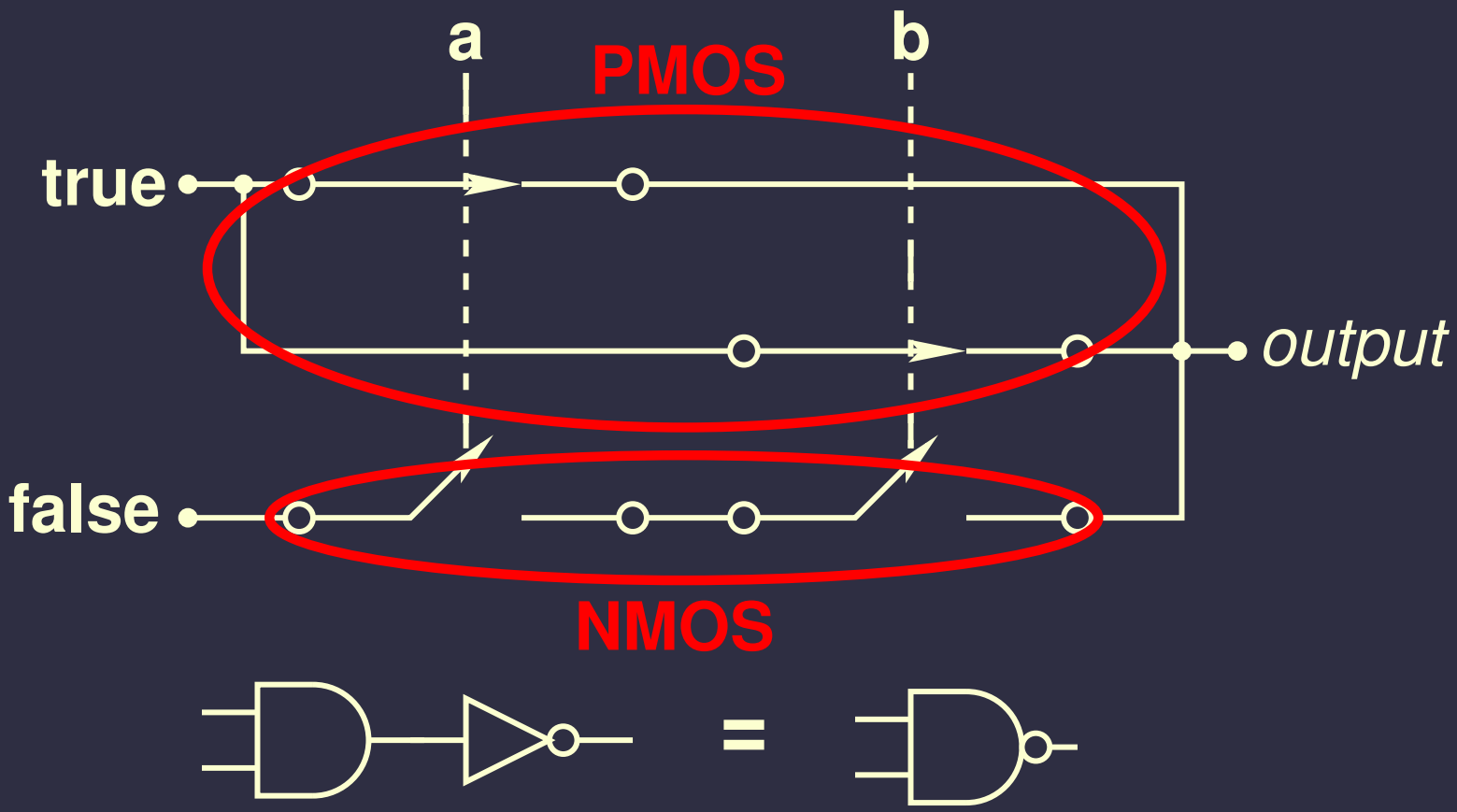
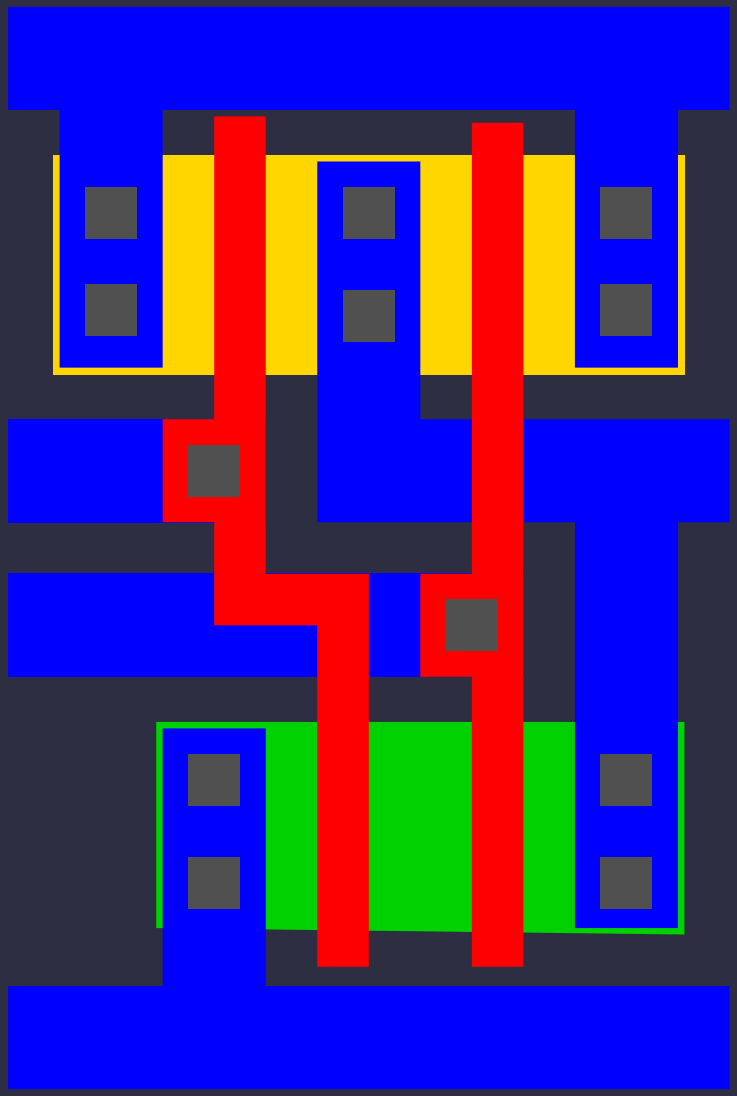
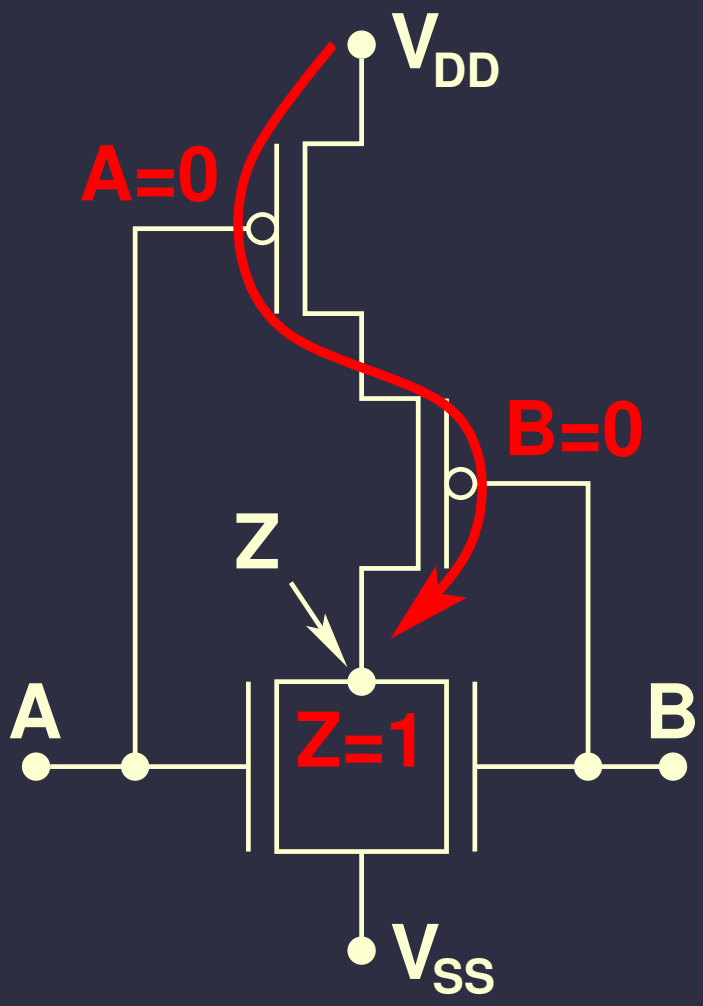


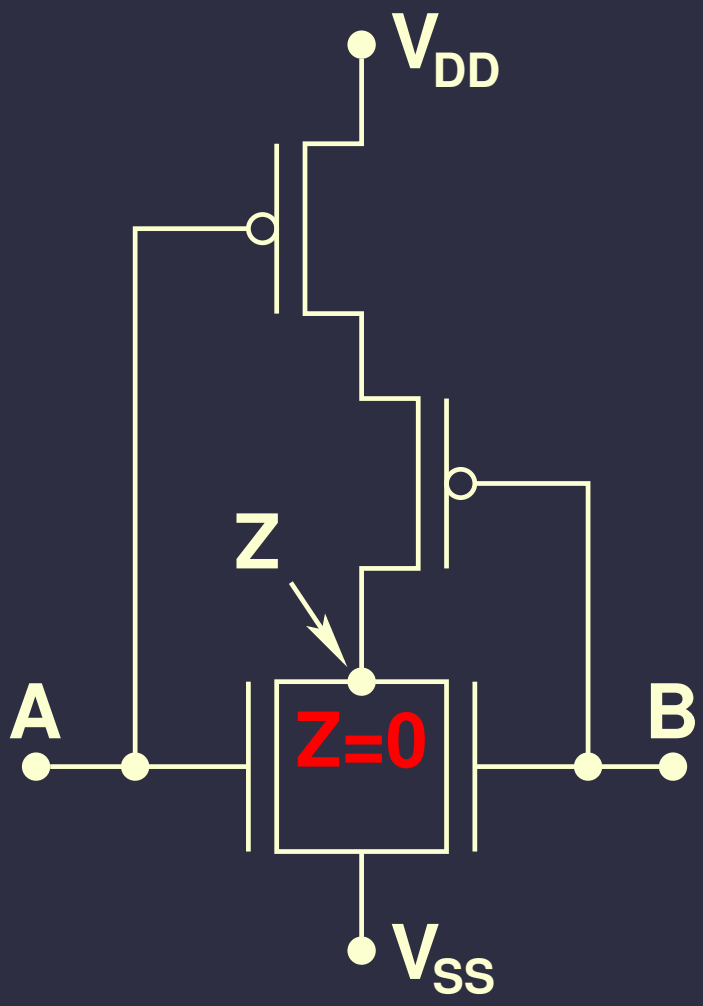
NAND layout



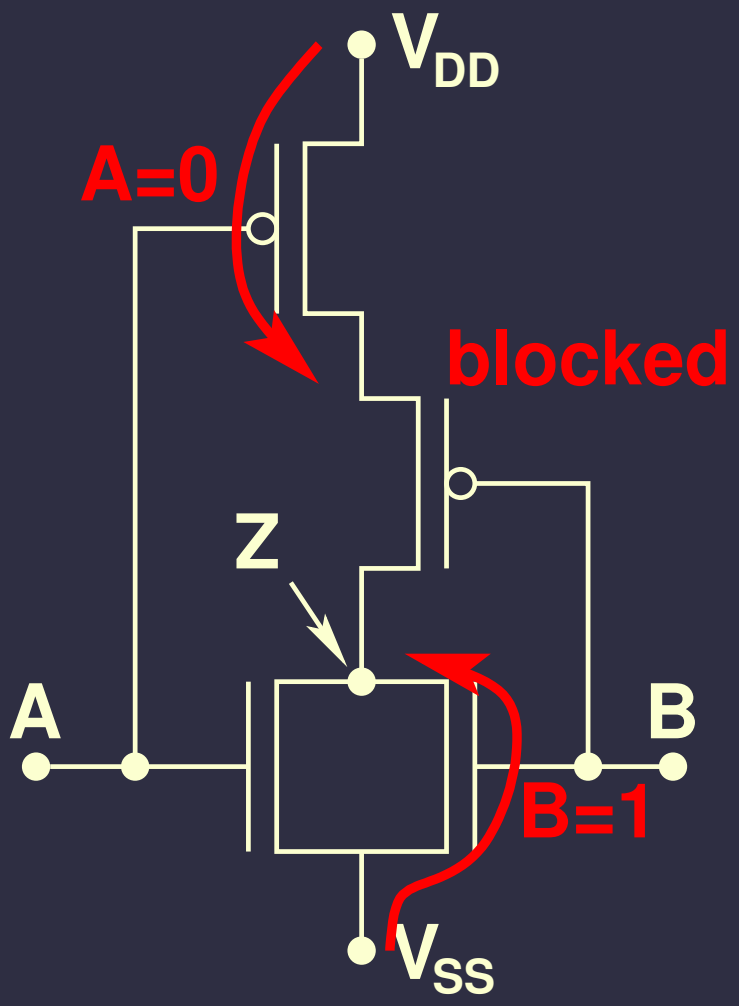
NOR operation



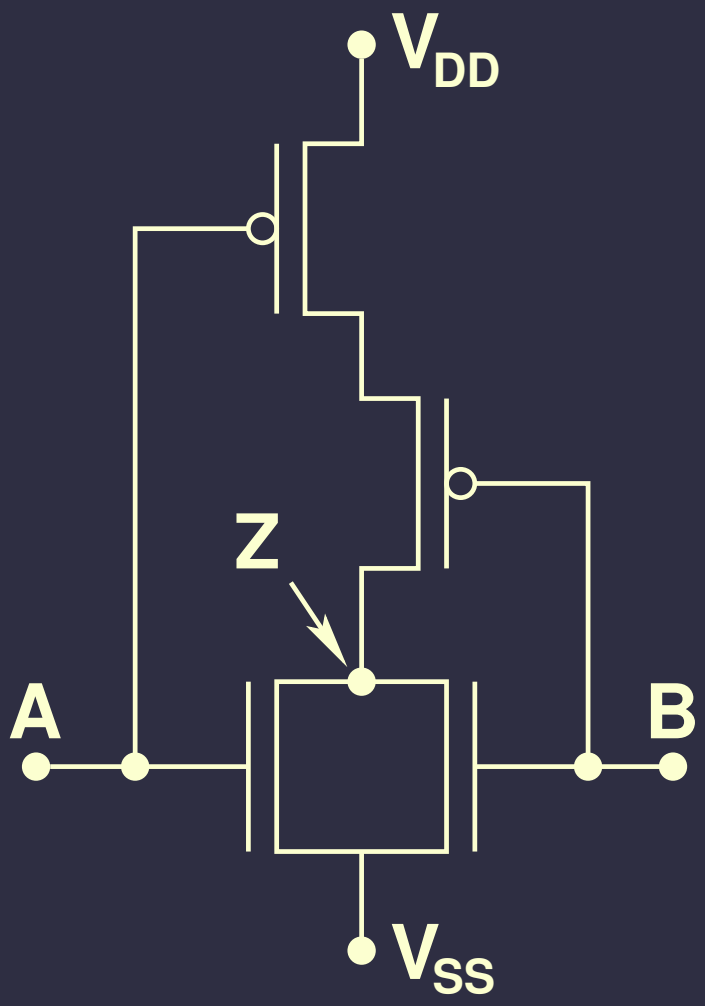
NOR operation



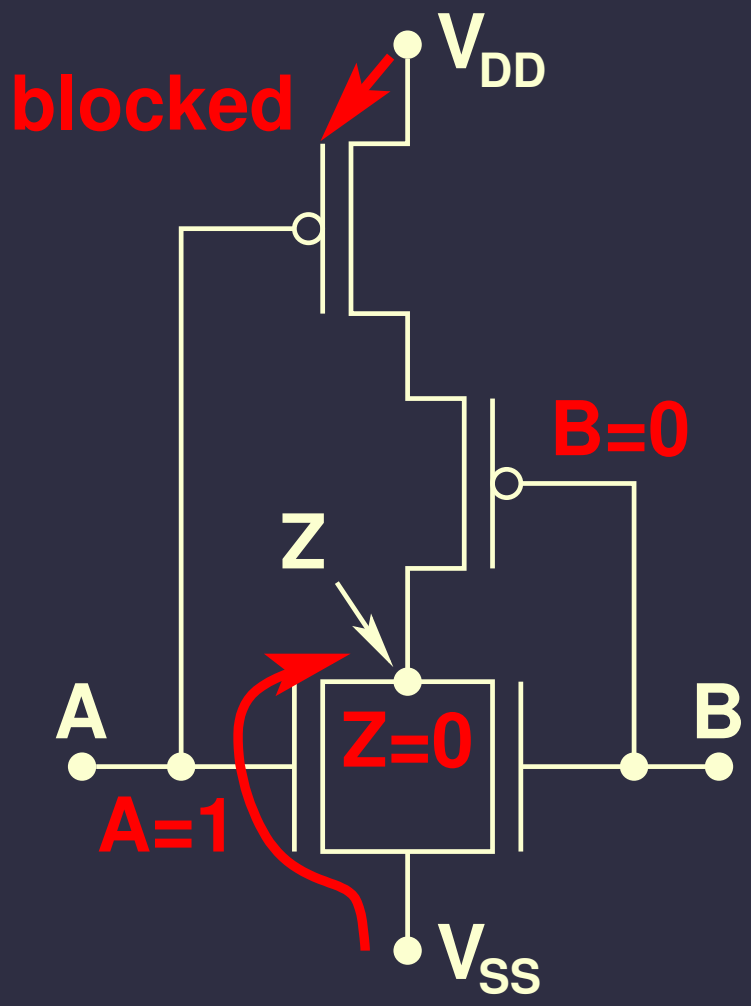
NOR operation



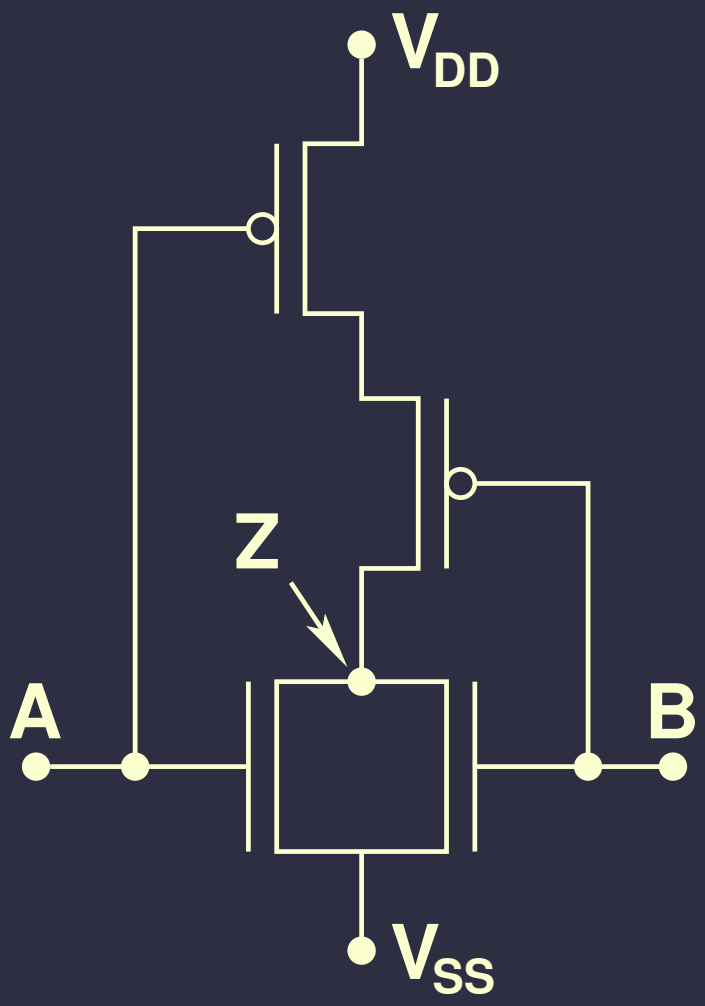
NOR operation



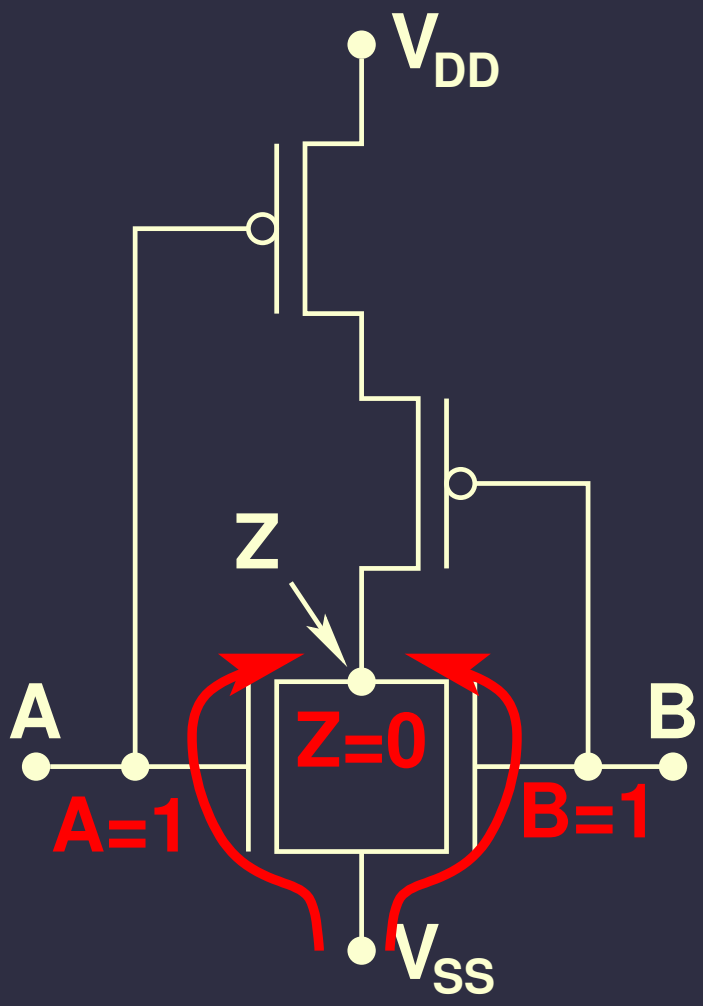
NOR operation



NOR operation



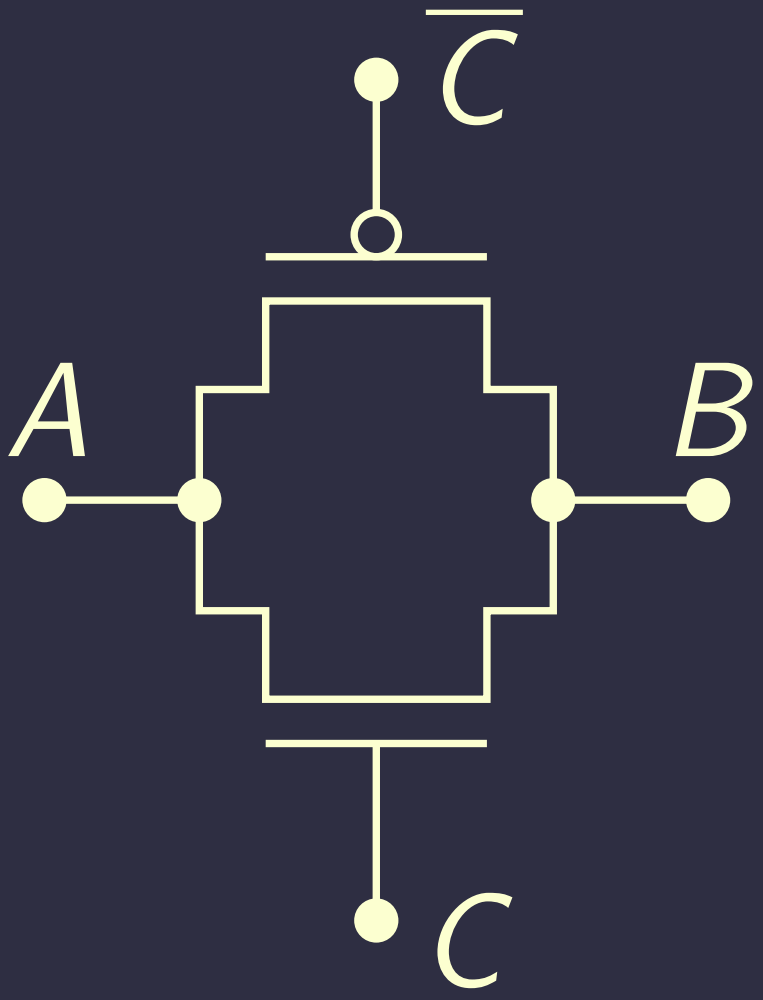
NOR operation



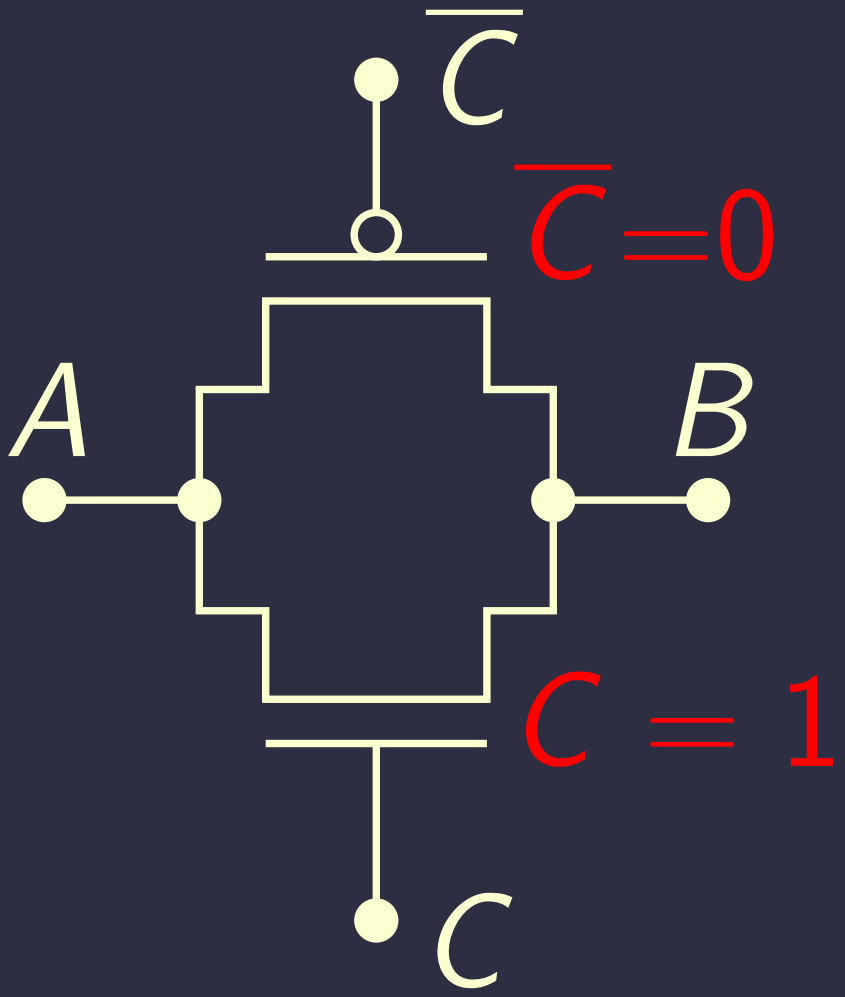
CMOS transmission gates (switches)

- NMOS is good at transmitting 0s
  - Bad at transmitting 1s
- PMOS is good at transmitting 1s
  - Bad at transmitting 0s
- To build a switch, use both: CMOS

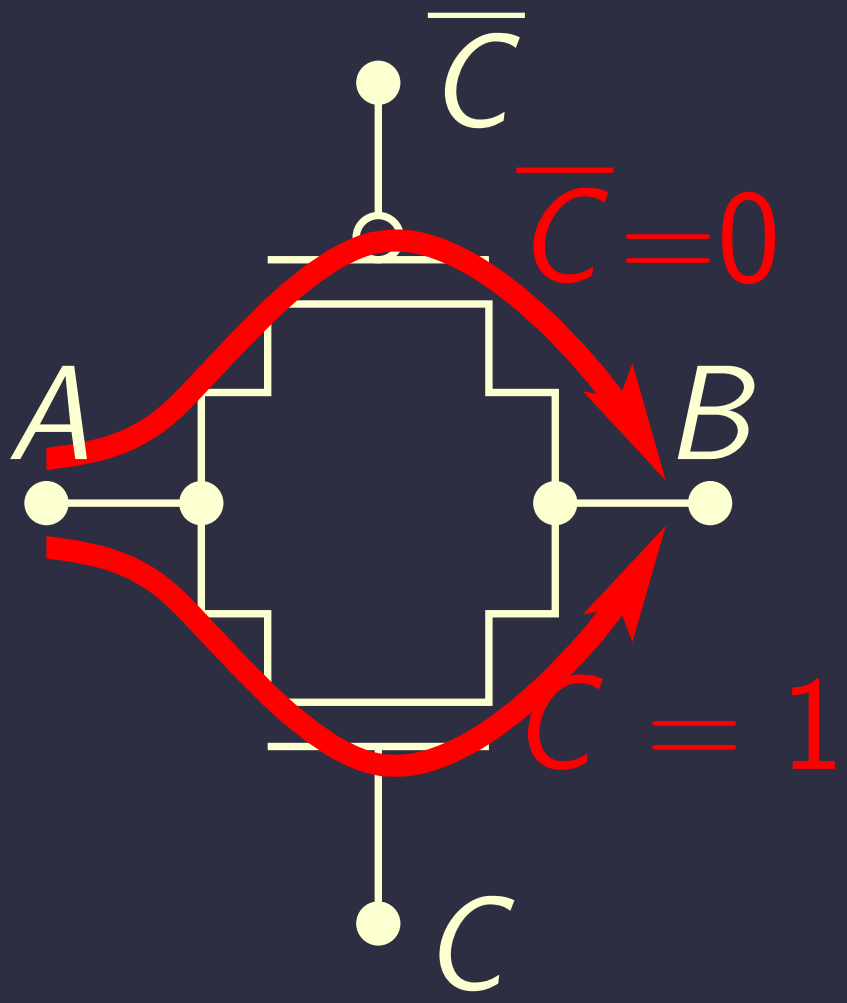
CMOS transmission gate (TG)



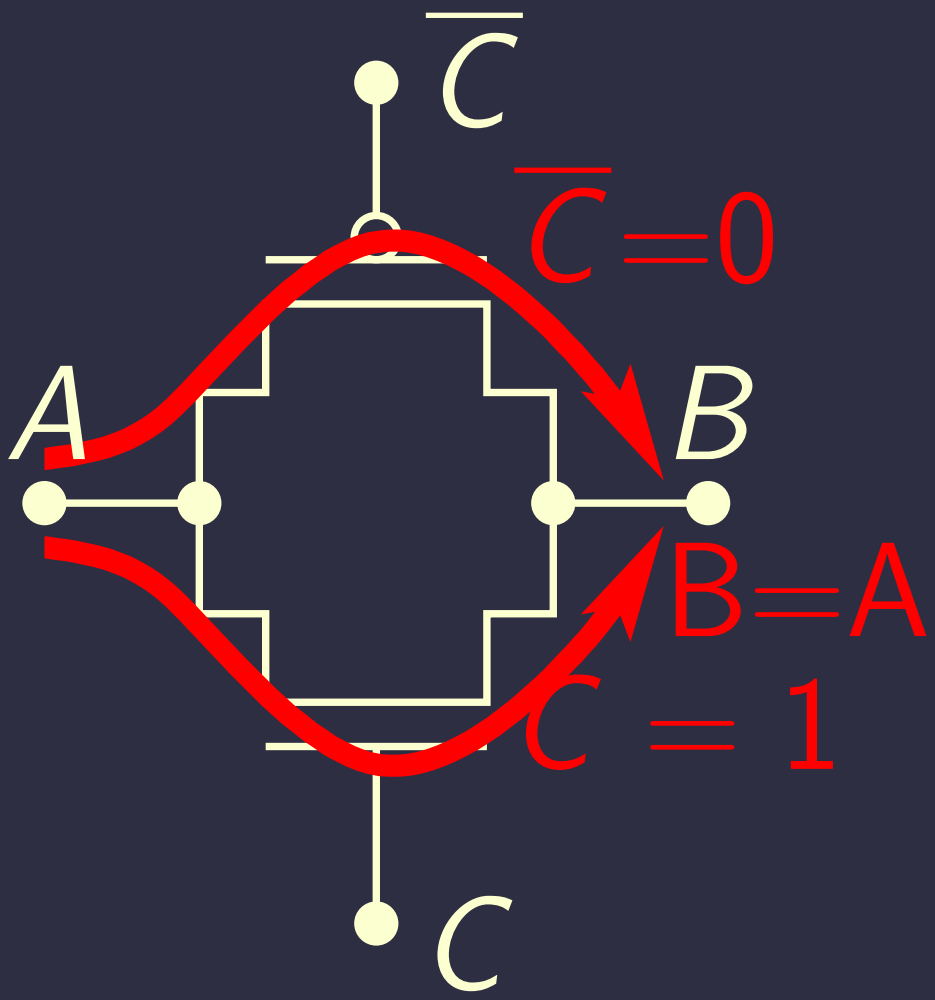
CMOS transmission gate (TG)



CMOS transmission gate (TG)



CMOS transmission gate (TG)



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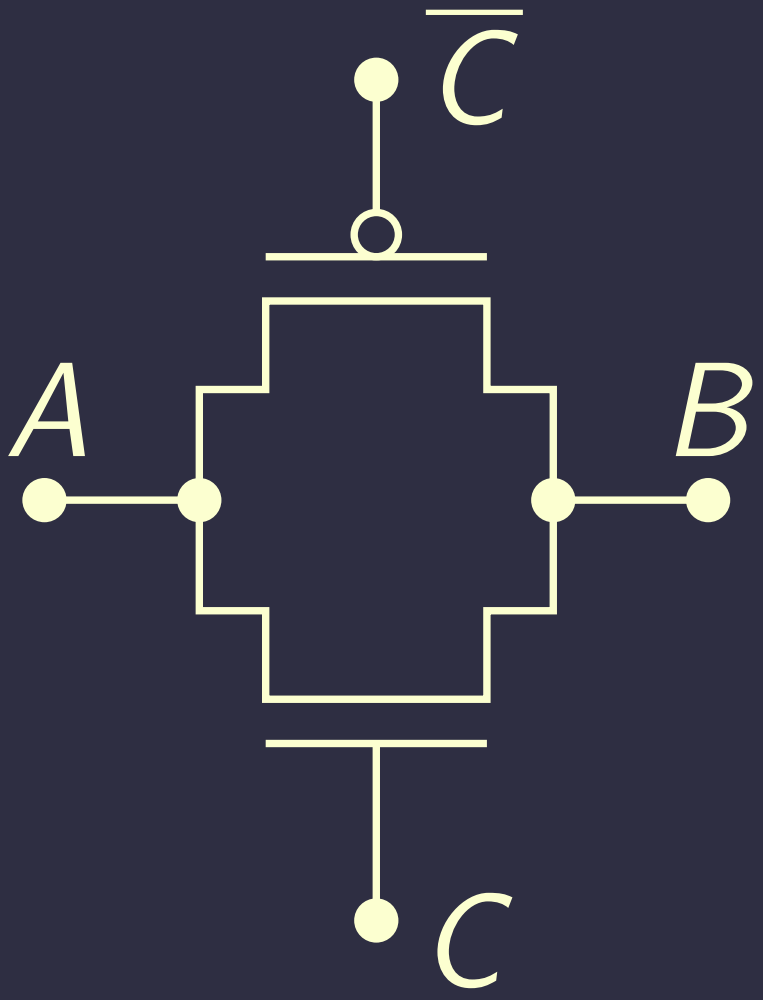

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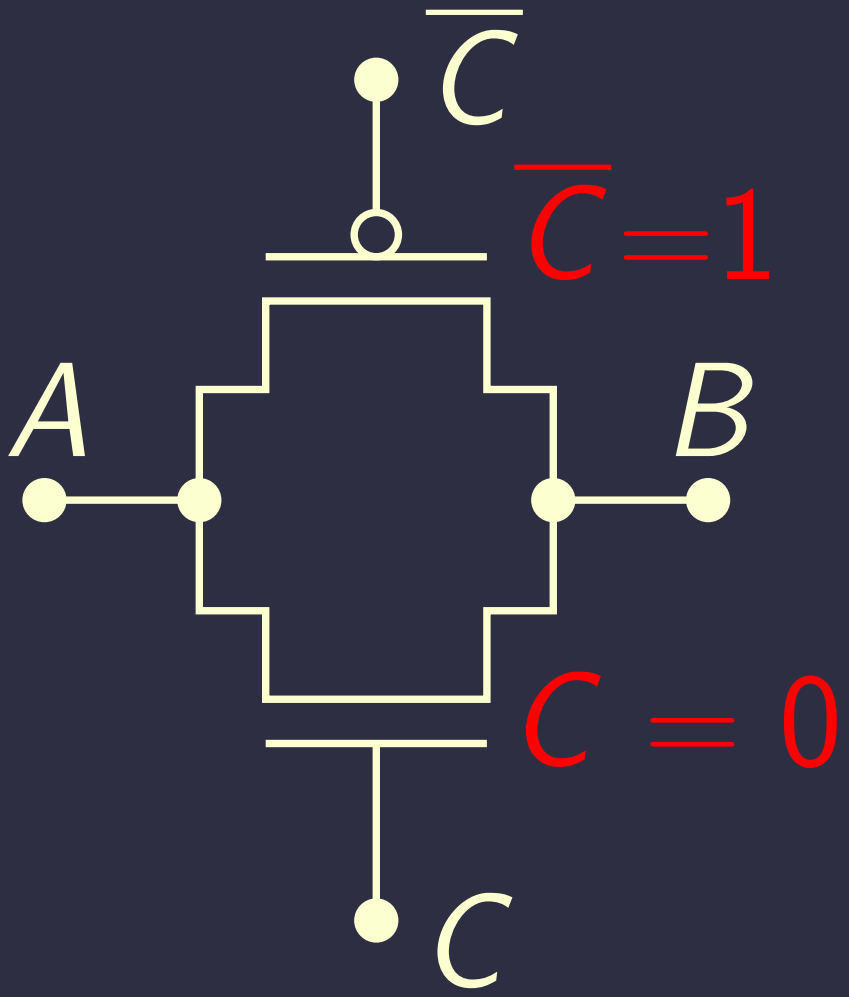

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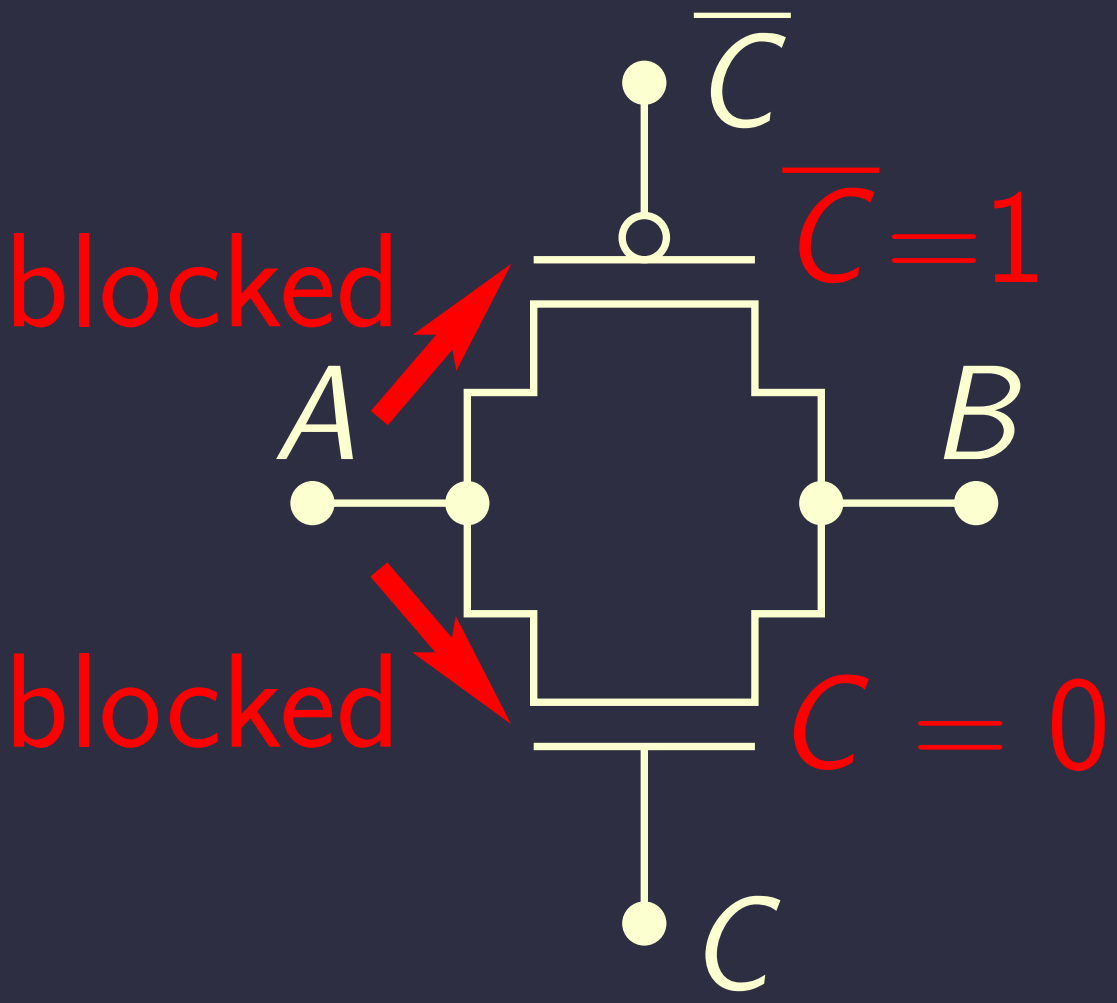
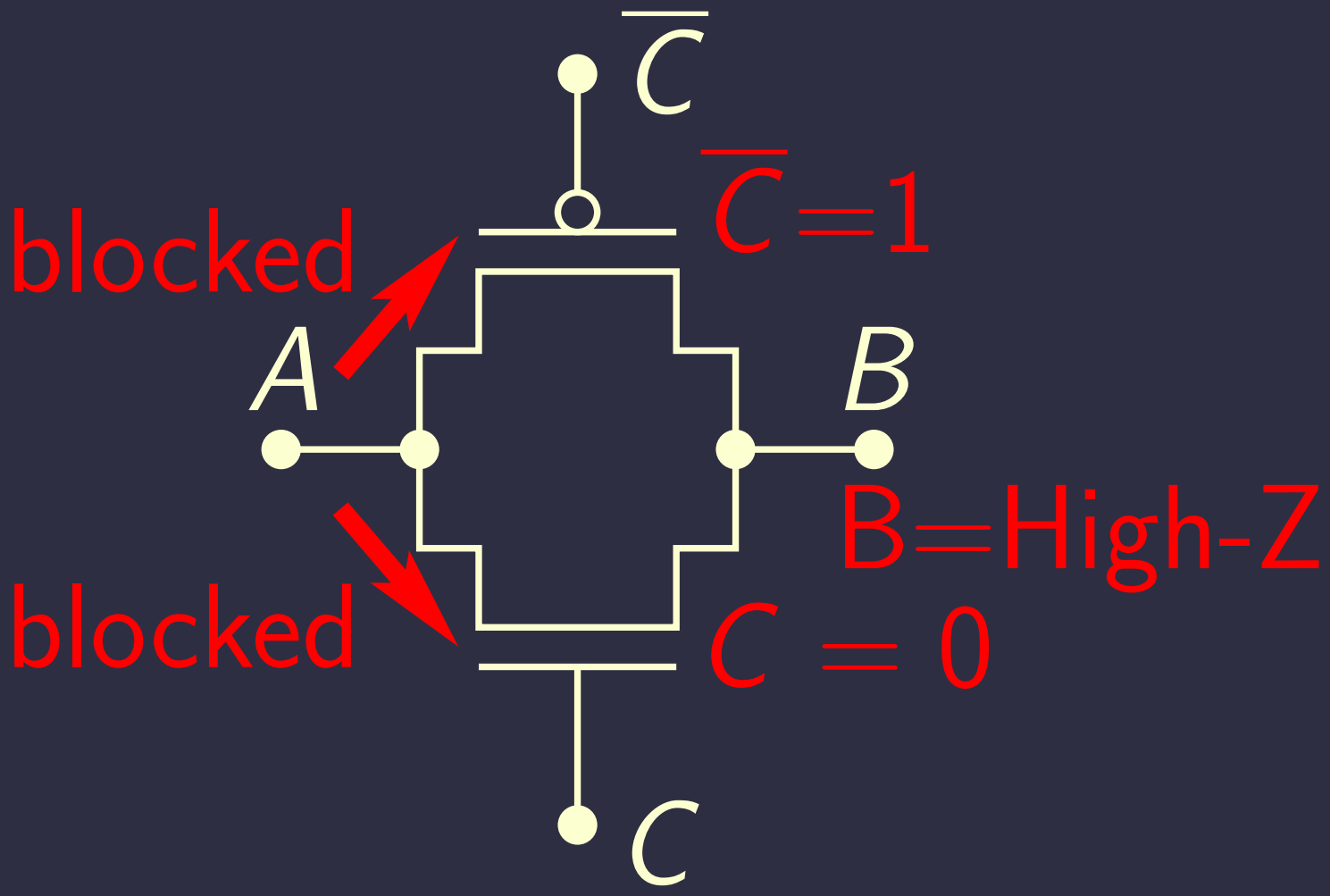
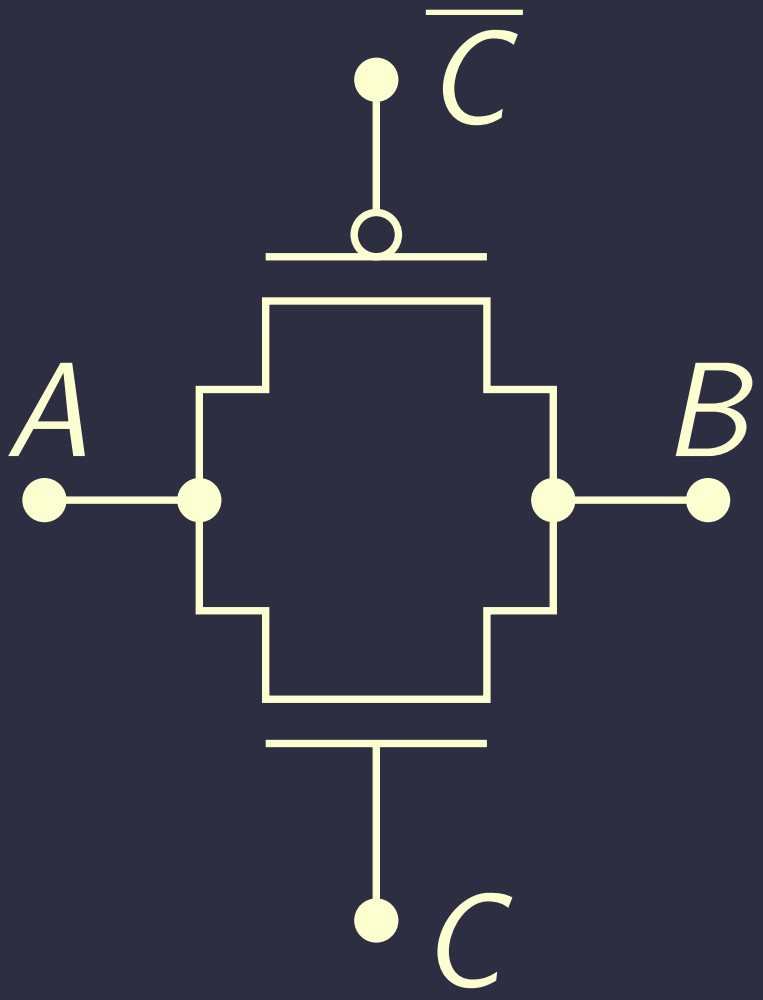


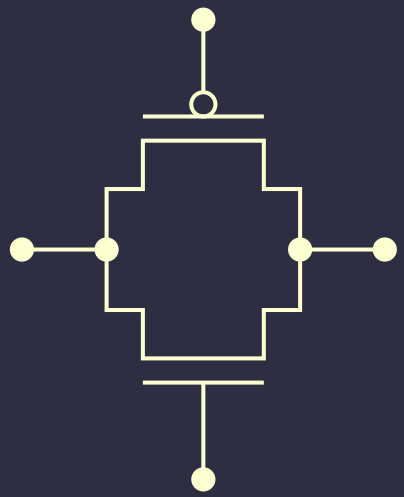
CMOS transmission gate (TG)

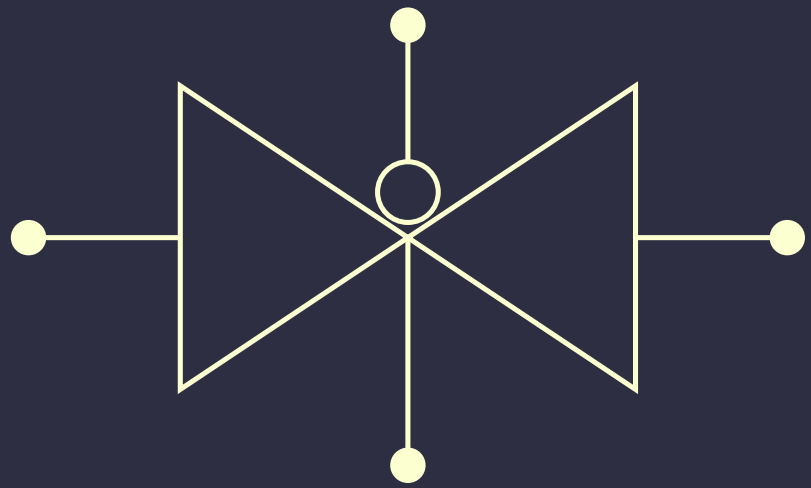


CMOS transmission gate (TG)



Other TG diagram





Logic gates vs. TGs

- What can each be used to implement?
- How to decide which to use?

Upcoming topics

- Diodes.
- Transistor static behavior.
- Transistor dynamic behavior.

Lecture plan

1. Lab one
2. Desired transistor behavior
3. Homework

Homework assignment and announcement

- 12 September: Read Section 3.3.2 in J. Rabaey, A. Chandrakasan, and B. Nikolic. *Digital Integrated Circuits: A Design Perspective*. Prentice-Hall, second edition, 2003.
- 17 September: Laboratory assignment one.