EECS 312 Discussion 10

11/8

Shengshuo Lu

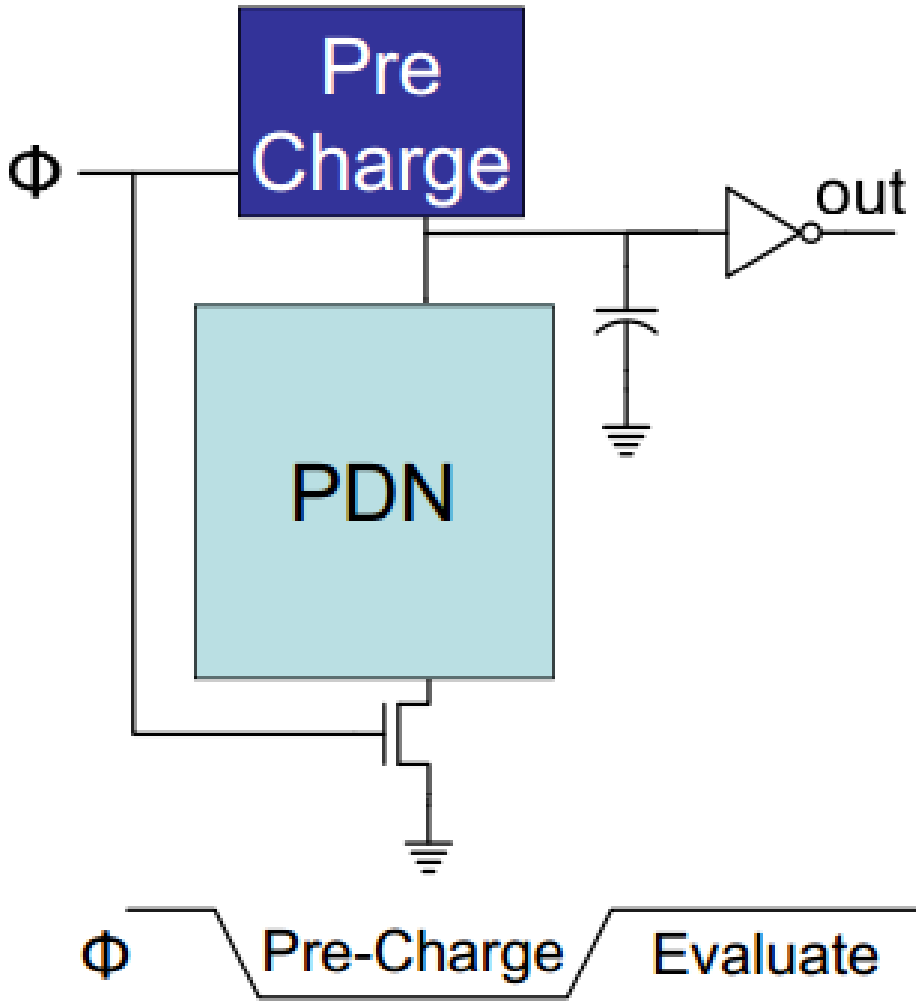
(luss@umich.edu)

Overview

- Reminder
  - Hw 4: Due Nov 16
- Dynamic Logic
- Sequential Logic

Dynamic Logic Families

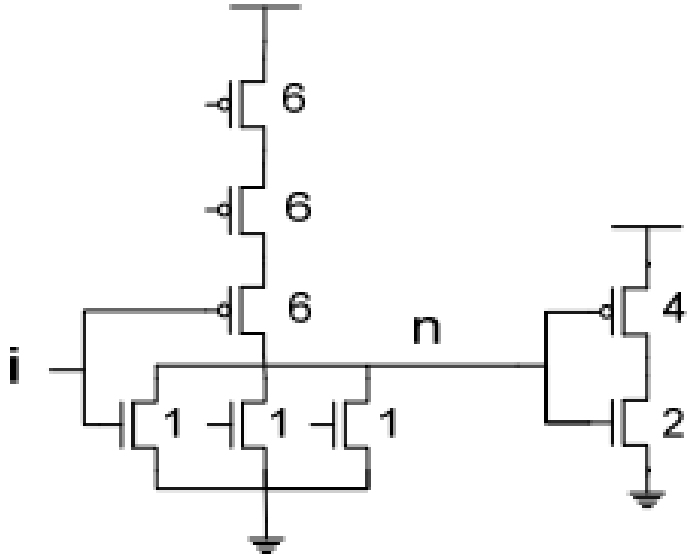
Basic Domino gate

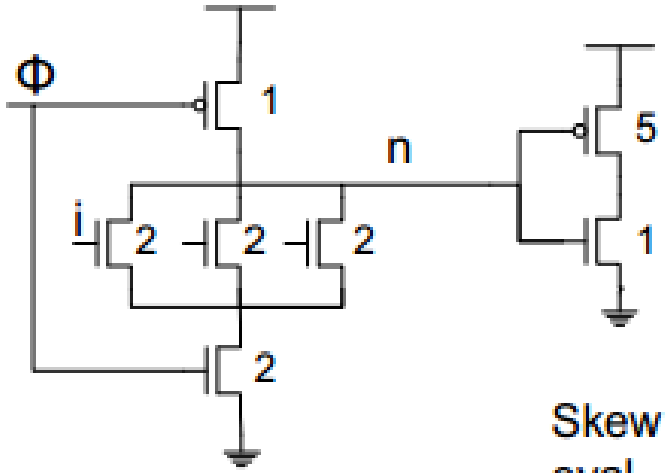


- Divide the clock in 2 phases:
  - Precharge
    - Output Low
    - Dyn. Cap precharge
    - PDN Off
  - Evaluate
    - Conditional discharge
    - Input must be stable and monotonic L→H

Domino / Static C_{in}/C_{out}

3-input OR gate



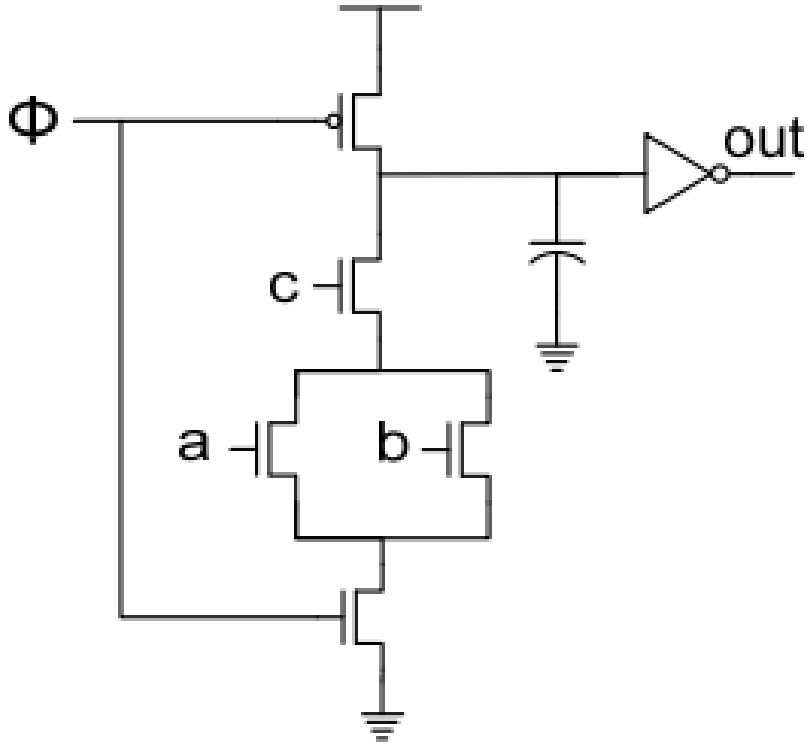


Skew for eval

Static:
$C_i = 7$
$C_n = 9$

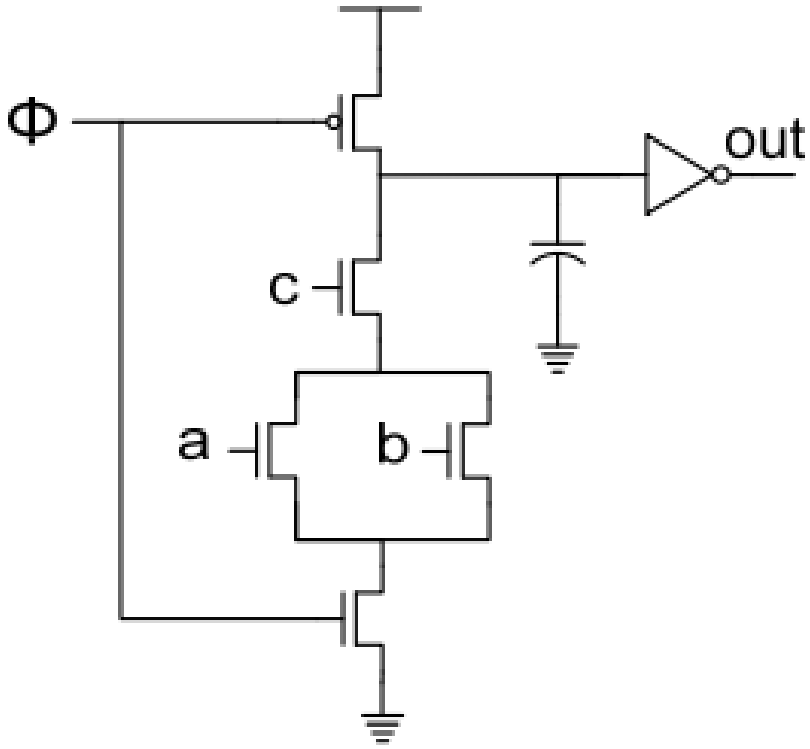
Dynamic:
$C_i = 2$
$C_n = 7$

Basic Domino gate



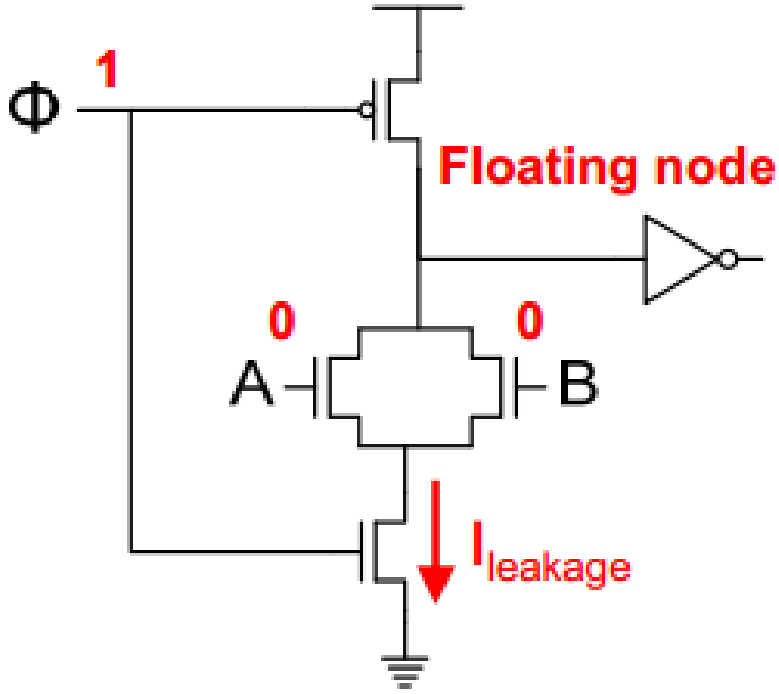
- Advantages:
  - Faster than CMOS
  - Input capacitance is lower
  - Early switch point
  - Inverter P/N > 2 (only rising delay important)

Basic Domino gate



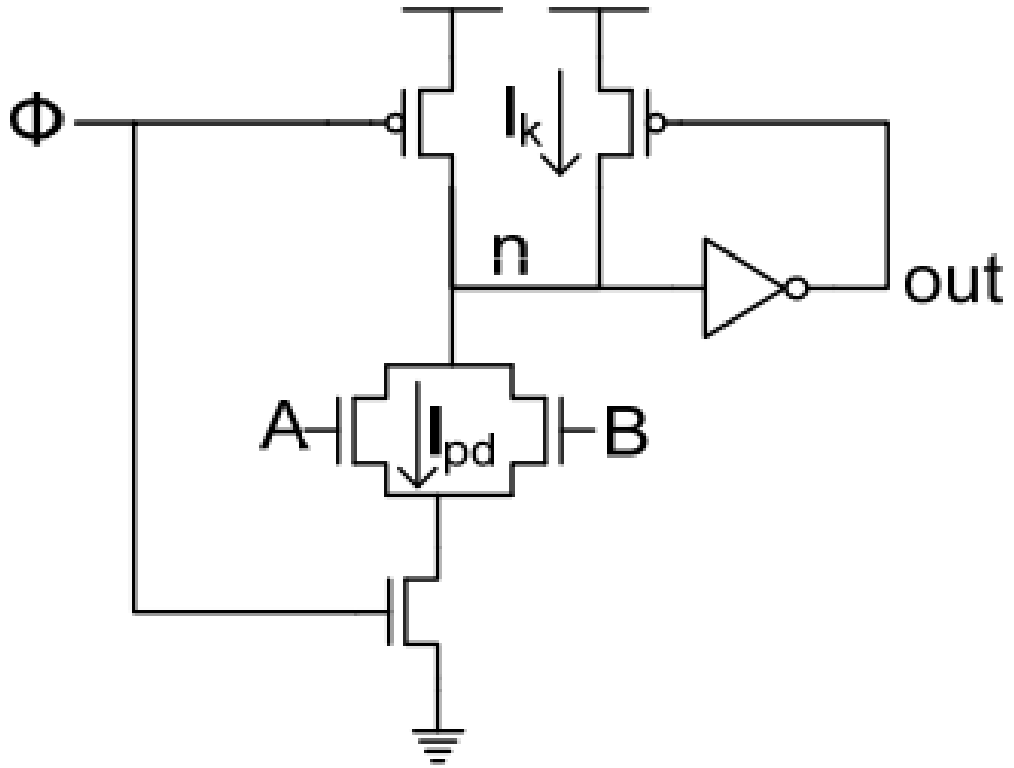
- Disadvantages:
  - Low noise margin
  - Charge sharing
  - Leakage currents
  - Internal capacitance charge sensitive to noise

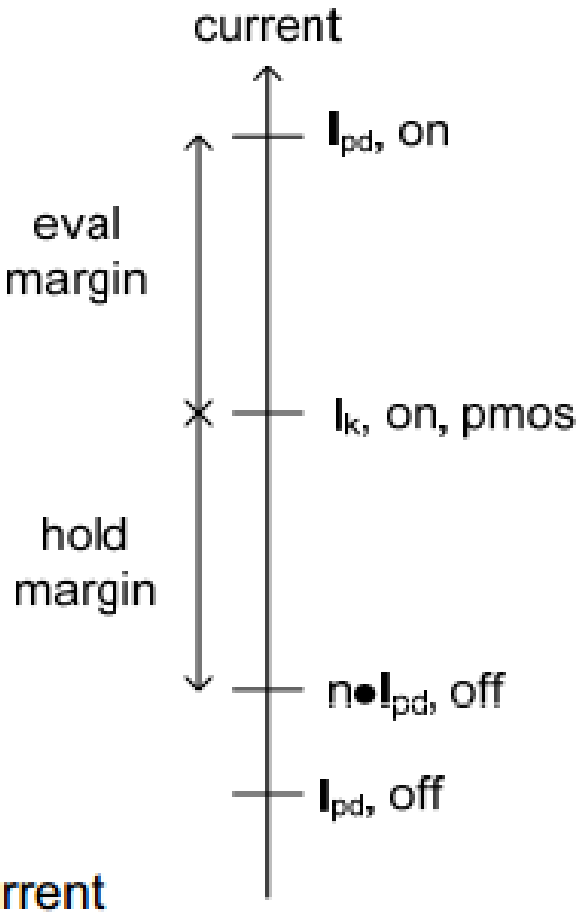
Issues: Leakage



- Dynamic node is floating during evaluation
  - Leakage current of NMOS can discharge it

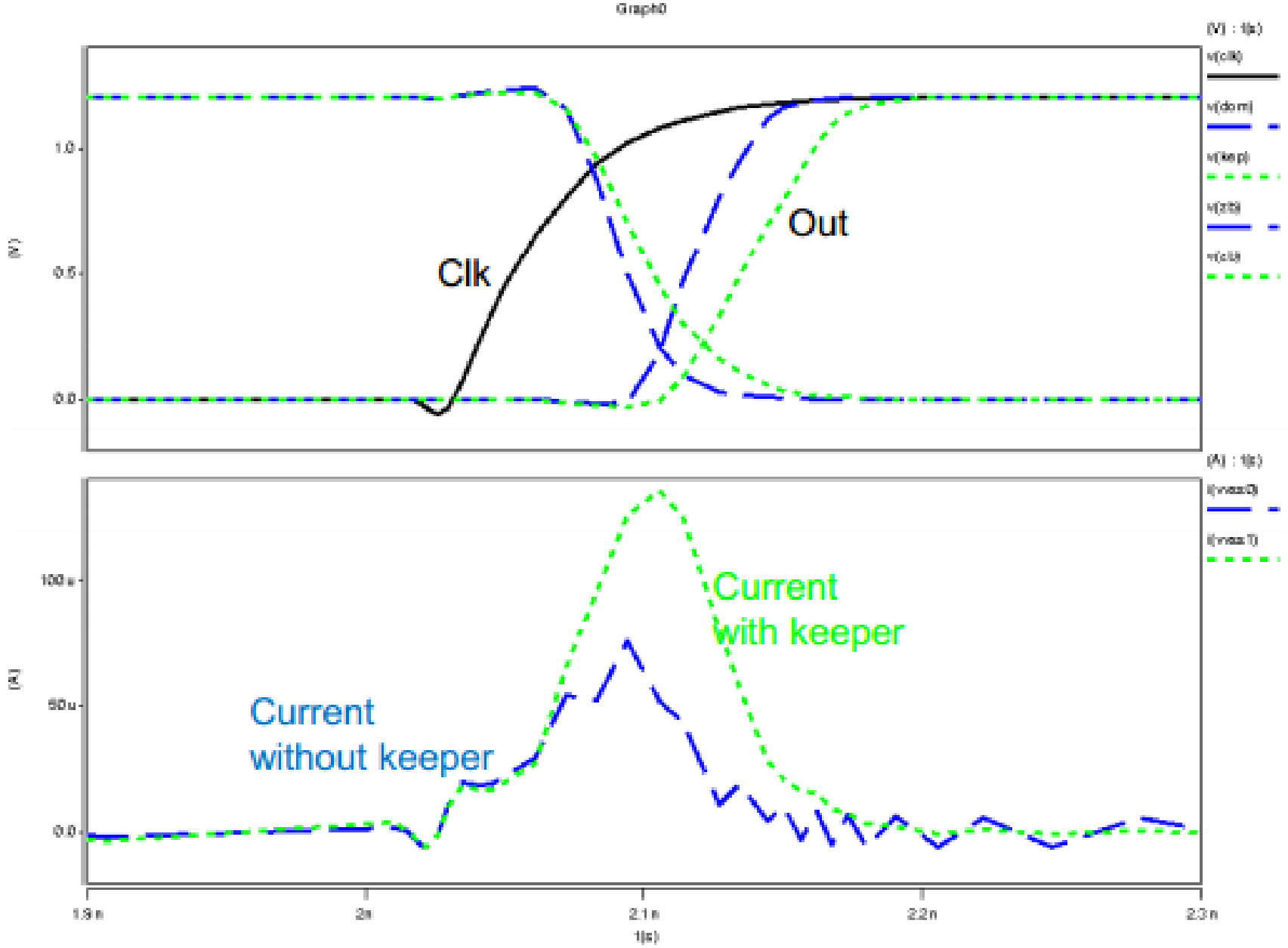
Issues: Leakage



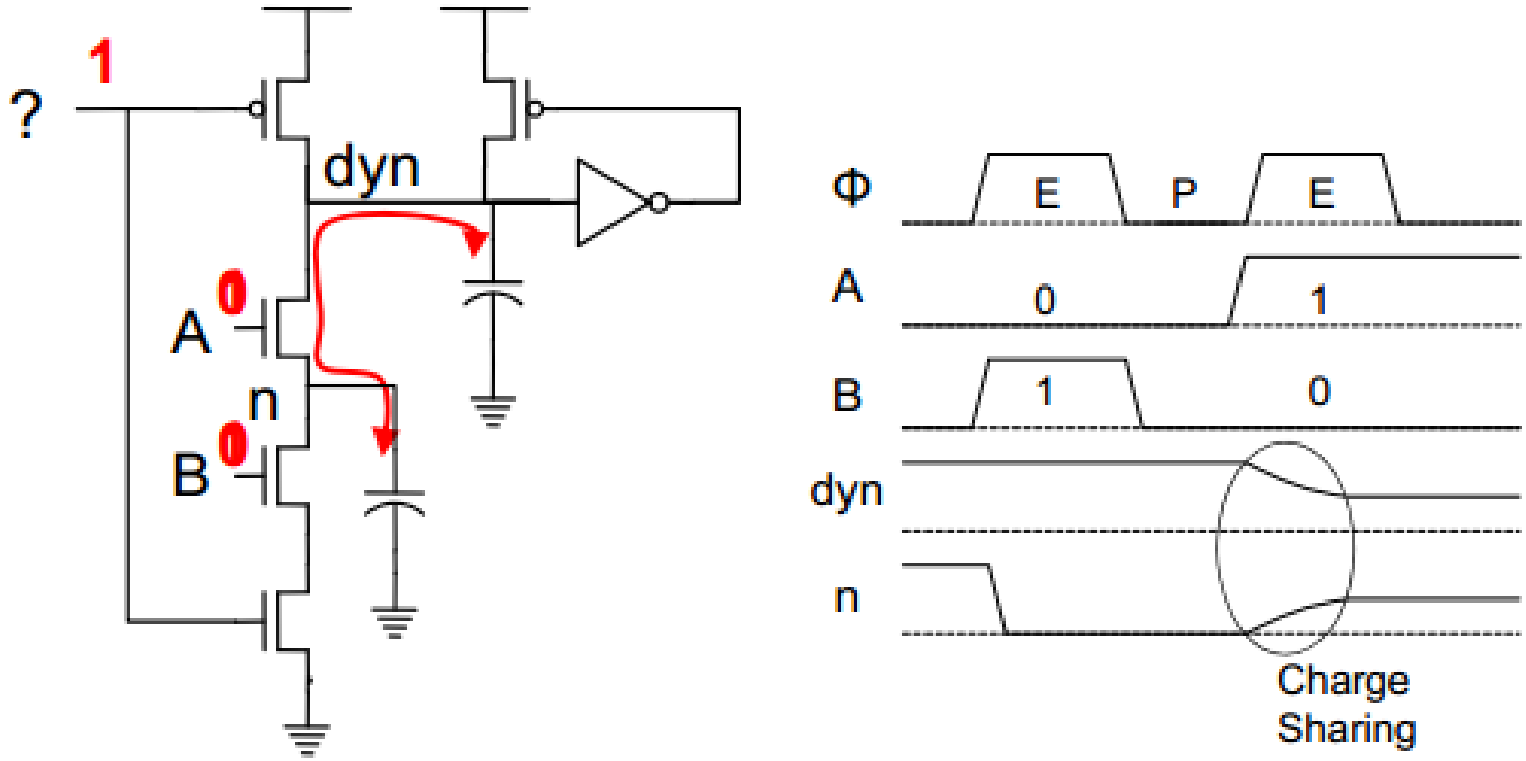


- Half latch devices:
  - Size PMOS to replenish the leakage current
  - Limits width OR gates

Domino – with and without keeper

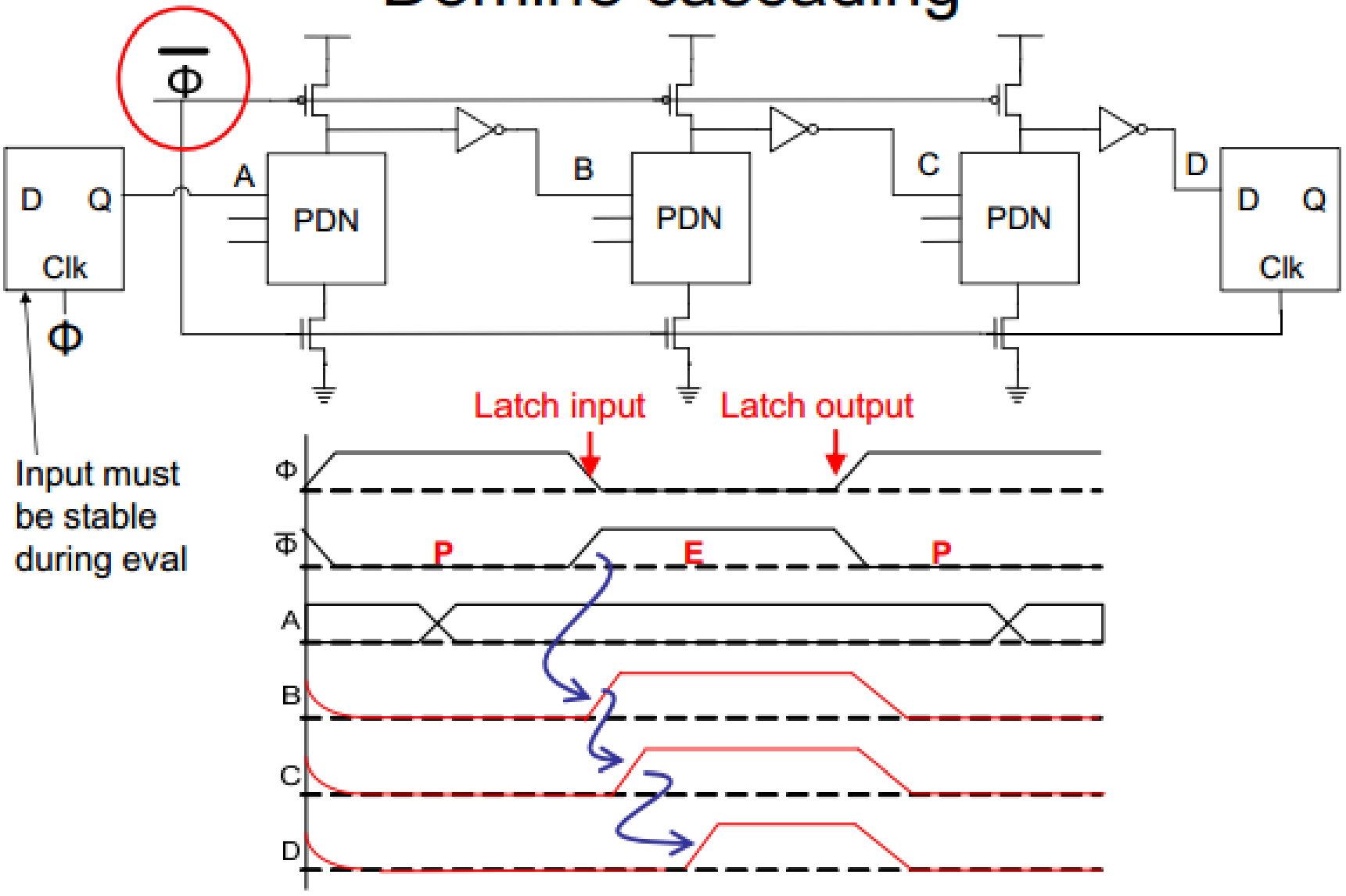


Issues: Charge sharing



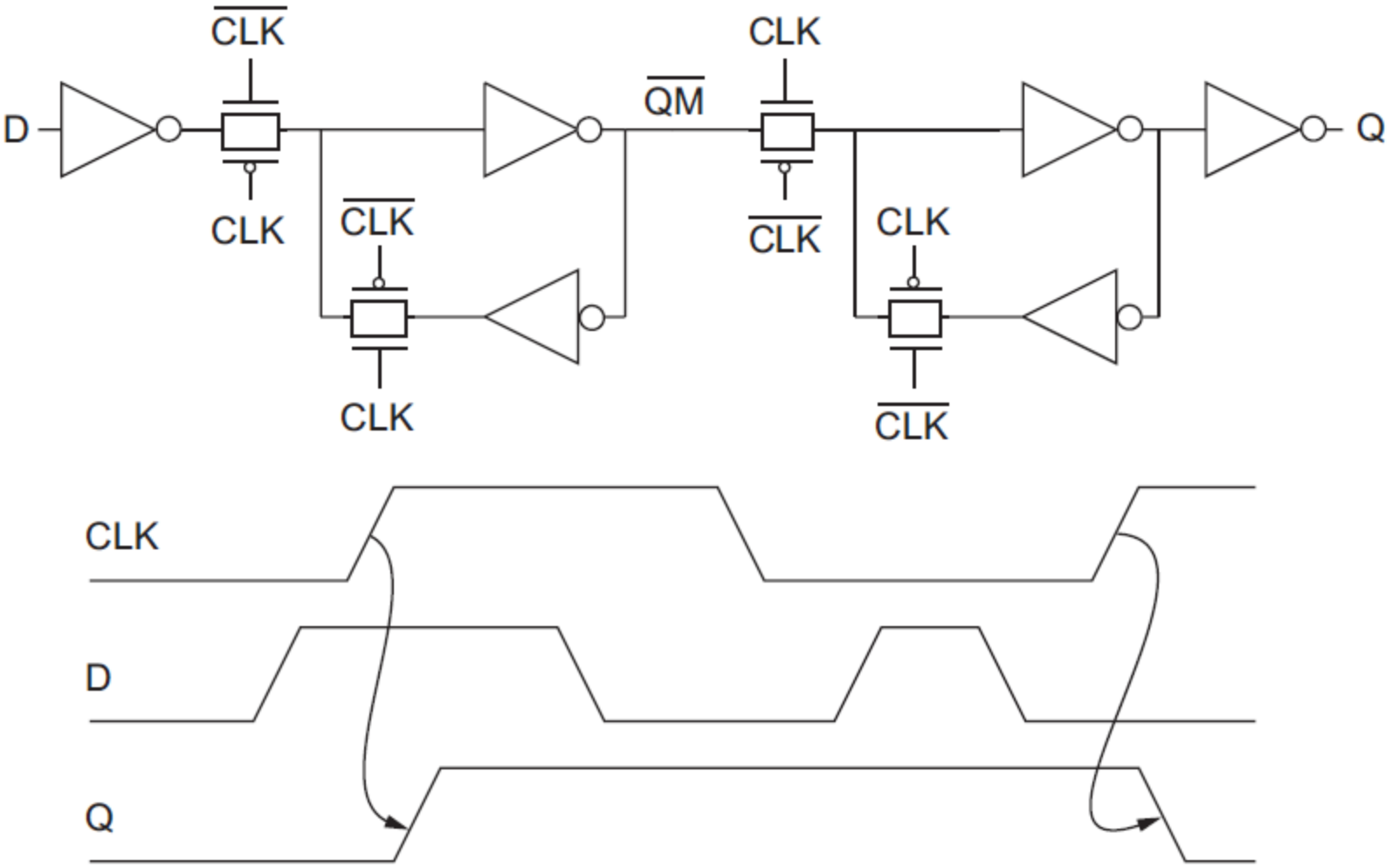
- In evaluate, dynamic node charge is shared with internal node caps
- Node was discharged in previous cycle

Domino cascading

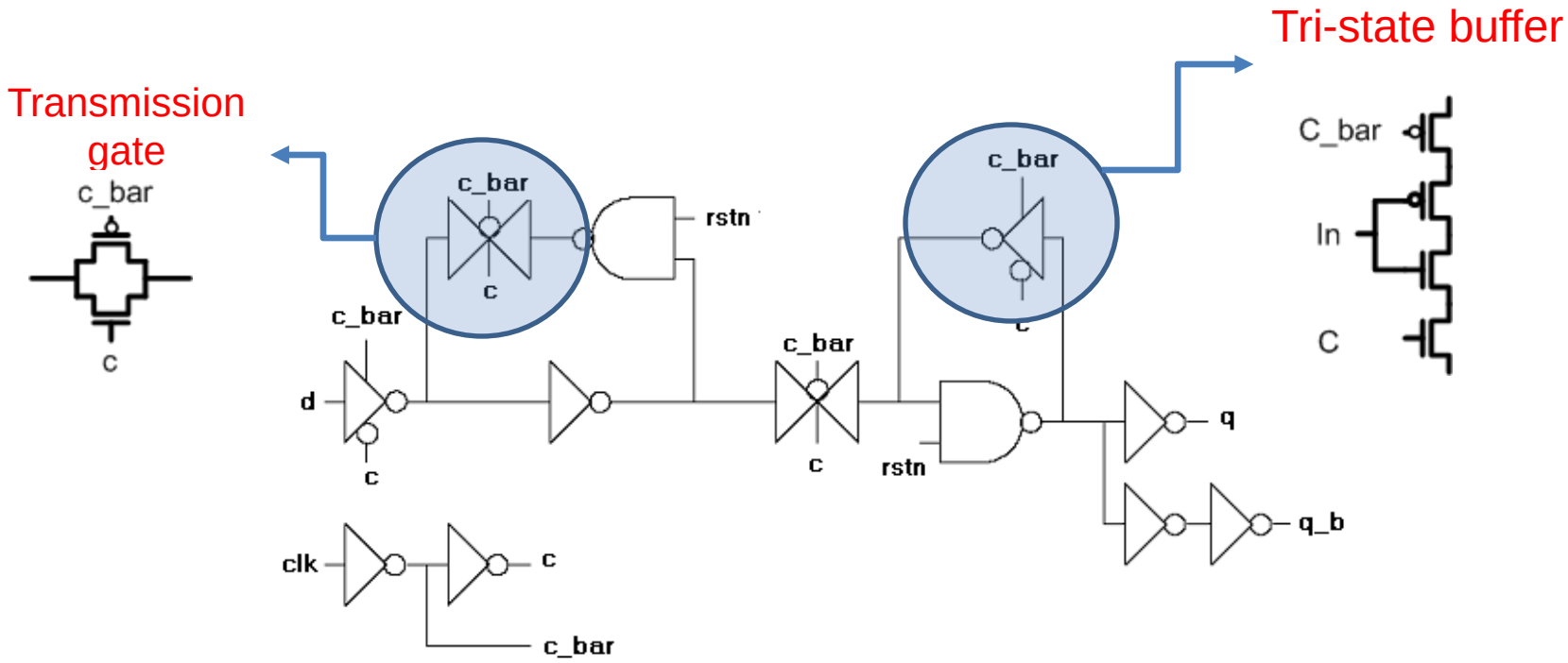


Sequential Logic

Flip-flop (Basics)



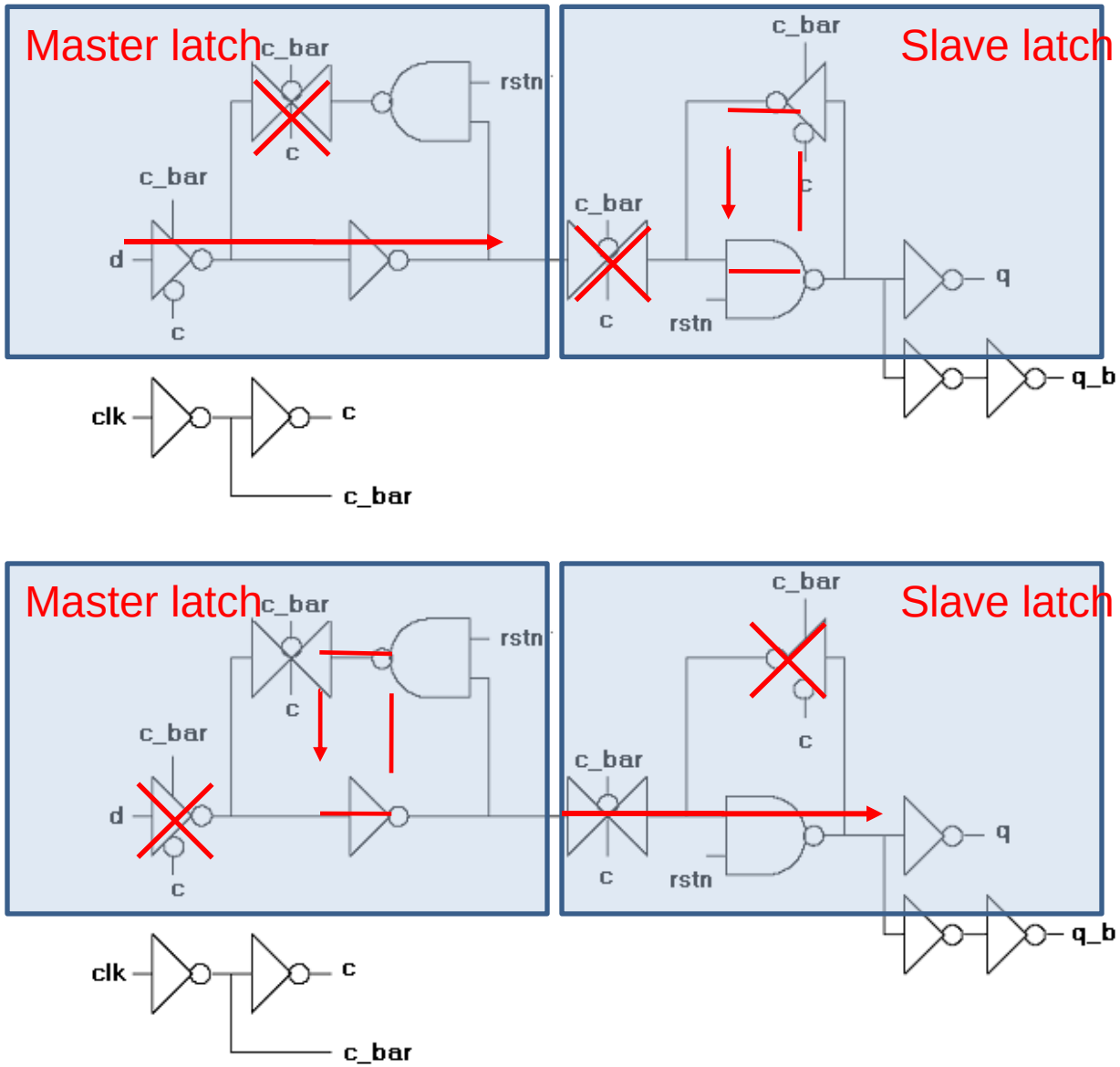
Flip-flop



- Flip Flop with Asynchronous Reset

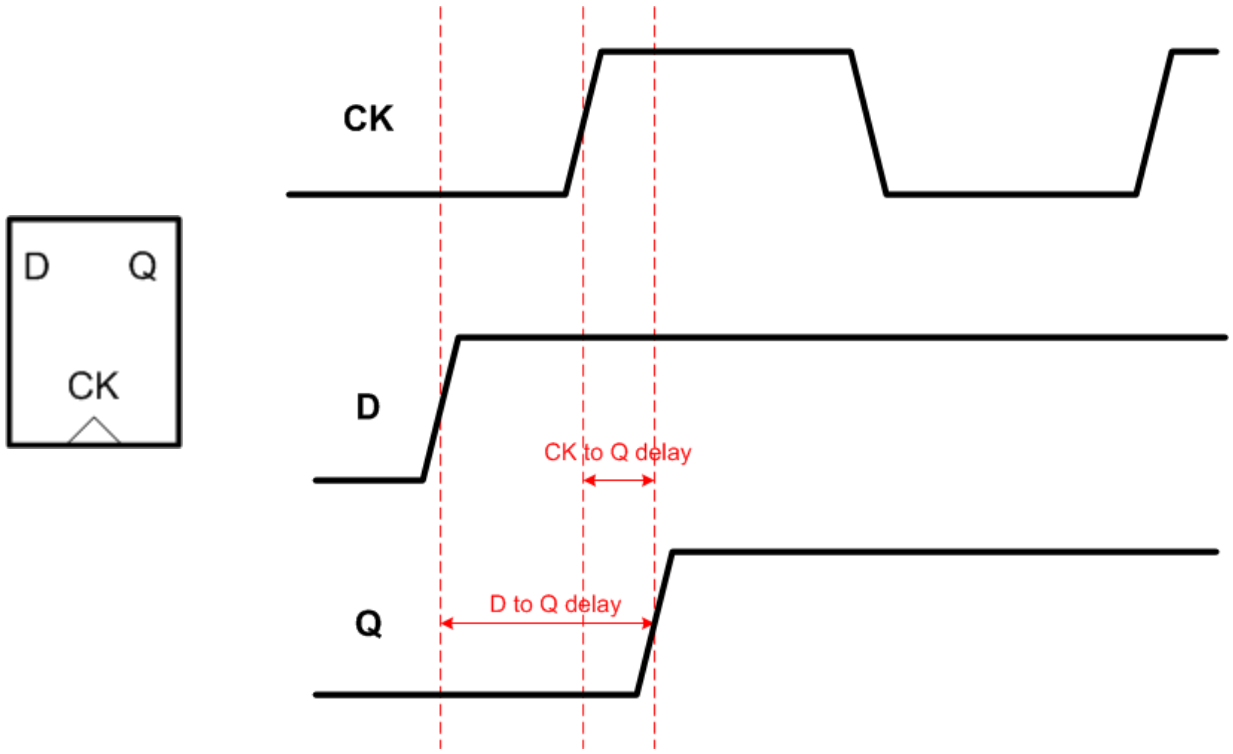
Flip-flop

- How it works
  - Divided flip flop into 2 latches (master and slave)
  - When master is transparent, slave holds.
  - When master holds, slave is transparent
  - Capture data at the rising edge of clock



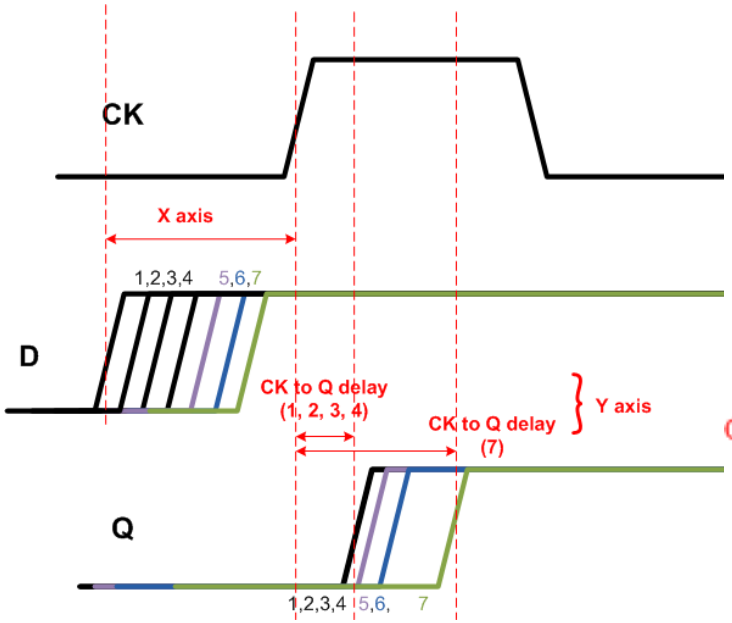
Flip-flop (continued)

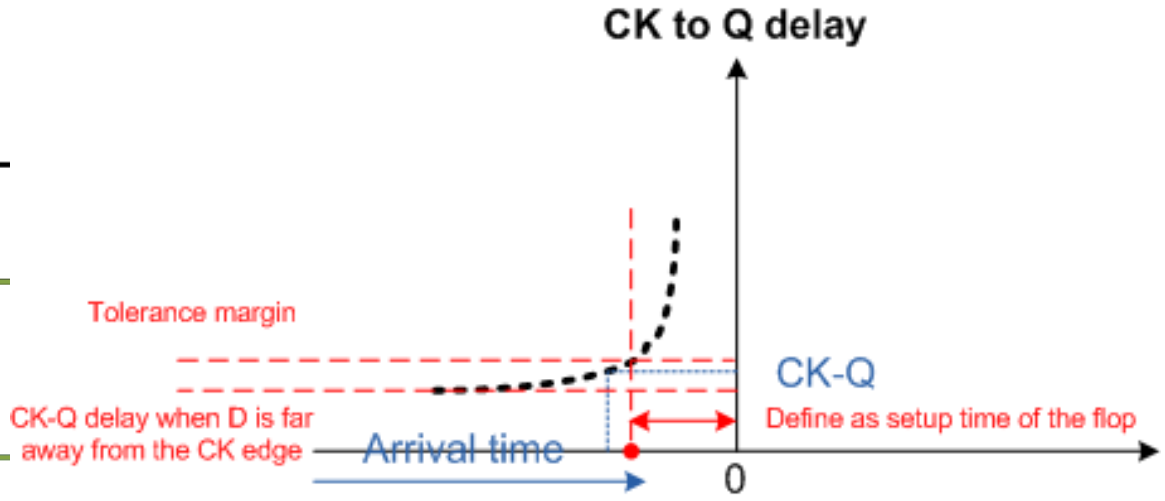
- Important terms : C-Q delay, D-Q delay



Flip-flop (continued)

- Setup Time
  - As D approaches to CK edge, C-Q delay goes up





When D arrives after the setup time point, we call it setup time violation

Setup-Time : Point at which CLK-Q delay rises 5% beyond nominal

Flip-flop (continued)

- Hold Time
  - Input should be stable for a period of time after the clk edge