EECS 312: Digital Integrated Circuits
Lab Project 3 – Inverting logic and low-energy function implementation

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Due: 25 October

1 Why is CMOS an inverting logic?

For the first two laboratory projects, there was little flexibility. Now it is time to try two designs on your own. We have learned in class that CMOS logic gates ought to produce inverted outputs, and we learned in laboratory project one how to properly design a CMOS inverter. Now, let's see what happens when these lessons are ignored. Design a CMOS buffer using a 360 nm wide NMOSFET and a 720 nm wide PMOSFET. Load the output with a 60 fF capacitor. In contrast with the proper design style taught in class, use the PMOSFET in the pull-down network and the NMOSFET in the pull-up network. Place a standard inverter design in the same schematic. Use the same V_{in} for the inverter and buffer. Plot V_{in} and V_{out} (for each design) with respect to time using square wave for V_{in}. Choose a period for V_{in} such that V_{out} nearly converges to its steady-state value. Plot a long enough duration to clearly see each gate's response to both a rising and falling V_{in} transition. Explain what you observed and give the reasons for this effect. Contrast the results for the inverting and non-inverting design styles. Only a few sentences are required: cover the most important points. However, an explanation is required.

2 Implement a logic function and minimize its energy consumption

Implement the following logic function using static CMOS logic:

$$f(a, b) = \overline{\overline{a} + b}.$$

Use a circuit structure and transistor sizes in order to minimize energy consumption for the highest-energy input transition. The time span over which to consider power consumption starts at the moment the input(s) switch and ends when the output crosses either the 0.25 V or 2.25 V point, whichever is later. The inputs to the system should be $\overline{a}$ and $\overline{b}$ and must each be passed through inverters constructed using 360 nm wide NMOSFETs and 720 nm wide PMOSFETs to produce a and b. Your design will take the resulting a and b as inputs. $\overline{a}$ and $\overline{b}$ may transition instantaneously, but of course a and b will transition gradually due to the non-ideal behavior of the inverters producing them. The energy consumed in these two inverters must be counted as part of the total circuit energy, but you may not change their sizes. The output of your gate must feed a 60 fF capacitor. When doing energy analysis for the gate, be sure that the highest energy consumption input transition is considered. A little thinking here can save a lot of effort. Think of how square waves with different periods can be used for the two inputs to simplify generation of many input transitions. It is fine to neglect analysis of transitions that clearly do not have worst-case energy consumption. Consider the sum of the energy dissipated in the channels of the two inverters and your logic gate. You may find the "Intel" integration function in the Waveform Calculator useful. Be careful when entering times to use E notation, not carrot notation, i.e., 5E-6 instead of 5*10^(-6). Explain what design decisions you made to minimize energy consumption and simplify analysis.

3 Deliverables

1. Schematic of non-inverting logic buffer.

2. Timing diagram for the non-inverting logic buffer.

3. Discussion of buffer behavior. Focus on the most important concepts.

4. Schematic of $f(a, b)$ implementation, including input inverters and load capacitor.

5. Timing diagrams showing V_C (for the output load capacitor), and the total power consumptions of all transistors for input transitions that may potentially result in worst-case energy consumption.

6. Explanation of the design decisions you made to minimize the energy consumption of the circuit.