Homework Four

EECS 312: Digital Integrated Circuits

Teacher: Robert Dick
Assigned: 8 November
Due: 20 November

You may discuss the assignment with your classmates. However, you need to understand and write the solutions independently.

1. **(10 pts.)** Show the circuit diagram for

$$f(a, b, c) = ab + \overline{a}\,\overline{b}\,\overline{c} \tag{1}$$

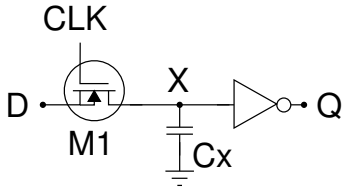
   implemented with

   (a) **(5 pts.)** Transmission gates (with output buffer or inverter) and

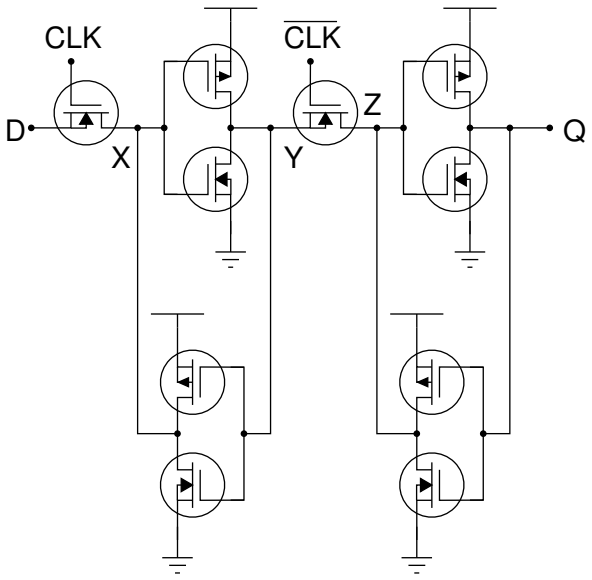
   (b) **(5 pts.)** Pass transistors (with output buffer or inverter).

   Do not assume access to complemented input literals.

2. **(10 pts.)** In the latch in the following figure, compute the setup time when D is low (that is, a low value is being passed from D to X). Assume the initial voltage at node X is $(V_{DD} - V_{Tn}(V_x)) = 1.8\,\text{V}$. You must compute the equivalent resistance of the pass transistor at the midpoint of the voltage swing of interest. Let the width of the NMOS pass transistor be W=1 µm and the PMOS/NMOS sizes of the inverter are 2 µm and 1 µm respectively. Assume that the junction+sidewall capacitance is 0.6 fF/µm multiplied by the transistor width and ignore overlap capacitance.



3. **(15 total pts.)** Assume the register shown below is driven at input D by a CMOS inverter. 4 cross-coupled inverters in the flip-flop have W_p=W_n= 0.5 µm and minimum channel length.



(a) **(7 pts.)** Find an inequality relationship among the width of the pass transistor connected to node X, the width of the (off-diagram) inverter driving that pass transistor, and the width of the appropriate transistor in the inverter driving node X that ensures proper functionality for storing a 0 (ignore body effect) at Q. You may need to make some simplifying assumptions regarding feedback; please describe these clearly in your answer. Take the switching voltage, $V_M = 1\,\mathrm{V}$ for the inverters with $W_p = W_n$ and the default technology parameters.

(b) **(4 pts.)** How would you redesign the flip-flop to relax the sizing requirement on the driving stage? A qualitative answer is sufficient.

(c) **(4 pts.)** Suppose we change the circuit by adding a feedback NMOS pass transistor inserted between the output of the feedback inverter in the leading stage and node X (the leading stage now looks like Figure 7-8a of the text). How does this change the sizing requirement of part (a)? A qualitative answer is sufficient.

4. **(10 pts.)** To perform a certain function in a microprocessor, data must propagate through 100 stages of logic, each having a delay equal to that of an inverter, t_{inv}. The speed of this operation sets the clock frequency of the system.

   (a) **(7 pts.)** Compare the speed (quantified by maximum clock frequency) of a non-pipelined system to that of a pipelined system with 10 stages. Let the design use registers having a delay equal to $3t_{inv}$ and a set-up time of $3t_{inv}$ also.

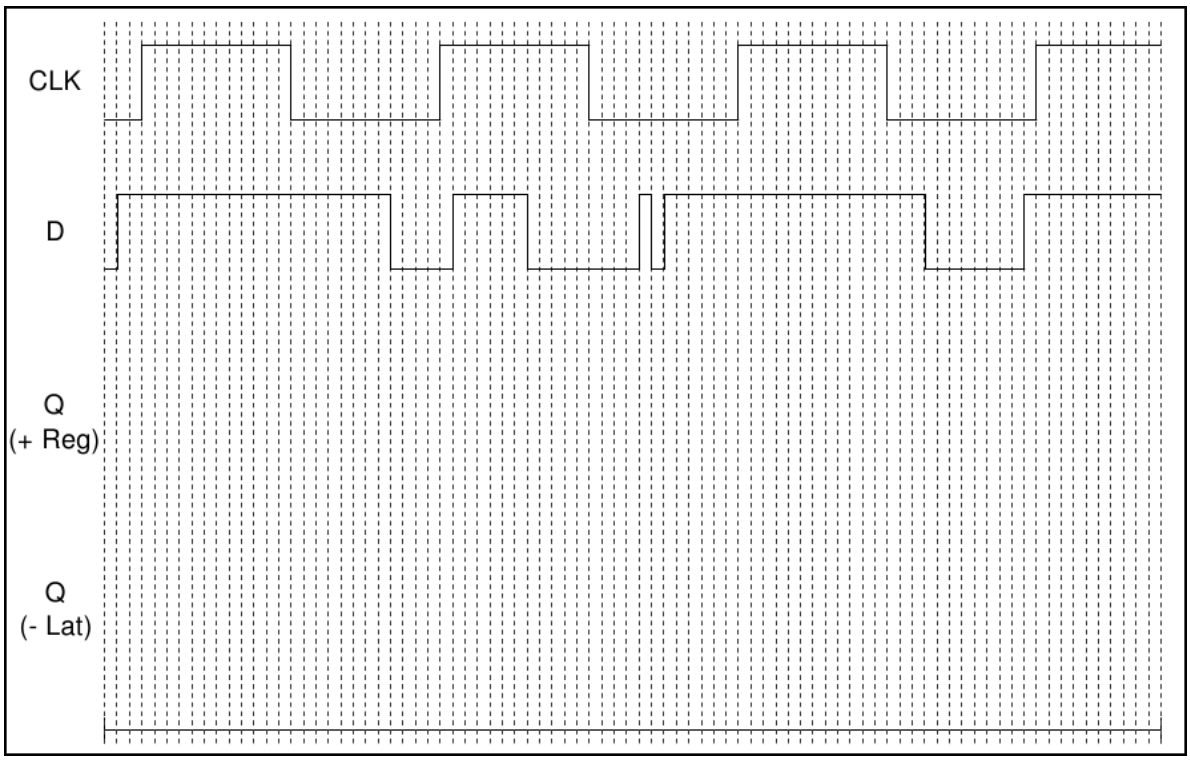
   (b) **(3 pts.)** What do the results imply about breaking up operations into an increasing number of very small operations?

5. **(10 pts.)** Given the following clock and data waveforms, draw the output waveforms for a

   (a) positive edge-triggered register and

   (b) a negative latch.

   The timing characteristics of these sequential elements follow: $t_{c\to Q} = 4$ units, $t_{D\to Q} = 3$ units, $t_{setup} = t_{hold} = 2$ units. Vertical dashed lines have a separation of one unit. Note the clock period is equal to 24 units. Clearly mark on the figure where setup and hold time violations occur for each sequential element.



6. **(10 total pts.)** Consider a CMOS inverter driving a latch through a noisy wire. We expect noise voltage of up to 70% of V_{DD} on either supply rail to be induced in the line. We need the input to this Latch to be "clean" or noise-free.

   (a) **(3 pts.)** Explain (in terms of a VTC) why a static CMOS inverter (or pair of inverters to make it non-inverting) will not be able to provide the required noise immunity if inserted before the Latch at the end of the wire.

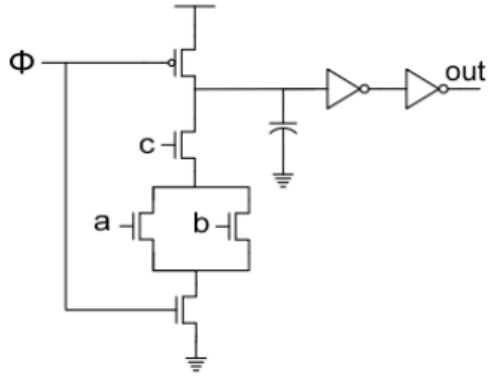
   (b) **(7 pts.)** Suppose we place a CMOS Schmitt trigger at the end of the line, before the latch. Size the controlling inverter (M3 and M4 in Figure 7-47 of the text) to ensure proper noise rejection assuming that both the input inverter and feedback inverter have $W_p = 2\,\mu\text{m}$, $W_n = 1\,\mu\text{m}$ with minimum channel lengths.

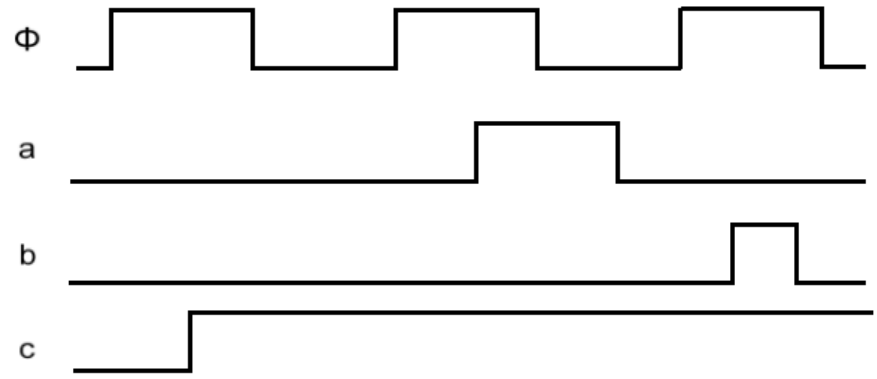
7. **(10 pts.)** Demonstrate that you know how to design a 4:1 MUX from the transistor level. Your design should have a structure making it possible to be sure that the maximum resistance from an output to V_{DD} or V_{SS} is no greater than that of a balanced, minimum-width inverter. You may size relative to w, the minimal width of a FET.

8. **(5 pts.)** What is the state of an asynchronous finite state machine the function of? What is the output of an asynchronous finite state machine the function of?

9. **(10 pts.)** Design a one-input circuit that will produce a constant output when its input is 0 and will produce an output that oscillates between 0 and 1 when its input is 1. Design and size this device such that the period of oscillation is approximately 5 ns. Use transistors to supply any required resistance and capacitance.

10. **(10 pts.)** Consider the dynamic gate shown in the following figure. Based on the input signal, draw the output signal.





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