EECS 312 Homework 2 Solution

Q1:

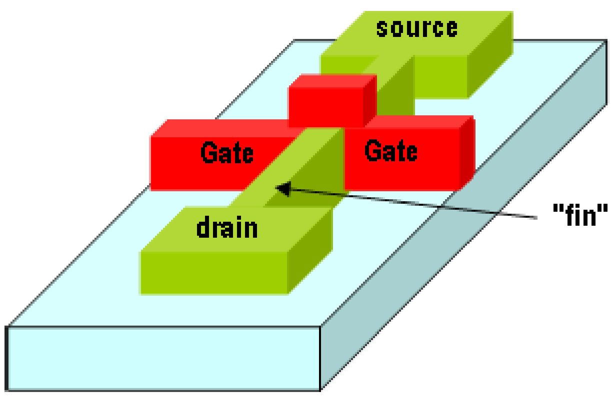
Plasma Etching is more selective (directional etching, anisotropic) compared to wet etching (isotropic) however wet etching can be performed in batch mode (processing many wafers all at once).

Q3:

By using the high k dielectric and keeping all the other parameters constant we can increase transconductance compared to the case with a low k dielectric material. $I \sim C_{ox}$ and $C_{ox} = E_{ox}/t_{ox}$. By changing silicon dioxide (SiO2) with a high K dielectric material, let's say y we have $I \sim C_y = E_y/T_y$ and $E_y > E_{ox}$. Therefore we have more current.

Q4:

A double-gate transistors on an SOI substrate in which the gate is wrapped around the channel.



Q5:

In the question it says: $V_{DD}=V_t$; conclusion: this devices is either in cut off or linear region.

a) C_{gcs}, C_{gcd} and C_{gcb} contribute to C_T.

b) $V_{gs} < V_t$: Cut-off: $C_T = C_{gcb} = WLC_{ox}$

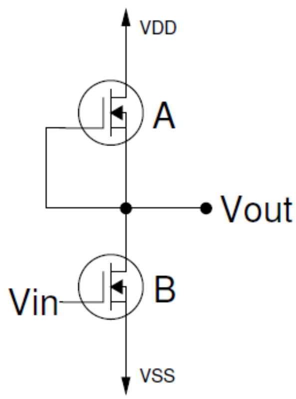
$V_{gs}-V_t < V_{ds}$: Saturation: $C_T = C_{gcs} = 2/3WLC_{ox}$

$V_{gs}-V_t > V_{ds}$: Linear: $C_T = C_{gcs} + C_{gcd} = 1/2WLC_{ox} + 1/2WLC_{ox} = WLC_{ox}$

c) $t = t1 + t2 = C1\Delta V1/I_{in} + C2\Delta V2/I_{in} = WLC_{ox}\cdot V_t/I_{in} + 2/3 \cdot WLC_{ox}\cdot(2V_t-V_t)/I_{in} + WLC_{ox}\cdot(3V_t-2V_t)/I_{in}$

$= 8/3\cdot WLC_{ox}\cdot V_t/I_{in}$

Q6:



V_{tA}=-0.4V V_{DD}=2.5V

(a) V_{in}=0V; this implies B is off
No current flows through A, but is on since $V_{GS}=0 > -0.4V$
The mode of operation of A is linear as $V_{GS}-V_t>V_{DS} = 0V$
(Vout=2.5V as it pulled to VDD)

(b) V_{in}=2.5V and B is on
(i) First assume both A and B is in linear region:
$I_D=k_n'W/L\ [(V_{GS}-V_t)V_{DS}-V_{DS}^2/2]$

Setting two current in two devices equal:

$k_n'W/L\ [(V_{GS\_B}-V_{t\_B})V_{DS\_B}-V_{DS\_B}^2/2] = k_n'W/L\ [(V_{GS\_A}-V_{t\_A})V_{DS\_A}-V_{DS\_A}^2/2]$
$(2.5-0.4)V_{out}-V_{out}^2/2 = 0.4(2.5-V_{out}) - (2.5-V_{out})^2/2$

- ➔ Doesn't solve

(ii) Assume B is in saturation while A is in linear:

$½\ k_n'W/L\ (V_{GS\_B}-V_{t\_B})^2 = k_n'W/L\ [(V_{GS\_A}-V_{t\_A})V_{DS\_A}-V_{DS\_A}^2/2]$
$½\ (2.5-0.4)^2 = 0.4(2.5-V_{out}) - (2.5-V_{out})^2/2$

Vout=2.1+2.062i , 2.1+2.062i → Complex, Not good.

(iii) Assume B is in linear while A is in saturation:

$k_n'W/L\ [(V_{GS\_B}-V_{t\_B})V_{DS\_B}-V_{DS\_B}^2/2]= ½\ k_n'W/L\ (V_{GS\_A}-V_{t\_A})^2$

$(2.5-0.4)V_{out}-V_{out}^2/2 = ½\ (0.4)^2$

V_{out} = <u>0.038V</u>, 4.16V (>V_{DD})
Check B is in linear: 2.5-0.038 > V_t → o.k.
Check A is in saturation: 0-(2.5-0.038) < V_t → o.k.

(c) $P_{avg} = 2.5V \cdot I_D \cdot 0.7\ (V_{in}=2.5V) + 2.5V \cdot 0 \cdot 0.3\ (V_{in}=0V)$
$= 2.5V \cdot (\ ½\ k_n'\ W/L\ (0.4)^2\ ) * 0.7 = 0.14 \cdot k_n' \cdot W/L$ Watt

Q7:

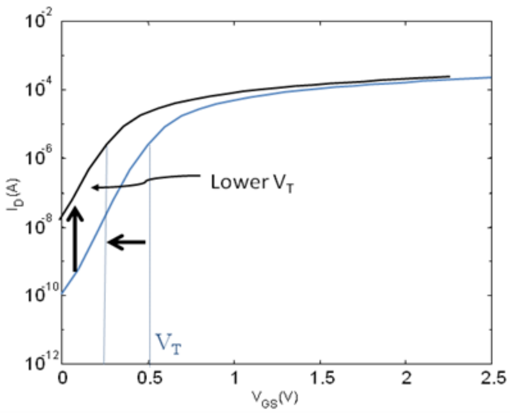
(a) $P_{dynamic} = CV^2f_{0\text{->}1}$
$P_{clock} = 10000 \cdot 40fF \cdot 2.5V^2 \cdot 1GHz = 2.5W$
$P_{comb} = 5000000 \cdot 6fF \cdot 2.5V^2 \cdot (0.1 \cdot 1GHz \cdot 0.5) = 9.375W$ → $f_{0\text{->}1}=\alpha_{sw} \cdot 1GHz \cdot 0.5$

$P_{dynamic} = P_{clock}+P_{comb} = 11.875W$

$Time_{depletion}=E_{battery}/P_{dynamic}=39W\cdot hr/11.875W=3.28$ hours

(b) I_{off} (I_{DS}@V_{GS}=0) is given as 10^{-10}A for V_t=0.5V

Determine I_{off} when V_t=0.25V



Note that V_t shift corresponds with a shift of I_{DS} vs. V_{GS} graph

Slope of sub-threshold region is 90 mV/dec and shifting the sub-threshold line left by 250mV will increase the off current by 250mV/90mV=2.78dec

Therefore I_{off} @ V_t=0.25V

$= 10^{-10}*10^{2.78}=10^{-7.22}=6.026\cdot10^{-8}A$

$P_{static} = I_{static}\cdot V$

$= 5010000 \cdot 6.026 \cdot 10^{-8} A \cdot 2.5V = 0.75W$

$P_{total} = P_{dynamic} + P_{static}$

$= 11.875W + 0.75W = 12.625W$

$Time_{depletion}=E_{battery}/P_{total}=39W\cdot hr/12.625W=3.09$ hours

% reduction = (3.28-3.09)/3.28 = 5.79%

(C) From Fig. 5-17 @ V_{DD}=1.3 normalized t_p is ~ 2. That is, propagation delay has doubled so peak frequency has to be halved. The operating clock frequency = 0.5 · 1GHz = 500mHz

$P_{dynamic} = P_{clock}+P_{comb} = 10000 \cdot 40fF \cdot 1.3V^2 \cdot 500mHz + 5000000 \cdot 6fF \cdot 1.3V^2 \cdot 0.10 \cdot 500mHz \cdot 0.5$

$= 1.61W$

$P_{static} = 5010000 \cdot 6.026 \cdot 10^{-8} A \cdot 1.3V= 0.391W$

$P_{total} = P_{dynamic} + P_{static} = 2.00W$

$Time_{depletion}=E_{battery}/P_{total}=39W\cdot hr/2W=19.5$ hours

(d) $P_{dynamic} = P_{clock}+P_{comb} = 10000 \cdot 40fF \cdot 2.5V^2 \cdot 500mHz + 5000000 \cdot 6fF \cdot 2.5V^2 \cdot 0.10 \cdot 500mHz \cdot 0.5$

$= 5.94W$

$P_{static} = 5010000 \cdot 6.026 \cdot 10^{-8} A \cdot 2.5V= 0.75W$

$P_{total} = P_{dynamic} + P_{static} = 6.69W$

$Time_{depletion}=E_{battery}/P_{total}=39W\cdot hr/6.69W=5.83$ hours

Q10:

$V_{instantaneous} = V_{final} + (V_{initial} - V_{final})\, e^{-t/RC}$

(a) By replacing the PMOSFET with 3.8kΩ,

$V_{DD}/2 = 0 - (V_{DD} - 0)\, e^{-t/3.8k\Omega \cdot 73.2fF}$

$t=\ln 2 \cdot 3.8k\Omega \cdot 73.2fF=0.693 \cdot 2.782 \cdot 10^{-10}= 192.81ps$

(b) PMOSFET will be cut-off when $V_{GS} > V_t$ and for a PMOSFET, the terminal with the higher voltage is source between source and drain terminals. In this problem, the terminal connected to C_L will have the higher voltage, so it works as a source terminal.

The PMOSFET will continue to discharge the C_L, but if C_L is discharged to $|V_{TP}|$=0.5V, the PMOSFET will be cut-off since $V_{GS}=0-V_S=-V_{CL} > V_t=-0.5V$
Therefore the final voltage of the capacitor is $|V_{TP}|$=0.5V

(c) Since we assumed resistor-switch model, the final voltage is still 0. In this equation, we assume there is a sudden change in resistance to infinity when PMOS cuts-off.
$0.5 = 0 - (V_{DD} - 0)\ e^{-t/3.8k\Omega \cdot 73.2fF}$
$t = \ln 5 \cdot 3.8k\Omega \cdot 73.2fF = 0.693 \cdot 2.782 \cdot 10^{-10} = 447.68ps$

(d) Resistor-switch model assumes a constant resistance (3.8KΩ) during a transition before cut-off and a step change in resistance to infinity as the PMOSFET becomes cut-off. However, with a real PMOSFET, on-resistance increases gradually with decreasing |Vgs|. Since R is a function of time that is monotonically increasing, RC time constant and delay will increase over a transition. Therefore, the delay calculated with resistor-switch model may be optimistic. i.e., with a real PMOSFET, it takes more time to get to the final voltage due to long tailed transition.