EECS 312: Digital Integrated Circuits
Midterm Exam

24 November 2009

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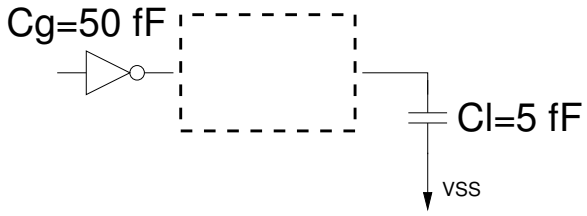
Show your work. Derivations are required for credit; end results are insufficient.
Closed book. No electronic mental aids. One side of one 8.5×11 inch page of notes may be used during the exam. permitted.

Honor Pledge: I have neither given nor received aid in this exam.

Signature:

1 Qualitative questions

1. **(10 pts.)** What is the optimal number of inverter stages to use between the fixed-capacitance inverter and the load in the following circuit? Using no more than three sentences, explain your answer.



2. **(10 pts.)** List two advantages of ratioed logic, and two disadvantages of ratioed logic.

3. **(10 pts.)** For each of the following types of load, indicate the scales (e.g., gate-level) at which the type of load will have a significant impact on circuit behavior:

   (a) Resistive,

   (b) Capacitive, and

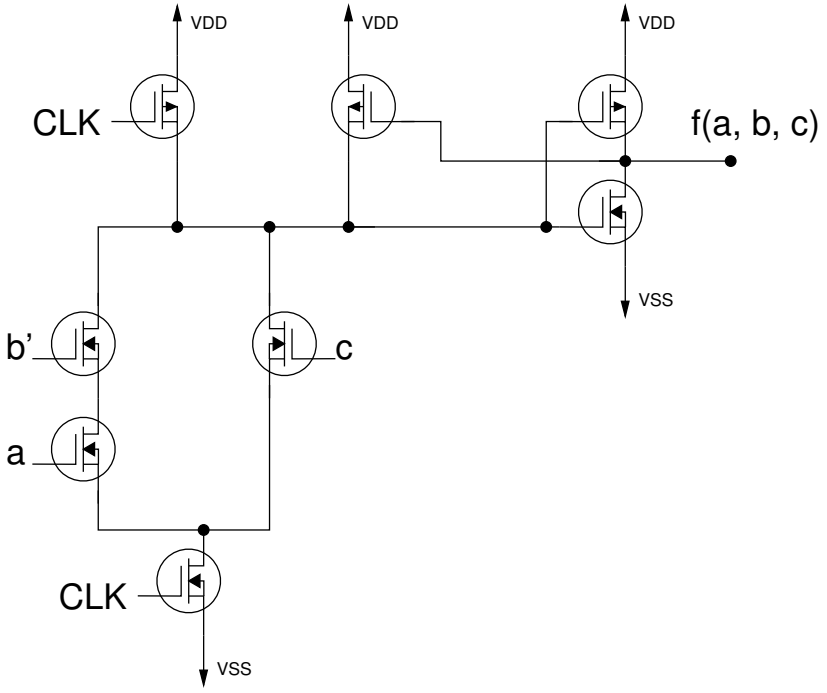
   (c) Inductive.

4. **(10 pts.)** What trend has caused the importance of inter-wire coupling capacitance, relative to substrate coupling capacitance, to increase?

2 Quantitative questions

5. **(10 pts.)** Draw the schematic for a non-inverting Schmitt trigger buffer composed entirely of NMOSFETS and PMOSFETS, i.e., if you need a resistor, use a MOSFET instead. You needn't specify precise transistor sizes, but may specify that individual transistors are wide (use W), medium (use M), or narrow (use N). It is understood that PMOSFETs will have twice the width of NMOSFETS with the same label. When the output of your design changes, this should have little impact on the previous gate, i.e., the gate driving your design, so be sure to have a high resistance at the input of your gate.

6. **(10 pts.)** What function $f(a, b, c)$ does the following circuit implement?



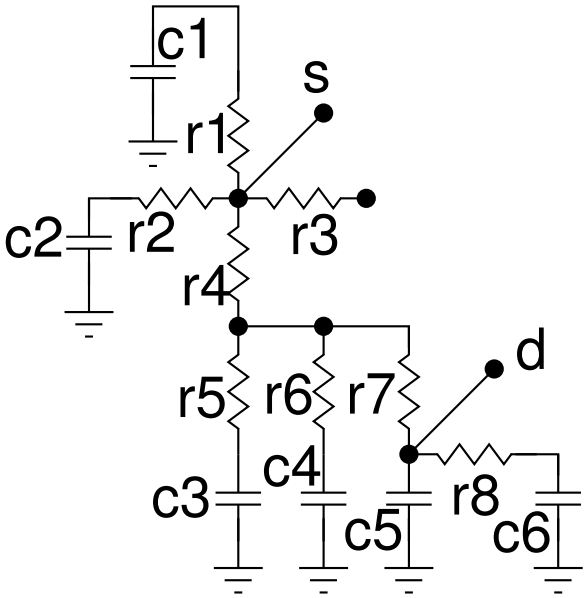
7. **(10 pts.)** Implement the following function using the minimal number of transistors. The output of your implementation should have full output range, from V_{SS} to V_{DD}. However, it needn't be particularly fast. You may use literals as direct inputs.

$$f(a, b, c) = (a\overline{b} + \overline{a}b)c$$

8. **(10 pts.)** Implement the following function as a single logic gate. Indicate the widths of all gates in terms of k, the minimal gate width. Size the transistors to achieve the same worst-case resistance as a balanced, minimal width inverter (i.e., an inverter with a k-wide NMOSFET and a $2k$-wide PMOSFET).

$$f(a, b, c, d) = \overline{a}(b\overline{c} + d)$$

9. **(10 pts.)** What is the Elmore delay time constant for the response at node d to a change at node s in the following circuit?



3 Reference material

	C_{OX} (fF/µm^2)	C_O (fF/µm)	C_j (fF/µm^2)	m_j	ϕ_b (V)	C_{jsw} (fF/µm)	m_{jsw}	ϕ_{bsw} (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

MODELS FOR CMOS DEVICES

CMOS (0.25 µm) – Unified Model.

	V_{T0} (V)	γ ($V^{0.5}$)	V_{DSAT} (V)	k' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	–0.4	–0.4	–1	-30×10^{-6}	–0.1

CMOS (0.25 µm) – Switch Model (R_{eq})

V_{DD} (V)	1	1.5	2	2.5
NMOS (kΩ)	35	19	15	13
PMOS (kΩ)	115	55	38	31

CMOS (0.25 µm) – BSIM Model

See Website: *http://bwrc.eecs.berkeley.edu/IcBook*

Name	Value
kT/q	$25.875\,^{\mathrm{mJ}}/_{\mathrm{C}}$
NMOSFET I_S	21.0 pA
PMOSFET I_S	41.8 pA
n (for I_D calculation)	1.5

VALUES OF MATERIAL AND PHYSICAL CONSTANTS

Name	Symbol	Value	Units
Room temperature	T	300 (= 27°C)	K
Boltzman constant	k	1.38×10^{-23}	J/K
Electron charge	q	1.6×10^{-19}	C
Thermal voltage	$\phi_T = kT/q$	26	mV (at 300 K)
Intrinsic Carrier Concentration (Silicon)	n_i	1.5×10^{10}	cm^{-3} (at 300 K)
Permittivity of Si	ε_{si}	1.05×10^{-12}	F/cm
Permittivity of SiO_2	ε_{ox}	3.5×10^{-13}	F/cm
Resistivity of Al	ρ_{Al}	2.7×10^{-8}	Ω-m
Resistivity of Cu	ρ_{Cu}	1.7×10^{-8}	Ω-m
Magnetic permeability of vacuum (similar for SiO_2)	μ_0	12.6×10^{-7}	Wb/Am
Speed of light (in vacuum)	c_0	30	cm/nsec
Speed of light (in SiO_2)	c_{ox}	15	cm/nsec

FORMULAS AND EQUATIONS

Diode

$$I_D = I_S(e^{V_D/\phi_T} - 1) = Q_D/\tau_T$$

$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1-m)} \times [(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]$$

MOS Transistor

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \text{ (sat)}$$

$$I_D = \upsilon_{sat} C_{ox} W\left(V_{GS} - V_T - \frac{V_{DSAT}}{2}\right)(1 + \lambda V_{DS}) \text{ (velocity sat)}$$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{{V_{DS}}^2}{2}\right) \text{ (triode)}$$

$$I_D = I_S e^{\frac{V_{GS}}{nkT/q}}\left(1 - e^{-\frac{V_{DS}}{kT/q}}\right) \text{ (subthreshold)}$$

Deep Submicron MOS Unified Model

$$I_D = 0 \text{ for } V_{GT} \le 0$$

$$I_D = k'\frac{W}{L}\left(V_{GT}V_{min} - \frac{V_{min}^2}{2}\right)(1 + \lambda V_{DS}) \text{ for } V_{GT} \ge 0$$

with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$

and $V_{GT} = V_{GS} - V_T$

MOS Switch Model

$$R_{eq} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1 + \lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1 + \lambda V_{DD}/2)}\right) \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{5}{6}\lambda V_{DD}\right)$$

Inverter

$$V_{OH} = f(V_{OL})$$

$$V_{OL} = f(V_{OH})$$

$$V_M = f(V_M)$$

$$t_p = 0.69 R_{eq} C_L = \frac{C_L(V_{swing}/2)}{I_{avg}}$$

$$P_{dyn} = C_L V_{DD} V_{swing} f$$

$$P_{stat} = V_{DD} I_{DD}$$

Static CMOS Inverter

$$V_{OH} = V_{DD}$$

$$V_{OL} = GND$$

$$V_M \approx \frac{rV_{DD}}{1+r} \quad \text{with} \quad r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}}$$

$$V_{IH} = V_M - \frac{V_M}{g} \qquad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

with $g \approx \frac{1+r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} = 0.69 C_L\left(\frac{R_{eqn} + R_{eqp}}{2}\right)$$

$$P_{av} = C_L V_{DD}^2 f$$

Interconnect

Lumped *RC*: $t_p = 0.69\ RC$

Distributed *RC*: $t_p = 0.38\ RC$

RC-chain:

$$\tau_N = \sum_{i=1}^{N} R_i \sum_{j=i}^{N} C_j = \sum_{i=1}^{N} C_i \sum_{j=1}^{i} R_j$$

Transmission line reflection:

$$\rho = \frac{V_{refl}}{V_{inc}} = \frac{I_{refl}}{I_{inc}} = \frac{R - Z_0}{R + Z_o}$$

CMOS COMBINATIONAL LOGIC

Transistor Sizing using Logical Effort

$$F = \frac{C_L}{C_{g1}} = \prod_1^N \frac{f_i}{b_i} \qquad G = \prod_1^N g_i \qquad D = t_{p0}\sum_{j=1}^{N}\left(p_j + \frac{f_j g_j}{\gamma}\right)$$

$$B = \prod_1^N b_i \qquad H = FGB \qquad D_{min} = t_{p0}\left(\sum_{j=1}^{N} p_j + \frac{N(\sqrt[N]{H})}{\gamma}\right)$$

Definitions useful in gate sizing	
g_i	Gate logical effort. Ratio of input capacitor to equal on-resistance inverter.
$G = \prod_{i=1}^{n} g_i$	Path logical effort.
$H = \frac{C_{out}}{C_{in}}$	Path electrical effort.
$b = \frac{C_{total}}{C_{useful}}$	Stage branching effort.
$B = \prod_{i=1}^{n} b_i$	path branching effort.
$F = GBH$	path effort.
$\hat{f} = g_i h_i = \sqrt[n]{F}$	Optimal stage effort.
$\hat{h_i} = \frac{\hat{f}}{g_i} = \frac{C_{i,out}}{C_{i,in}}$	Optimal stage electrical effort.
$D_i = G_i h_i + p_i$:	Stage delay.

For sizing inverters, $\forall_{i=1}^{n} b = g = 1$.