EECS 312: Digital Integrated Circuits
Final Exam Solutions

23 April 2009

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Show your work. Derivations are required for credit; end results are insufficient.
Closed book. You may use a calculator.

Honor Pledge: I have neither given nor received aid in this exam.

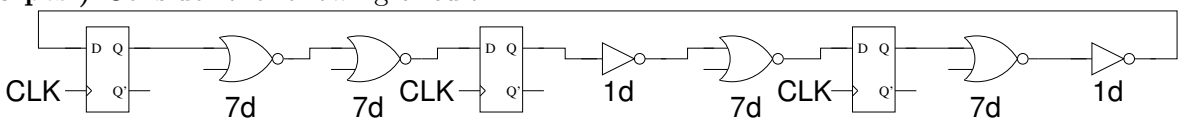
Signature:

1. **(10 pts.)** $k_n = \frac{W\mu_n\epsilon_{ox}}{Lt_{ox}}$ When the move from SiO_2 to high-κ gate dielectric occurred, what qualitative changes were made to the variables upon which k_n depends? You may assume that k_n remains fixed. Use only a few sentence fragments for your answer.

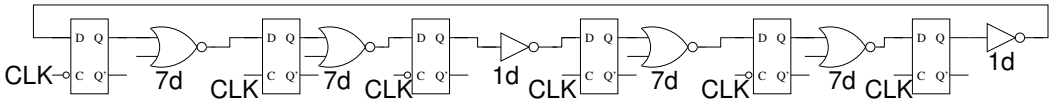
   $\epsilon_{ox} \uparrow, t_{ox} \uparrow$.

   Note: If you didn't get this one, please read the Spectrum article and the midterm solutions.

2. **(10 pts.)** Consider the following circuit:



   The numbers near the logic gates indicate delays. Disconnected logic gate inputs may be assumed to be stable. Draw the gate- and latch-level diagram of a two-phase latch-based reimplementation of this circuit and indicate the minimal safe clock period. Do not change anything but the positions of the latches. You may neglect latch delays.



   The clock period must clearly be greater than

$$p = 2\sum_{i=0}^{n-1} d_i/n = 10d.$$

   Given that

$$\phi_{i+1} = \phi_i - p/2 + d_i,$$

   we can compute the phase each stage:

$$\phi_0 = 2d, \phi_1 = 4d, \phi_2 = 0d, \phi_3 = 2d, \phi_4 = 4d, \phi_5 = 0d.$$

$$\max_{i=0} n - 1\phi_i - \min_{i=0} n - 1\phi_i = 4d - 0d = 4d$$

$4d < p/2(5d)$ **so the minimal period of** $10d$ **is valid.**

3. **(10 pts.)** Indicate two ways of programming floating-gate transistors and two ways of erasing floating-gate transistors. It is fine for the methods to require slightly different floating gate transistor designs. Use at most four short phrases.

   Programming

   - **Fowler-Nordheim tunneling from source or drain to floating gate or**
   - **Avalanche injection of hot carriers accelerated between source and drain.**

   Erasing

   - **Exposure to ultraviolet light, the photons of which impart enough energy to charge carriers in the floating gate to overcome the energy barrier separating the floating gate from other nodes or**
   - **Fowler-Nordheim tunneling from the gate to source or drain.**

4. **(10 pts.)** Draw the transistor-level diagram for a sense amplifier that reprograms the read value. Your circuit should have the following inputs: *read–program*, *equalize*, *bit*, and $\overline{bit}$. You may not assume access to complemented input literals.

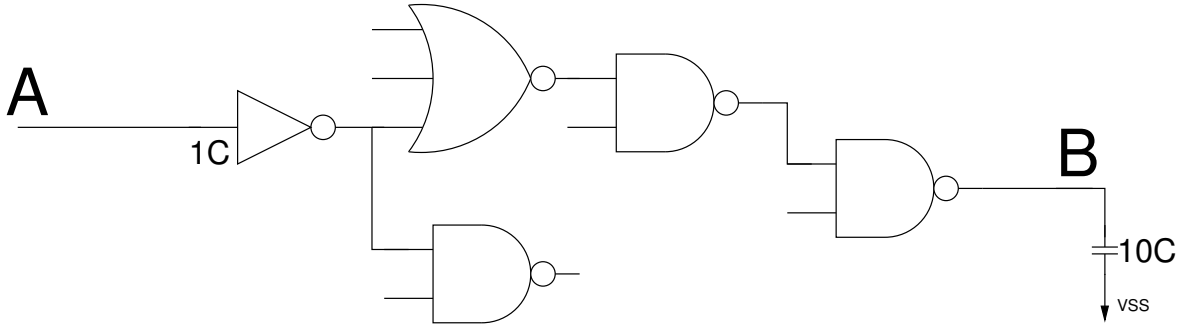
   See the textbook's diagram of a DRAM sense amplifier. An additional inverter is necessary to invert the *read–program* signal used to control the PMOSFET in series with the amplifier.

5. **(10 pts.)** Draw a gate-level diagram for a three-bit carry-lookahead adder. Correctness counts the most, but efficiency also counts. You may use hierarchy. In other words, once you show how to construct something more complex than a standard logic gate, you can assign a symbol to it and reuse that symbol.

$$p_i = a_i \oplus b_i$$
$$g_i = a_i b_i$$
$$s_i = a_i \oplus b_i \oplus ci_i$$
co_i **not used**
$$ci_0 = 0$$
$$ci_1 = g_0$$
$$ci_2 = g_1 + p_1 g_0 = \overline{\overline{g_1}\,\overline{p_1 g_0}}$$
$$ci_2 = g_2 + p_2(g_1 + p_1 g_0) = g_2 + p_2 g_1 + p_2 p_1 g_0 = \overline{\overline{g_2}\,\overline{p_2 g_1}\,\overline{p_2 p_1 g_0}}$$

The schematics are straight-forward, and are left as an exercise to the reader. You can verify your results using the textbook.

6. **(10 pts.)** Use the concept of logical effort to size the gates in the following circuit to minimize the delay for path $A \rightarrow B$.



You need not round your sizes.

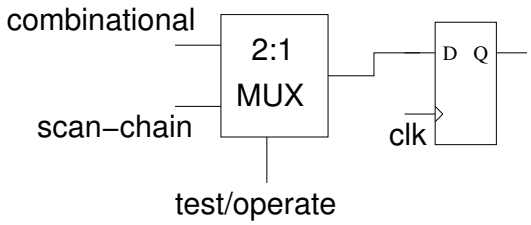
$$
\begin{aligned}
F &= BGH \\
B &= \frac{7/3 + 4/3}{7/3} = \frac{11}{7} = 1.57 \\
G &= 1\frac{7}{3}\frac{4}{3}\frac{4}{3} = 4.15 \\
H &= 10C/C = 10 \\
F &= 65.16 \\
\hat{f} &= \sqrt[4]{65.16} = 2.84 \\
\hat{h_i} &= \hat{f}/g_i \\
\hat{h_4} &= 2.13 \\
\hat{h_3} &= 2.13 \\
\hat{h_2} &= 1.22 \\
\hat{h_1} &= 2.84 \\
h_i &= Cout_i/Cin_i \\
Cin_i &= Cout_i/h_i \\
C\hat{in}_i &= C\hat{out}_i/\hat{h}_i \\
C\hat{in}_4 &= 10C/2.13 = 4.69C \\
C\hat{in}_3 &= 4.69C/2.13 = 2.20C \\
C\hat{in}_2 &= 2.20C/1.22 = 1.80C \\
C\hat{in}_1 &= \frac{1.80C + 1.80C \cdot 4/7}{2.84} = 1.00C
\end{aligned}
$$

7. **(10 pts.)** Draw a transistor-level diagram of a 3:8 decoder in which the transistors are sized to achieve the same output resistance to ground and V_{DD} as an inverter with gate capacitance $3C$.

This is a set of three-input NOR gates in which the PMOSFETs have

gate capacitances of $6C$ and the NMOSFETs have gate capacitances of C. You may assume access to complemented input literals, but no credit will be taken off for those who include inverters in their designs.

8. **(10 pts.)** Draw the gate-level diagram of a rising edge triggered scan-flop, i.e., a flip-flop that can be used to support normal operation and scan-chain testing. You may use transistors in addition to logic gates. If sizing is essential for correct operation, label the appropriate gates and/or transistors as "narrow" and "wide".



Instead of showing all the possible designs of the D flip-flop and 2:1 MUX, the reader can refer to the textbook.

9. **(10 pts.)** Determine the worst-case delay from precharge disable to output transition for a single-bit cell in a four-word MOS NAND ROM. λ =125 nm. All gates are 2λ long and 4λ wide. Sources and drains are 3λ long and 4λ wide. Assume (1) a default 0.25 µm process, (2) all inputs experiences a perfect step voltage change, and (3) an output capacitance of 10 fF.

See Figure 12-13 on page 639 in the textbook (Rabaey et. al) for the NAND ROM schematic. We replace the grounded PMOS inputs with a precharge PMOS and add an NMOS footer below the NMOS stack. Note that if one assumes that the wordline inputs change before the end of the precharge period, the footer is not necessary.

Assume that bits 0-2 store logic 1 values and bit 3 stores a logic 0 value. The worst case delay will occur when reading bit 3, because the output must discharge through the three NMOS controlled by wordlines 0–2 and the footer. Assume that bit 3 is implemented by a wire, as shown in Figure 12-13 in the book.

We compute the Elmore delay of the equivalent RC network. Note that when determining the capacitances, due to the step function (i.e., instantaneous) inputs we include only the diffusion caps and not gate caps. Many of the diffusion caps will only charge to $V_{dd} - V_{th}$ during precharge, but for Elmore delay calculations we assume they charge to the full V_{dd}. This will result in acceptable error.

The source and drain caps are given by Equation 3.45 on page 111 in the textbook.

The PMOS drain cap is 0.631 fF.
The NMOS source and drain caps are 0.725 fF.
The NMOS equivalent resistance 6.5 kΩ.

Thus, the Elmore delay is given by

$$11.36f \cdot (4 \cdot 6.5k) + 1.45f \cdot (3 \cdot 6.5k) + 1.45f \cdot (2 \cdot 6.5k) + 1.45f \cdot (6.5k)$$

which equals 0.35 ns.