EECS 303: Advanced Digital Logic Design
Final Exam

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Show your work. Derivations are required for credit; end results are insufficient.

1. Use the Quine–McCluskey method to find a minimal *product-of-sums* expression for the following function:
$$f(a, b, c) = \sum(3, 4)$$
Do not skip any steps.

2. What is $\mathcal{NP}$-Completeness? Use three or fewer sentences to answer.

3. When faced with an $\mathcal{NP}$-Complete problem during the design of a digital system, what are your options, and what are the advantages and disadvantages of each option? For each option, use only a few words to list advantages and disadvantages.

4. Consider the following cover:

```
000X
0X00
0X01
X1XX
X11X
1XXX
```

   (a) Determine cubes are relatively essential, totally redundant, and partially redundant.
   (b) Indicate the minimal subset of cubes covering the initial on-set.

5. Use kernel extraction to minimize the following function:
$$f(a, b, c, d) = \sum(0, 2, 5, 7, 8, 9, 10, 11, 12, 14, 15)$$

6. Explain, using up to three sentences, the *main* reason for switching to a high-k gate dielectric in 45 nm process technology.

7. Draw a side-view diagram for a floating-gate transistor and use up to three sentences to explain its operation.

8. Show the diagram for a multiplier that takes unsigned 4-bit operands. Use only AND gates and half adders.

9. Show a minimal state diagram and state assignment for a T flip-flop that is both rising and falling edge active.

10. Show the state diagram for a finite state machine that outputs a one if and only if it has received the sequence 001 at any time in the past or it has just received the sequence 01.

11. Name the following device and indicate a commonly-used component in which it is used. Correct component names that reveal no knowledge such as "a computer" will receive no credit.

```
ENTITY example IS
        PORT (
                a, b, c: IN bit;
                f: OUT bit
        );
END example;

ARCHITECTURE arch OF example IS
BEGIN
        f <= (a AND b) OR (a AND c) OR (b AND c);
END arch;
```

12. In the third lab assignment (the one on the video controller), separate address and data busses were used. If the number of input/output ports on the processor, video controller, and memory chips were tightly constrained, would it be possible to time multiplex use of a single bus for both address and data transmission? Would doing so have change timing diagram cycle used in this lab? Use three or fewer sentences to answer.