Introduction to Computer Engineering – EECS 203

http://ziyang.eecs.northwestern.edu/~dickrp/eecs203/

Instructor:	Robert Dick	TA:	Neal Oza
Office:	L477 Tech	Office:	Tech. Inst. L375
Email:	dickrp@northwestern.edu	Phone:	847-467-0033
Phone:	847–467–2298	Email:	nealoza@u.northwestern.edu
		TT:	David Bild
		Office:	Tech. Inst. L470
		Phone:	847-491-2083
		Email:	d-bild@northwestern.edu

NORTHWESTERN UNIVERSITY

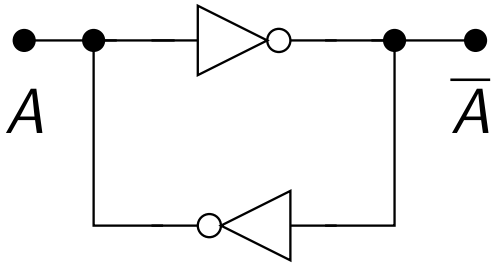
Memory

- Combinational logic outputs a function of inputs, only
- Sequential logic outputs a function of inputs and *state*
- State is remembered
- Consider a sequential vending machine

Flip-flop introduction

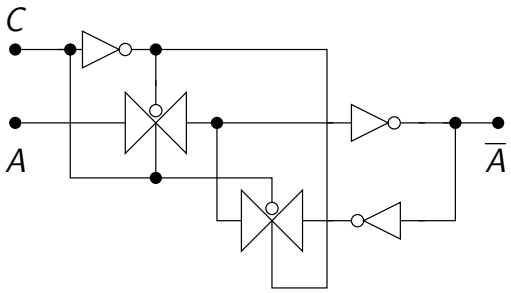
- Stores, and outputs, a value
- Puts a special clock signal in charge of timing
- Allows output to change in response to clock transition
- More on this later
  - Timing and sequential circuits

Feedback and memory



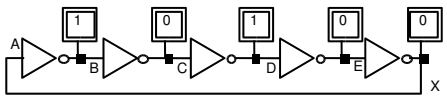
- Feedback is the root of memory
- Can compose a simple loop from NOT gates
- However, there is no way to switch the value

TG and NOT-based memory



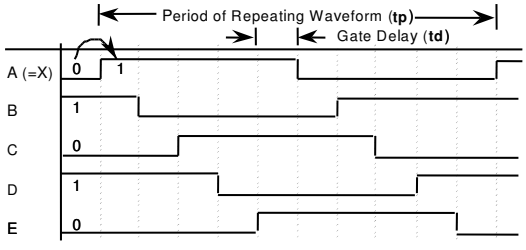
- Can break feedback path to load new value
- However, potential for timing problems

Ring oscillators

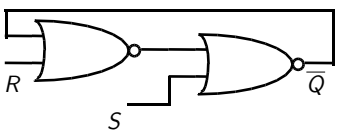


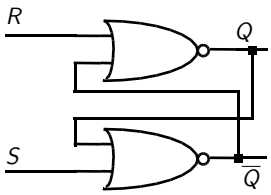
Like pulse shaping circuits with memory

Ring oscillators

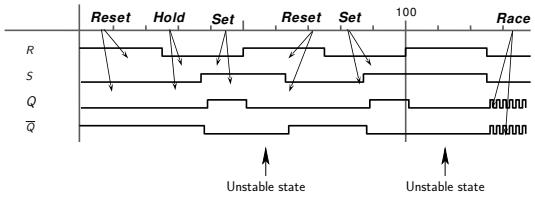


Reset/set latch

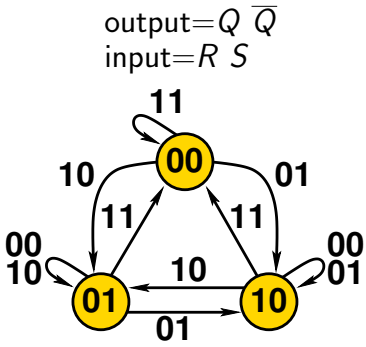




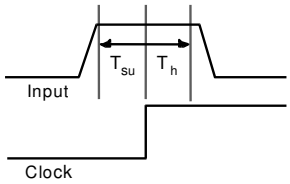
Reset/set timing



RS latch state diagram

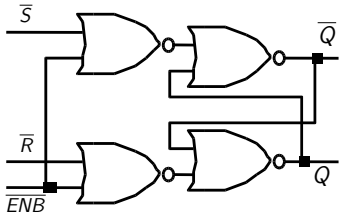


Clocking terms

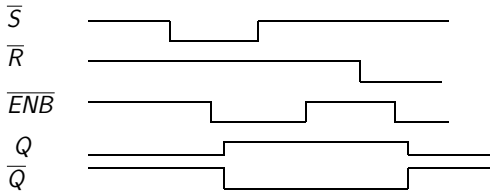


- Clock – Rising edge, falling edge, high level, low level, period
- Setup time: Minimum time before clocking event by which input must be stable (T_{SU})
- Hold time: Minimum time after clocking event for which input must remain stable (T_H)
- Window: From setup time to hold time

Gated RS latch



Gated RS latch

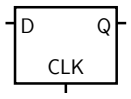


Memory element properties

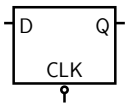
Type	Inputs sampled	Outputs valid
Unclocked latch	Always	LFT
Level-sensitive latch	Clock high (T_{SU} to T_H) around falling clock edge	LFT
Edge-triggered flip-flop	Clock low-to-high transition (T_{SU} to T_H) around rising clock edge	Delay from rising edge

Clocking conventions

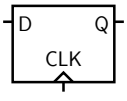
Active-high transparent



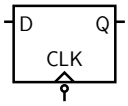
Active-low transparent



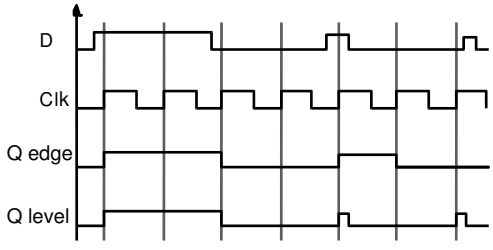
Positive (rising) edge



Negative (falling) edge



Timing for edge and level-sensitive latches



Summary

- Memory
- Latches
- Flip-flops (more on these later)

Reading assignment

- M. Morris Mano and Charles R. Kime. *Logic and Computer Design Fundamentals*. Prentice-Hall, NJ, fourth edition, 2008
- Sections 5.1–5.7
- Sections 6.1–6.4

Computer geek culture reference

Computer security

- PGP
- (Open)SSH
- (Type II) remailers
- Wireshark
- Crack