Homework 2

EECS 203

Due 18 April 2008

Prepared by Robert Dick and Russ Joseph

"Mano" is M. M. Mano and C. R. Kime, *Logic and Computer Design Fundamentals*. Prentice-Hall, NJ, fourth ed., 2008.

Please keep track of how long you spend doing this homework assignment. Specifically, how much time is needed to do the problems after studying enough to understand the concepts?

Please note that the assigned homework may not be enough for some people. If the concepts are still a little fuzzy after doing the homework, please take advantage of the other problems in Mano and/or see me for more problems.

Refer to Table 1.2 in Mano if you need help converting between decimal and binary numbers.

When you can verify an answer, e.g., by using a truth table, check it.

1. **(0 pts.)** Do Mano 2.10, 2.12, 2.15, 2.22, and 2.25. Check your solutions using the information on the book webpage. If these problems are difficult, see me or a TA.
2. **(10 pts.)** CMOS and TTL review
   (a) Draw the schematic for a CMOS inverter constructed from one NMOS and one PMOS transistor
   (b) What happens if the input to a CMOS logic gate, e.g., an inverter is not connected?
   (c) Draw the schematics for two CMOS inverter connected in series
   (d) If the input to the first inverter has not changed recently, and the output of the second inverter is not connected to anything, is current presently flowing in the circuit?
      - Note to circuits geeks: Assume the gate oxide is a perfect insulator and ignore leakage current – treat the transistors like digital switches.
3. **(15 pts.)** Lab preparation
   (a) Draw a schematic for a circuit that uses a resistor and SPST switch (like the one in your lab kit) to produce a high signal when the switch is open and a low signal when the switch is closed.
   (b) What logic family is the 74LS00 in?
   (c) What does the "LS" in 74LS00 stand for?
   (d) Why is it often useful to put a resistor in series with a light-emitting diode?
   (e) What is a DIP package?

(f) Removing tight DIP packages from a breadboard with your fingers can cause pins to bend. What color is your lab kit's DIP chip puller?

(g) What happens if the input to a TTL logic gate is not connected?

4. **(5 pts.)** Give the truth table for a three-input function that can not be implemented using one-level logic. Do not use even parity (XNOR) or odd parity (XOR) as an example.

5. **(10 pts.)** Use Karnaugh maps to find minimal SOP expressions for the following functions

   (a) $f(a,b,c) = \sum(0,1,6) + d(2,3)$

   (b) $f(a,b,c) = \sum(2,7) + d(0,5,6)$

6. **(10 pts.)** Use (inverted) Karnaugh maps and De Morgan's Laws to find minimal POS expressions for the following functions

   (a) $f(a,b,c) = \sum(0,7) + d(1,2,4,5)$

   (b) $f(a,b,c) = \sum(1,2,6) + d(3,5)$

7. **(20 pts.)** Consider the following function.

$$f(a,b,c,d) = \sum(1,2,5,7,13) + d(0,6,10,15)$$

   (a) Show its truth table

   (b) Use a Karnaugh map to find the corresponding minimal SOP expression

   (c) Use a Karnaugh map to find the corresponding minimal POS expression

   (d) Use De Morgan's Laws or "bubble pushing" to convert the SOP expression that can be directly implemented with only NAND and NOR gates

   (e) Draw the schematic for the resulting NAND/NOR circuit

8. **(10 pts.)** Implement the following function in CMOS logic with the minimum number of transistors. Assume that you do NOT have complemented inputs available to you.

$$f(a,b,c,d) = \overline{b}\ \overline{d}\ + \overline{b}\ \overline{c}\ + \overline{a}\ \overline{d}\ + \overline{a}\ \overline{c}$$

9. **(0 pts.)** How much time did you spend on this assignment?

10. **(0 pts.)** Were there any problems that were mostly busy-work? In other words, were there any problems that required a lot of time without helping you to learn new concepts? If so, which ones.

11. **(0 pts.)** Were there any problems for which the lectures and book didn't give you enough background information? If so, which ones?