Homework 1
EECS 203
Due 11 April
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"Mano" is M. M. Mano and C. R. Kime, *Logic and Computer Design Fundamentals*. Prentice-Hall, NJ, fourth ed., 2008.

Please keep track of how long you spend doing this homework assignment. Specifically, how much time is needed to do the problems after studying enough to understand the concepts?

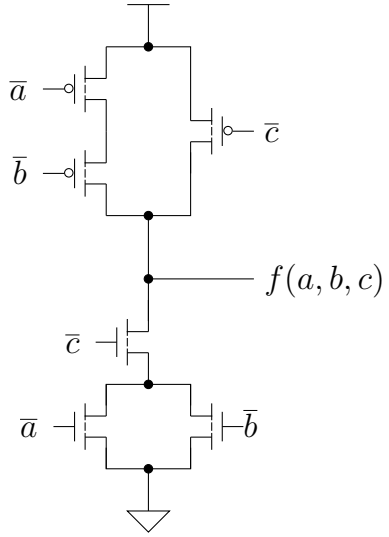
Please note that the assigned homework may not be enough for some people. If the concepts are still a little fuzzy after doing the homework, please take advantage of the other problems in Mano and/or see me for more problems.

1. Do and self-check Mano 2.1, 2.2, and 2.9 (don't hand in). If this is difficult, see me or a TA.
2. **(10 pts.)** Find a minimum literal count Boolean formula for a function with the following truth table.

a	b	c	d	f(a, b, c, d)
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

3. **(10 pts.)** *Mano 2.3.a* Prove the identity of the following Boolean equation using algebraic manipulation:
$$AB\overline{C} + B\overline{C}\,\overline{D} + BC + \overline{C}\,D = B + \overline{C}\,D$$
4. **(10 pts.)** *Mano 2.4* Suppose that $A \cdot B = 0$ and $A + B = 1$. Use algebraic manipulation to prove that
$$(A + C) \cdot (\overline{A} + B) \cdot (B + C) = B \cdot C$$
5. **(10 pts.)** *Mano 2.8* Using DeMorgan's Theorem, express the function
$$F = \overline{A}\,BC + \overline{B}\,\overline{C} + A\overline{B}$$
   - with only OR and complement operations
   - with only AND and complement operations

6. **(10 pts.)** Consider the following CMOS circuit diagram



   (a) Is this implementation safe? In other words, can ground and power be shorted or will the output ever be left in a high impedance state?

   (b) Give a truth table for the implemented function.

   (c) Write a minimum literal count Boolean formula for the function.

7. **(10 pts.)** A two-input XNOR gate implements the following function:

$$f(a,b) = ab + \overline{a}\,\overline{b}$$

   Show how to implement this gate using only transmission gates. Note that more efficient implementations are possible.

8. **(10 pts.)** OR gate implementation

   (a) Draw the circuit diagram of a three-input OR gate using only NMOS and PMOS transistors. Use the minimal number of transistors necessary to build a correctly functioning gate. For this problem, please do not assume that you can complement inputs with zero cost, i.e., if you need to invert something, use an inverter.

   (b) If you can't do this with three PMOS and three NMOS transistors, use one sentence to explain why.

9. How much time did you spend on this assignment?

10. Were there any problems that were mostly busy-work? In other words, were there any problems that required a lot of time without helping you to learn new concepts? If so, which ones.