## Quiz (0 pts.) EECS 203 Prepared by Robert Dick

- 1. Draw a diagram of a transmission gate composed of NMOS and PMOS transistors.
- 2. Draw a gate-level schematic for an implementation of the following function using only NAND and NOR gates. You may assume access to complemented and uncomplemented inputs.

$$f(a,b,c) = (a+b)\overline{c}$$

3. Find a minimal POS formula for the following function:

$$f(a, b, c) = \sum (0, 2, 4) + d(1, 5, 7)$$