Midterm exam
ECE 203
24 October 2005
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You may not use books, notes, or calculators when completing this exam.
Please show your work.
Please look over all the problems now and ask questions if any of them are not clear.
(*n* pts.) Means the problem is worth *n* points.
Good luck!

1. **(10 pts.)** Consider a CMOS-like process with a V_{DD} of 5 V and a threshold of (-)0.7 V. The inverter output voltage, $V_{out}(V_{in})$, is the following function of input voltage, V_{in},

$$V_{out}(V_{in}) = \begin{cases} 4.75\,\mathrm{V} - V_{in} \text{ if } V_{in} \leq 2.25\,\mathrm{V} \\ 2.5\,\mathrm{V} \text{ if } 2.25\,\mathrm{V} < V_{in} < 2.75\,\mathrm{V} \\ 5.25\,\mathrm{V} - V_{in} \text{ if } V_{in} \geq 2.75\,\mathrm{V} \end{cases}$$

   NAND and NOR gates have similar transfer functions, i.e., they do not restore.

   (a) Can this logic be safely used to implement all Boolean functions? Why? An explanation is necessary.

   (b) Can this logic be safely and efficiently used to implement all Boolean functions? Why? An explanation is necessary.

2. **(5 pts.)** Use a Karnaugh map to find the minimal SOP expression for the following function.

$$f(a,b,c,d) = \sum(0,4,5,6,7,11,12,14,15) + d(2,3,13)$$

3. **(5 pts.)** Use the Quine-McKluskey method to minimize the following function

$$f(a,b,c) = \sum(1,2,4,5) + d(3)$$

4. **(10 pts.)** Implement a 2:1 MUX using as few 1:2 DMUXs as possible.

5. **(3 pts.)** Is it possible to build a transmission gate out of two-input NAND gates? If so, show the diagram. If not, explain why.

6. **(3 pts.)** Is it possible to build a two-input NAND gate out of transmission gates? If so, show the diagram. If not, explain why.

7. **(14 pts.)** Graduate students in Northwestern University's EECS department have discovered a new, extremely fast, and compact device technology with which it is possible to fabricate only OR and NOT gates. Show the schematic for a six-bit two's-complement carry-select adder with overflow detect that uses three-bit ripple-carry chains. Use hierarchy, i.e., if you need an AND, build the AND from OR and NOT, then use the AND. Efficiency counts but points will not be deducted for slight imperfections such as using a full-adder when a half-adder would do.